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Circuit Implementation of an A/D Converter Based on the Negative β-Map with a Discrete-Time Integrator

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Abstract—We propose design methods of an A/D converter based on a negative β-map, which is robust against noise, and mismatches and deviations in circuit devices, using a discrete-time damped-integrator suitable for IC implementation. In addition, we propose two SC circuit examples for the A/D converter based on the negative β-map. Moreover, we directly apply the A/D converter to a chaos generator with simple modifications. Because the trajectories of the negative β-map is confined in an invariant subinterval, the resulting chaos generator is robust against circuit non-idealities and noise. Finally, we confirm the proposed methods and circuits through SPICE simulations with ideal circuit elements.

1. Introduction

A data conversion method with a radix of a positive real number (β-converter) has been proposed [1, 2]. The β-converters are Nyquist-rate converters with exponential bit-rate accuracy like PCM-type converters, and also robust against circuit deviations and noise like oversampled $\Sigma\Delta$-type converters. Furthermore, another data conversion method with a radix of a negative real number has been proposed based on a negative β-map [3, 4]. The size of an invariant subinterval of an ordinary β-map is fixed, but the position of that is translated according to the quantizer threshold [1, 2]. In contrast, an invariant subinterval of the negative β-map stays around the center of the domain of the map, however, the size of it varies with the quantizer threshold. In addition, the size of the invariant subinterval most expands when the quantizer threshold is set at either edge of the permissible range, so that a possible dynamic range of the converter becomes large [3, 4]. Therefore, the conversion method based on the negative β-map improves conversion accuracy, in particular, near the upper and lower bounds of the permissible range of the quantizer threshold value.

A circuit block diagram of the data encoder (A/D converter) based on the negative β-map has been proposed [3, 4]. However, the block diagram is not suitable for practical circuit implementation, especially for IC implementation. Therefore, in this paper, we propose design methods of the A/D converter based on the negative β-map with a discrete-time integrator suitable for IC implementation. Moreover, two examples of switched-capacitor (SC) circuits for the A/D converter based on the negative β-map are constructed with the proposed methods.

In addition, we apply the proposed A/D converter circuits to a chaos generator by setting the bit-length of the A/D converters infinity. The trajectories of the negative β-map are confined in a finite invariant subinterval because the map is eventually locally onto. Therefore, the proposed chaos generators are robust against mismatches of the circuit elements and noise, that is, they are stable without divergence of the trajectories.

Finally, SPICE simulation results with ideal circuit elements are shown in oder to demonstrate feasibility of the proposed methods and circuits.

2. Data Converter Based on the Negative β-Map

The negative β-map $R(\cdot)$ is given by eq. (1) [3, 4].

$$R(x) = \begin{cases} s - \beta x, & x \in [0,\ \gamma\nu), \\ \beta s - \beta x, & x \in [\gamma\nu,\ s), \end{cases} \tag{1}$$

where $\nu \in [s(\beta-1),\ s)$ is a threshold parameter, $-2 < -\beta < -1$ is a radix of the conversion, $s > 0$ is a scaling parameter, and $\gamma = 1/\beta$. Let us define discrete-time t_n (n is an integer). Then, we can rewrite eq. (1) as a one-dimensional discrete-time dynamical system as

$$x(t_{n+1}) = R(x(t_n)) = \begin{cases} s - \beta x(t_n), & x(t_n) \in [0,\ \gamma\nu), \\ \beta s - \beta x(t_n), & x(t_n) \in [\gamma\nu,\ s). \end{cases} \tag{2}$$

Next, we define a binary variable $b(t_n) \in \{0,\ 1\}$ as

$$b(t_n) = Q_\theta(x(t_n)) = \begin{cases} 0, & x(t_n) \in [0,\ \theta), \\ 1, & x(t_n) \in [\theta,\ s), \end{cases} \tag{3}$$

where $Q_\theta(\cdot)$ is a quantizer with threshold of $\theta = \gamma\nu$. As a result, eq. (2) can be rewritten as

$$x(t_{n+1}) = \overline{b(t_n)}s + b(t_n)\beta s - \beta x(t_n) = s\left(\overline{b(t_n)} + \beta b(t_n)\right) - \beta x(t_n). \tag{4}$$

We can rewrite eq. (2) in a different way as

$$\begin{aligned} x(t_{n+1}) &= s\left(\overline{b(t_n)} + \beta b(t_n)\right) - \beta x(t_n) \\ &= s\left(\overline{b(t_n)} + b(t_n) + (\beta-1)b(t_n)\right) - \beta x(t_n) \quad (5) \\ &= s(1 + (\beta-1)b(t_n)) - \beta x(t_n). \quad (6) \end{aligned}$$

Let us sample an input signal x_{input} at $t = t_1$ as

$$x(t_1) = x_{input}. \tag{7}$$

Then, we can obtain a binary sequence $BS_L(x_{input})$ given in eq. (8) by repeating eq. (4) or eq. (6) from $t = t_1$ to $t = t_L$ (L is a bit-length of the A/D conversion).

$$BS_L(x_{input}) = (b_1 b_2 \cdots b_L)_{-\beta,s}, \tag{8}$$

where $b_n = b(t_n)$ $(n = 1, 2, \ldots, L)$, $b_1 = b(t_1)$ is the MSB, and $b_L = b(t_L)$ is the LSB.

The permissible range (tolerance σ_ν) of ν is given by $\sigma_\nu = s(2-\beta)$ [3, 4]. Therefore, θ can fluctuate in a range σ_θ given by

$$\sigma_\theta = \gamma\sigma_\nu = \gamma s(2-\beta) = s(2\gamma - 1). \tag{9}$$

That is, even if the value of θ is fluctuated because of environmental changes, non-ideal characteristics of the circuit elements, and noise, the A/D converter based on the negative β-map works correctly if the value of θ remains in the range of σ_θ.

Moreover, the value of β in the real circuit can be well estimated from the observed bit-sequences using the characteristic equation [1, 2, 3, 4].

3. Implementation of the A/D Converter Based on the Negative β-Map with a Discrete-Time Integrator

A discrete-time integrator is favorable in analog sampled-data ICs. Many switched-capacitor (SC) and switched-current (SI) circuits, for example, which are effective for IC implementation of the discrete-time integrators, have been proposed and matured. Some of those discrete-time integrator circuits are robust against the non-ideal characteristics and mismatches of circuit devices, parasitic devices, and noise. Therefore, we propose two design methods to construct the A/D converter based on the negative β-map through the discrete-time integrator in this section.

3.1. Design Method Based on eq. (4)

The Z transformation of eq. (4) results in

$$X(z) = s\left(\overline{B(z)} + \beta B(z)\right)z^{-1} - \beta X(z)z^{-1}, \tag{10}$$

where $X(z)$, $B(z)$, and $\overline{B(z)}$ are Z-domain variables for $x(t_n)$, $b(t_n)$, and $\overline{b(t_n)}$, respectively. Moreover, from eq. (3),

$$B(z) = Q_\theta(X(z)), \text{ and } \overline{B(z)} = \overline{Q_\theta(X(z))}. \tag{11}$$

Therefore,

$$X(z) = s\left(\overline{Q_\theta(X(z))} + \beta Q_\theta(X(z))\right)z^{-1} - \beta X(z)z^{-1}. \tag{12}$$

As a consequence,

$$X(z) = s \cdot \frac{z^{-1}}{1+\beta z^{-1}} \cdot \left(\beta Q_\theta(X(z)) + \overline{Q_\theta(X(z))}\right). \tag{13}$$

This shows that a discrete-time integrator with a damping-factor of β can construct the A/D converter circuit based on the negative β-map.

3.2. Design Method Based on eq. (5)

The Z-transformation of eq. (5) gives

$$\begin{aligned} X(z) &= s\left(\overline{B(z)}z^{-1} + B(z)z^{-1} + (\beta-1)B(z)z^{-1}\right) - \beta X(z)z^{-1} \\ &= s\{1 + (\beta-1)B(z)\}z^{-1} - \beta X(z)z^{-1} \\ &= s\left\{1 + (\beta-1)Q(X(z))\right\}z^{-1} - \beta X(z)z^{-1}. \end{aligned} \tag{14}$$

As a result,

$$X(z) = s \cdot \frac{z^{-1}}{1+\beta z^{-1}} \cdot \{(\beta-1)Q(X(z)) + 1\}. \tag{15}$$

This suggests another method to construct the A/D converter circuit based on the negative β-map utilizing a discrete-time integrator with a damping-factor of β.

4. SC Circuit Implementation of the A/D Converter Based on the Negative β-Map

We use a SC damped-integrator circuit shown in Fig. 1, as an illustration, to implement the A/D converter based on the negative β-map given by eqs. (13) and (15). The Z-domain transfer function of the circuit in Fig. 1 is

$$V_o(z) = \frac{z^{-1}}{1 + \left(\frac{C_k}{C_i} - 1\right)z^{-1}} \cdot \left(\frac{C_{f0}}{C_i}V_{i0}(z) + \frac{C_{f1}}{C_i}V_{i1}(z)\right), \tag{16}$$

where $V_o(z)$, $V_{i0}(z)$, and $V_{i1}(z)$ are Z-domain variables for $v_o(t_n)$, $v_{i0}(t_n)$, and $v_{i1}(t_n)$, respectively.

First, by comparing eq. (13) and eq. (16), we find that we can implement eq. (13) with the circuit in Fig. 1 by setting $V_o(z) = X(z)$, $V_{i0}(z) = Q_\theta(X(z))$, $V_{i1}(z) = \overline{Q_\theta(X(z))}$, $C_{f0}/C_i = s\beta$, $C_{f1}/C_i = s$, and $C_k/C_i = \beta + 1$.

This leads a SC A/D converter circuit based on the negative β-map shown in Fig. 2 which includes an additional SC circuit to sample the input signal x_{input}, and a quantizer circuit $Q_\theta(\cdot)$ in a feedback loop. The clock waveforms which drive the circuit in Fig. 2 are shown in Fig. 3. In the figure, L is a bit-length for conversion. Moreover, $\phi\mathsf{C}$ samples x_{input}; at the same time, it resets the charge on C_i. Furthermore, $\phi\mathsf{P} = \phi\mathsf{A} \bullet \overline{\phi\mathsf{C}}$. In order to sample x_{input} according to eq. (7), we set the value of C_s in Fig. 2 as $C_s/C_i = 1$.

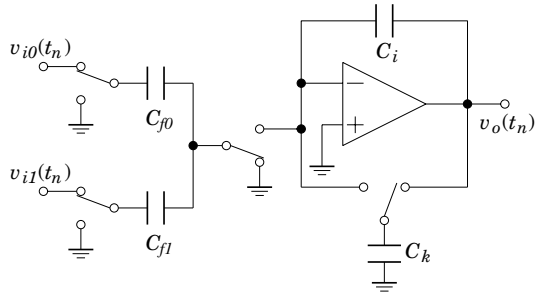

Figure 1: A switched-capacitor damped-integrator.

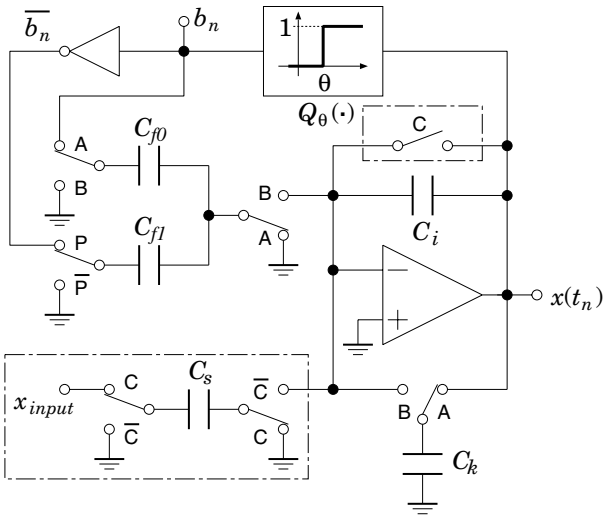

Figure 2: A SC A/D converter circuit based on the negative β-map derived from eq. (13). $\phi\mathsf{P} = \phi\mathsf{A} \bullet \overline{\phi\mathsf{C}}$. The circuit inside the chain-lines is unnecessary for the chaos generator without setting the initial condition. In this case, $\phi\mathsf{P} = \phi\mathsf{A}$.

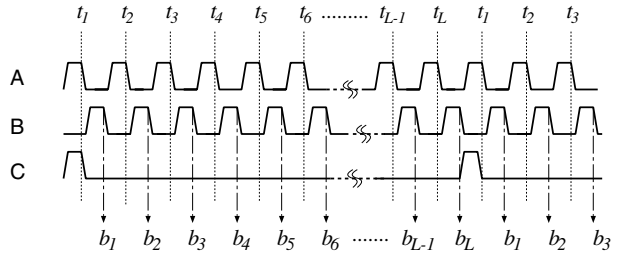

Figure 3: Clock waveforms for the circuit in Fig. 2 and Fig. 4. The output bit-sequence b_n is sampled at the falling edge of $\phi\mathsf{B}$, i.e., at $t_{n+1/2}$.

Second, we propose another SC circuit implementation of the A/D converter based on the negative β-map according to eq. (15). Comparison between eq. (15) and eq. (16) shows that we can implement eq. (15) with the SC integrator shown in Fig. 1 by setting $V_o(z) = X(z)$, $V_{i0}(z) = Q_\theta(X(z))$, $V_{i1}(z) = 1$, $C_{f0}/C_i = s(\beta - 1)$, $C_{f1}/C_i = s$, and $C_k/C_i = \beta + 1$.

The final circuit including a SC circuitry C_s to sample x_{input}, and a quantizer $Q_\theta(\cdot)$ is shown in Fig. 4. In the figure, $C_s/C_i = 1$, and $V_U = 1$ V. The clock waveforms for Fig. 4 are the same as those in Fig. 3. Moreover, $\phi\mathsf{P} = \phi\mathsf{A} \bullet \overline{\phi\mathsf{C}}$.

4.1. Application to a Chaos Generator

Chaos generator circuits with a uniform invariant measure distribution have been proposed based on, e.g., the Bernoulli-map and the tent-map . However, most of those circuits are unstable when their trajectories approach to both ends of the domain of the maps. In contrast, the chaos generator based on the negative β-map proposed in this subsection is stable because the negative β-map is eventually locally onto, so that the trajectories of the map remains in a finite invariant subinterval smaller than the domain of the map.

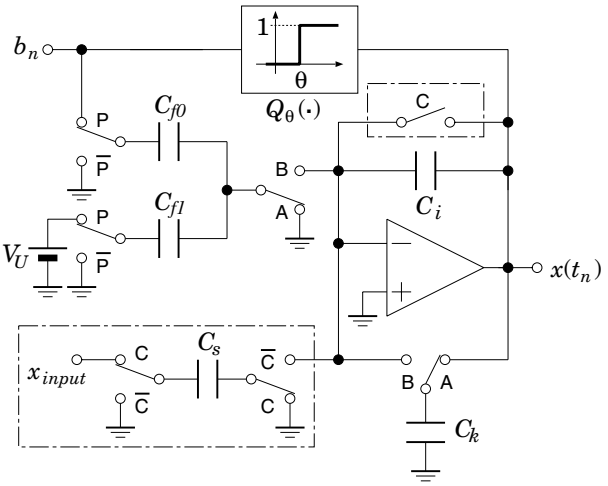

Figure 4: Another SC circuit implementation of the A/D converter based on the negative β-map using eq. (15). $\phi\mathsf{P} = \phi\mathsf{A} \bullet \overline{\phi\mathsf{C}}$. The circuit inside the chain-lines can be omitted for the chaos generator without need for setting the initial condition. In this case, $\phi\mathsf{P} = \phi\mathsf{A}$.

The A/D converter circuits in Figs. 2 and 4 can be directly used as chaos generators by setting their bit-length infinity ($L = \infty$) by making $\phi\mathsf{C}$ a mono-pulse. Moreover, if no setting for the initial condition is needed, the SC circuits for input sampling enclosed by the chain-lines in Figs. 2 and 4, and the clock $\phi\mathsf{C}$ can be omitted to make the circuits compact.

5. SPICE Simulations

In order to confirm the feasibility of the proposed circuits, we simulate the circuits with ideal circuit elements. Although both circuits in Figs. 2 and 4 were simulated and confirmed, the results from the circuit in Fig. 4 are shown in this paper for want of space. Moreover, we assume that the value of β is known, because the object of simulations is to confirm the circuit operations under ideal conditions. In the following simulations, we use $\beta = 5/3$, and $s = 3$.

We simply compare the bit-sequences $BS_L(x_{input})$ from the circuit simulations and those obtained from theoretical calculations in the first simulation. Table 1 shows the comparison for different values of x_{input} where $L = 8$. From the table, we can confirm that the proposed A/D converter circuit properly converts the input signals to corresponding bit-sequences.

Next, we evaluate the conversion errors obtained from the SPICE simulations. With the bit-length of L, the bound for the conversion errors is given by $\epsilon_L(x) = |x_{input} - \widehat{x}_L| \leq s\gamma^L/2$, where $\widehat{x}_L$ is a decoded value from $BS_L(x_{input})$ [3, 4]. From this equation, we select $L = 13$ for $\epsilon_L(x) \leq 2^{-9}$.

The conversion errors for different input values x_{input} are shown in Fig. 5. In the figure, the quantizer threshold θ is a parameter. On the other hand, the conversion errors when we swept θ are shown in Fig. 6 for different values of x_{input}. From these figures, we can conclude that the proposed circuit properly operates with the specified conversion accuracy even if the quantizer threshold changes. That is, we

Table 1: Comparison between the output sequences obtained from the SPICE simulations of the circuit in Fig. 4 and theoretical calculations for $L = 8$.

Input	Threshold	Output Bit-Sequences $BS_L(x_{input})$		
x_{input}	θ	SPICE	Theory	Error
0.2	1.21	01011101	01011101	0
	1.5	01011100	01011100	0
	1.79	01010010	01010010	0
0.5	1.21	01110111	01110111	0
	1.5	01001111	01001111	0
	1.79	01001111	01001111	0
0.8	1.21	01111010	01111010	0
	1.5	01100110	01100110	0
	1.79	00010100	00010100	0

have confirmed robustness of the proposed circuit against the fluctuation of θ, which is one of the advantages of the A/D converter based on the negative β-map.

Finally, we set $L = \infty$ in the A/D converter circuit of Fig. 4 to realize a chaos generator. Figure 7 shows an example of the chaos attractor from the circuit with $\theta = 1.5$. The invariant subinterval of the map in this case is [LB $= s - \nu =$ 0.5, UB $= \beta s - \nu = 2.5$) [3, 4] while the domain of the map is [0, 3]. As shown in the figure, the chaotic trajectory is confined in the invariant subinterval, which guarantees stable behavior of the circuit.

6. Conclusions

We have proposed the design methods for constructing the A/D converter based on the negative β-map using the discrete-time damped-integrator. The proposed methods are suitable to implement the A/D converter in ICs because the discrete-time integrator is a preferred circuit element in ICs. In addition, we have proposed, as an illustration, two SC circuit examples for the A/D converter based on the negative β-map. Moreover, we have applied the proposed A/D converter to the chaos generator by simply making the conversion bit-length $L = \infty$. Because the trajectories of the negative β-map is confined in the invariant subinterval, the resulting chaos generator is robust against circuit non-idealities and noise. Finally, we have confirmed the proposed methods and circuits through SPICE simulations with ideal circuit elements.

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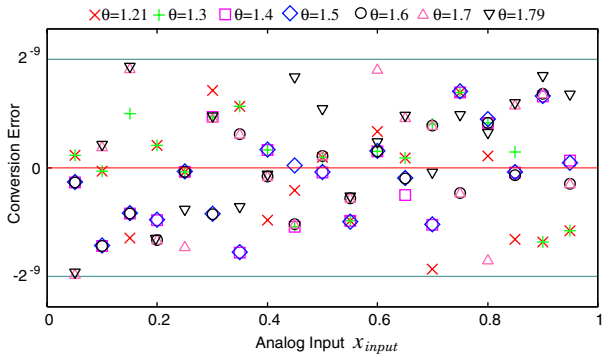

Figure 5: The conversion errors for different values of the quantization threshold θ when the input x_{input} is swept in the circuit of Fig. 4.

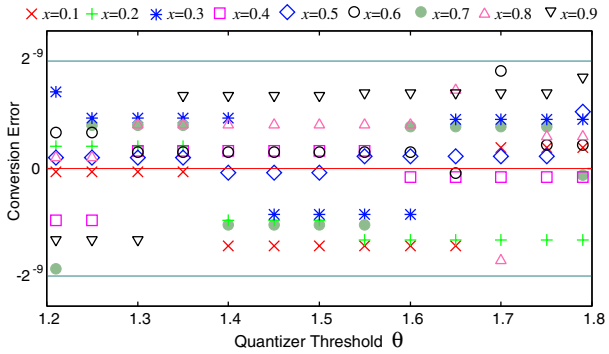

Figure 6: The conversion errors when the quantizer threshold θ is swept for different values of the input x_{input}.

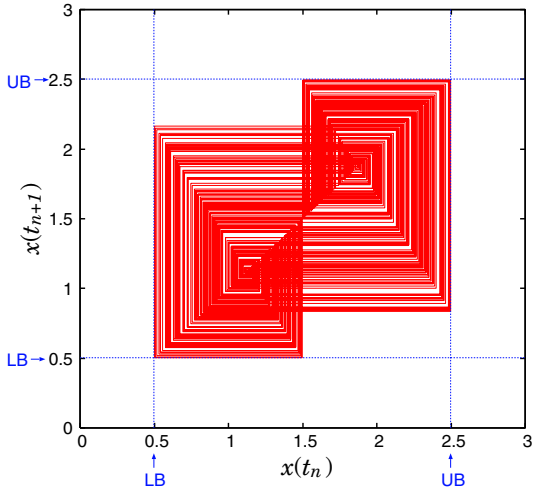

Figure 7: An example of the chaotic attractor obtained from the circuit in Fig. 4 with $L = \infty$ and $\theta = 1.5$. 500 points in the steady-state are plotted. The lower bound LB and upper bound UB for the invariant subinterval are 0.5 and =2.5, respectively, in this case [3, 4].

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