On the Nonidealities of a Tunable CMOS Transconductor

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Abstract — **In this communications we present characteristics and simulation results for a tunable fully differential CMOS transconductor (OTA) designed in an AMS 0.18µm CMOS technology following an architecture recently proposed by Tien-Yu Lo et al. The investigations envisaged the OTA behavior with respect to the amplitude and frequency of the input signal as well, as to the load.**

Keywords—CMOS, transconductor, nonlinearity, frequency response.

I. INTRODUCTION

The use of OTA's in integrated circuits design has no need to be emphasized. Moreover, electrically tunable OTA's have various applications as versatile building blocks for filters [1,2], oscillators [3], analog master-slave circuits etc. A recent OTA application in a channel selection filter for multi-mode direct-conversion radio receivers is presented in [1] with an implementation in TSMC 0.18µm technology.

The basic building block in the above mentioned work is a large range tunable fully differential OTA based on a translinear loop. The authors show that the use of differential OTA's significantly improve performances compared to conventional MOSFET-resistor or MOSFET only transconductors. The aim of this communication is to report an independent design of the architecture proposed in [1] for the tunable transconductor optimized with respect to linearity and to study its frequency behavior for large signal operation.

II. PRINCIPLE AND CIRCUIT

A. The principle

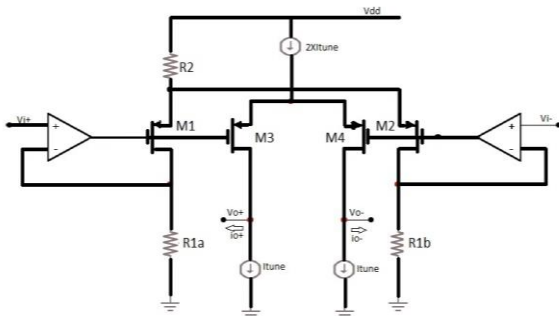The principle used for building the tunable differential OTA is presented in Fig. 1.

Fig. 1. Principle of OTA schematic (adapted from [1]).

The schematic performs two tasks, one to convert the input voltage to current and the other one to make a current multiplication by means of a translinear loop [4]. Roughly, the precision of the voltage to current conversion is thus determined first by the (non)linearity of the voltage to current dependency of the triode biased transistors that will finally replace the resistors R_{1a} and R_{1b} (Fig. 2) and second by the current multiplication errors. Since we do not envisage a rail to rail functionality this offset does not matter significantly. Transistors M1 and M2 work in all cases in weak inversion while M3 and M4 work for small G_m (small current Itune) in weak inversion and for high G_m (high current Itune) in strong inversion, where G_m represent the transconductance of the OTA.
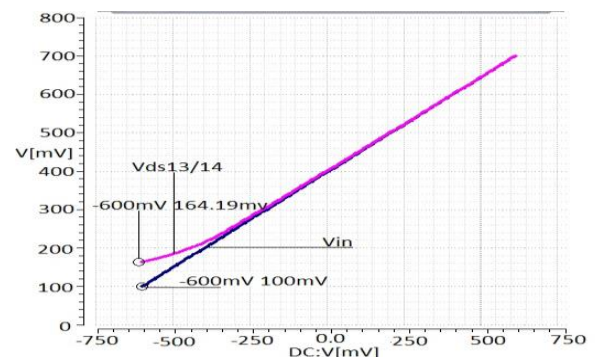

Fig. 2. Ideal and triode transistor based conversion (M13 and M14 in Fig.3) of input voltage to resistor voltage. The maximum error is 64.19 mV .

Both cases are discussed in [1] where it is shown that in the first case the transconductance is proportional to I_{tune} while in the second one, proportional to the square root of I_{tune}.

B. The circuit architecture

In Fig. 3 the schematic of the differential OTA is represented. The circuit has been independently designed following the same architecture as in [1] but in an AMS 0.18µ CMOS technology and all simulations have been done with transistor level current sources as shown in the figure.

III. RESULTS

A. OTA Characteristics

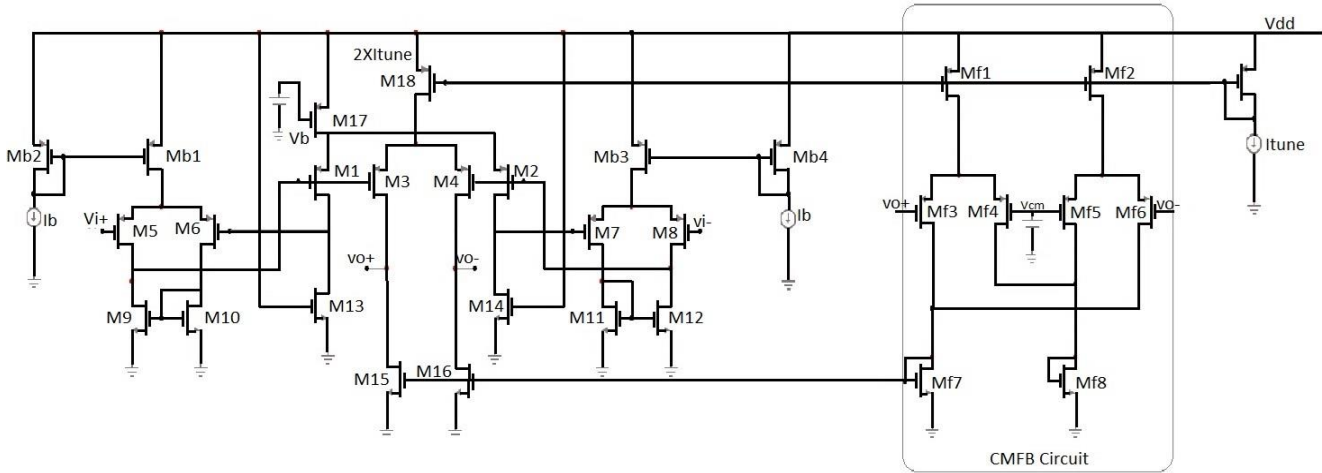The main features of the designed OTA are summarized in Table 1.

Fig. 3. Schematic of the OTA implementation based on [1]

TABLE 1.

Technology	0.18μm
Supply	1.2V
Tuning ratio [G_{m-max} / G_{m-min}]	35
Gm variation[%]	[3.12-109.98μS]
HD3	-52dB
THD@[1Hz-100MHz, Av=500mVpp]	<1%
Power Consumption	0.072 mW @[Itune= 1uA]
	0.44 mW @[Itune=100uA]

The DC characteristics for an input voltage in the range -0.6V to +0.6V, I_{tune} from 1μA to 100 μA and common mode voltage of 0.4V are shown in Fig. 4 where the output current has been plotted. The variation of G_m with the tuning current is shown in Fig. 5.
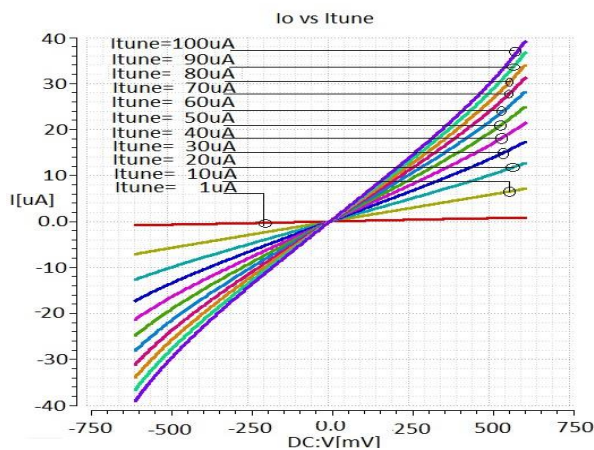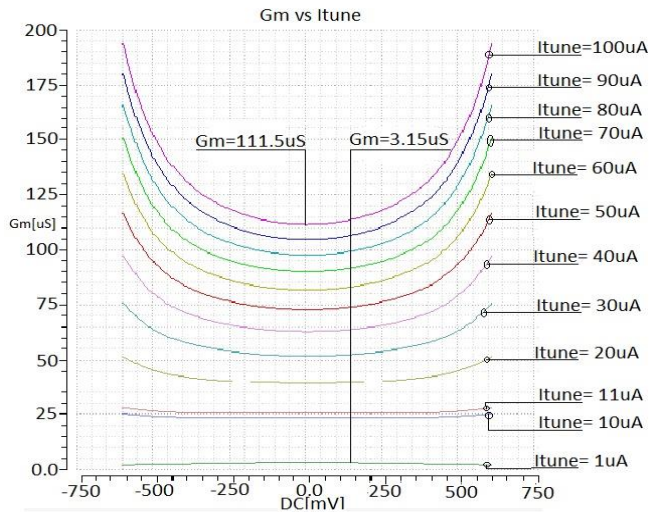

Fig. 5 G_m variation vs I_{tune}.

B. Large Signal Distortion Analysis

A particular aspect investigated in this paper refers to large signal distortion analysis. It well known that distortion is an important aspect related to OTA design [5-8]. In what follows we give more results regarding distortion by plotting the THD dependence both on amplitude and frequency (Figs. 6 and 7) for two values of the resistive load and for two extreme values of the tuning currents.

We consider that this kind of characterization of distortion gives more insight regarding the nonideal behavior of an OTA. The interesting and intriguing aspect of the THD plots is their shape around the frequency of about 20 MHz. Even though it is well known that the AC analysis gives no information related to distortion we have run an AC and a PZ simulation and found a peak in the frequency response due to the pair of complex conjugate poles $p_{1,2}=-3.88511e^7 \pm 5.18053e^7$ with a quality factor Q=0.833.

Fig. 4 Family of DC characteristics for tuning currents in the range 1- 100 μA.

This result leads to the conclusion that the observed shape of the THD can be (partially) explained by the fact that for certain frequencies the third harmonic is "amplified". This hypothesis has been confirmed by two (Periodic Steady State) PSS simulations, (with the same input level) one with a low frequency of 1 MHz and the other one with 20MHz such that its third harmonic is in the range of the AC peak determined by the complex poles. It is apparent that in the second case the third harmonic is more than three times higher explaining the higher THD around the frequency of 20 MHz.
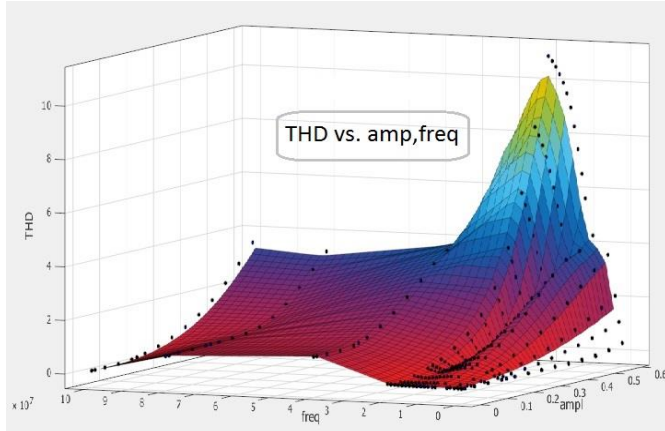

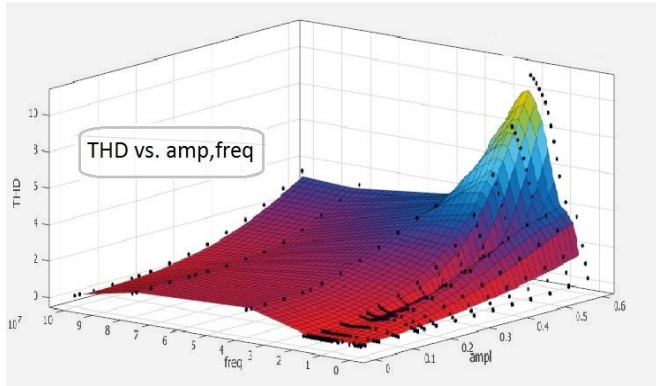Fig.6 THD vs frequency and amplitude   [I_{tune} =1μA, R_l=50 Ω]

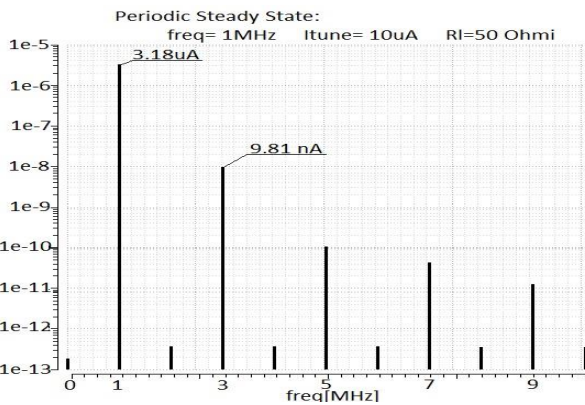Fig.7 THD vs frequency and amplitude [I_{tune}=100μA,R_l=1KΩ]
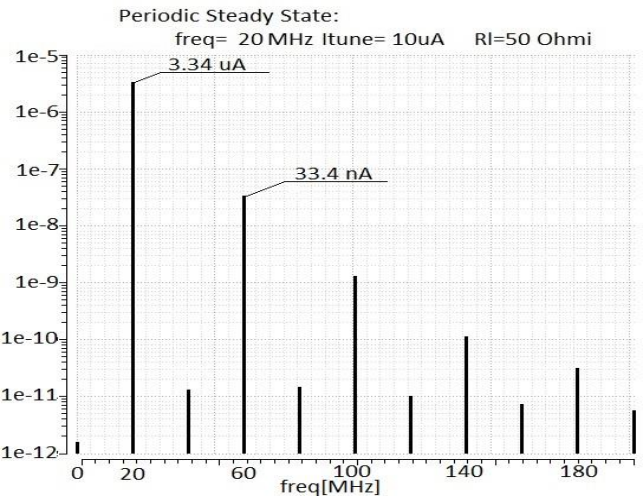

Fig. 8 Output spectrum for I_{tune}=10 μA.

Fig. 9 Output spectrum for I_{tune}=10 μA

Overall, it has been found that for amplitudes less than 0.5$V_{pp}$and frequencies up to 100MHz the THD does not exceed 1%.

IV. CONCLUDING REMARKS

A fully differential tunable OTA has been designed in an AMS 0.18μ CMOS technology and investigated from the point of view of large signal distortion. Besides, the remarkable OTA characteristics, the THD plot vs both amplitude and frequency proves to be a significant tool for describing the nonidealities of the circuit.

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