60 GHz Front-end Components in 130 nm CMOS Technology For Broadband Wireless Communication

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***Abstract*—This paper presents two front-end key components in 130 nm RF CMOS technology for 60 GHz applications: a single balanced mixer with high Conversion Gain (CG), reduced Noise Figure (NF) and low power consumption, and an LC cross coupled Voltage Controlled Oscillator (VCO) with very good linearity, considering V_{ctrl}, and very low Phase Noise (PN). In both circuits, are employed custom designed inductors and balun structures in order to enhance their performance. The inductor achieves an inductance of 198 pH and a quality factor (Q) of 30, at 30 GHz, and the balun shows less than 1° and less than 0.2 dB phase and amplitude imbalance, respectively, from 57 to 66 GHz. The mixer shows a conversion gain greater than 15 dB and a noise figure lower than 12 dB. In addition, the VCO achieves a phase noise lower than -106 dBc/Hz at 1MHz offset, and shows great linearity for the entire band. Both circuits are biased with a 1.2 V supply voltage and the total power consumption is about 10.6 mW for the mixer and 10.92 mW for the VCO.**

Keywords—60 GHz Band; RF CMOS; Millimeter-Wave; Down-Conversion Mixer; Integrated Balun; VCO; Cross Coupled; Coplanar Waveguide; CPW;

I. INTRODUCTION

The last few years, there is a large commercial interest in using the unlicensed 57 to 66 GHz band for high data rate wireless communication. The available spectrum ranges from 5 to 9 GHz depending the country, and is divided into approximately 2.16 GHz wide four sub-channels as shown in Fig. 1. This wide available spectrum in the 60 GHz band around the world, is very promising for many applications, such as: (a) Wireless Personal and Local Area Networks (WPAN/WLAN) [1], (b) replacement of High-Definition Multimedia Interface (HDMI) from point-to-point streaming video links at 60 GHz [2], (c) Wireless ad-hoc communications e.g. notebook to notebook, notebook to printer, notebook to camera, camera to printer, notebook to TV, tablet to camera, camera to TV etc., (d) Wireless Sensor Networks (WSN) and many other applications.

In all these applications, for both homodyne and heterodyne wireless transceivers architectures, key components of the receiver's system are the Voltage Controlled Oscillator (VCO) and the Down Conversion mixer, Fig. 2. They have a very important purpose: the VCO, as a key component of the frequency synthesized LO, has to provide the appropriate signal in order to be used by the down-conversion mixer for converting a high-frequency input RF signal to a more manageable lower frequency signal. The mixer has to provide enough conversion gain in order to suppress the noise contribution of the following stages, low noise figure (NF) and wide bandwidth. Furthermore, in order to reduce signal distortion, linearity is also a critical parameter. As far as the VCO is concerned, low phase noise (PN), high linearity considering the tuning control voltage and broadband operation are the most critical parameters.

In this paper, we present the designed circuits and simulation results of a single balanced mixer with high conversion gain, low noise figure and low power consumption, and a cross coupled LC Voltage Controlled Oscillator (VCO) at 30 GHz with linear performance and very low phase noise. The performance of both components makes them very promising for 60 GHz applications.

In Section II, is presented the proposed mixer topology along with the simulation results. In Section III, is demonstrated the designed voltage control oscillator and also, the results from simulation. In both cases, comparison results are provided with similar topologies found in literature.

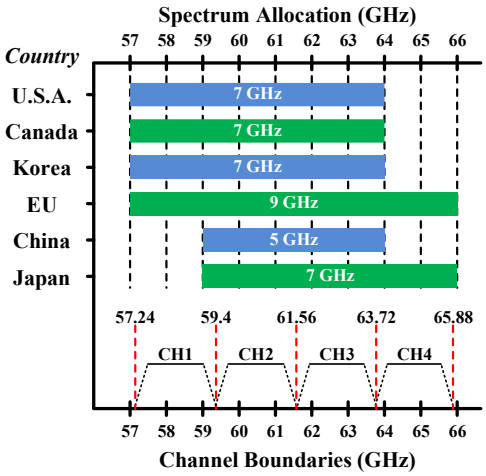


Fig. 1. International unlicensed spectrum for the 60 GHz band.

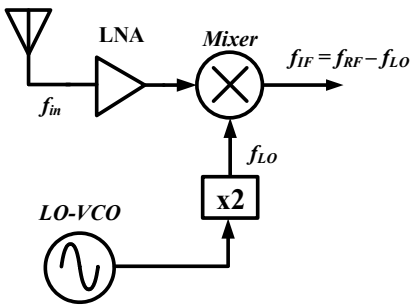
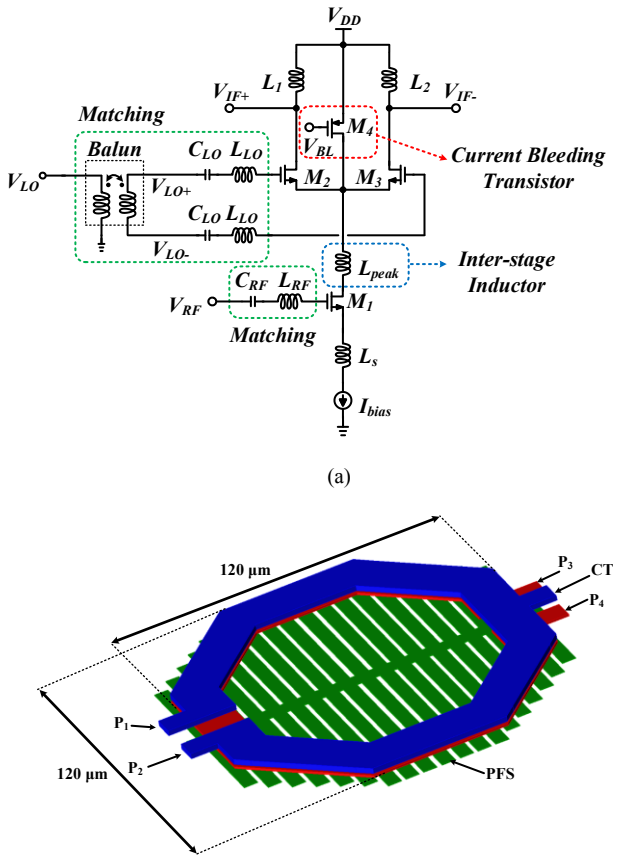


Fig. 2. Typical receiver architecture.

II. Down-Conversion Mixer

A. Proposed Single-Balanced Mixer topology

The proposed single-balanced mixer is illustrated in Fig. 3, along with the integrated transformer type balun. The mixer topology consists of a typical single-balanced mixer, where the transistor M_1 implement the transconductance stage and the transistors M_2-M_3 implement the switching stage. The inductors L_1 and L_2 are used instead of resistors for gain and linearity purposes since an increase in resistance results in a decrease in the voltage headroom at the output node. The inductive load (L_1 and L_2) and the parasitic capacitances of M_3-M_6 form two resonating tanks at the desired IF frequency. The inductors and capacitors at the differential RF and LO ports along with the source degeneration inductors L_s, are used for matching purposes. The circuit is biased using a current source implemented by a current mirror, which controls the current that flows through the transconductance transistor M_1.



(a)

(b)

Fig. 3. (a) Proposed 60 GHz single-balanced down-conversion mixer and (b) integrated passive balun structure.

Considering that in millimeter-wave applications, even the smallest parasitic capacitance can significantly deteriorate the performance of the circuit, an inter-stage inductor, L_{peak}, is used in order to compensate these parasitic capacitances. This leads to significant increase of the conversion gain. If we wanted to succeed a similar gain without using this technique, extremely large bias current need to be used. This technique also improves the mixer's linearity.

In addition, in order to further improve the conversion gain of the mixer, the current bleeding technique is implemented by the PMOS transistor M_4. The value of the control voltage V_{BL} sets the PMOS transistor M_4, ON or OFF, which allows us to control the current flowing through the switching stage. The current bleeding technique is widely used in integrated mixer optimization because it can improve conversion gain and noise figure, simultaneously. The basic characteristic of this technique is that different currents flow through the transconductance stage and the switching stage. The transconductance stage transistor M_1, may consume strong current in order to increase gain and linearity, while the switching stage transistors M_2-M_3 demand less current in order to accomplish an instantaneous switching action. Instantaneous switching action leads to a minimum time decrement in which all of the switching transistors are on. As a result, noise contribution of the switching stage at the mixer output decreases, while at the same time gain performance significantly improves.

B. Integrated Transformer Balun Structure

Due to the differential switching stage of the down-conversion mixer, a passive transformer-type balun was designed in a stacked structure as shown in Fig. 3(b). The balun is used to provide single to differential conversion at the LO input of the mixer. In millimeter-wave frequencies the balun occupies a relatively small area (120×120 µm^2) and is implemented in the top two metal layers. Also, a patterned floating shield (PFS) using a lower metal layer, was used in order to improve the performance of the balun [9]-[10]. Metal width, number of turns and sizing were all optimized to provide low insertion loss, minimum phase and amplitude imbalances, through Electromagnetic Simulations (EM) by using the ADS Momentum. The designed balun structure has an amplitude imbalance lower than 0.2 dB and a phase imbalance less than 1° for the entire band of interest.

C. Simulation Results

The proposed single-balanced down-conversion mixer topology was designed in 130 nm CMOS technology which provides 8-metal layers with the design environment of Cadence software. A simple matching was performed at RF and LO ports for the entire band around 60 GHz, and the results of the S-parameter simulations considering the return losses at these ports are shown in Fig. 4.

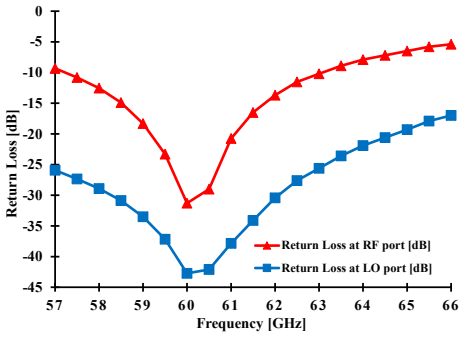


Fig. 4. Return loss at RF and LO port.

The mixer is biased from a 1.2 V supply voltage. The RF and LO signals were set to -30 dBm and 0 dBm, respectively, for maximum conversion gain and minimum NF. Using an RF signal at 60.48 GHz and an LO signal at 55.48 GHz, the down-converted IF signal is at 5 GHz. The simulation results show that, the proposed mixer achieves an approximately 16 dB conversion gain while the NF is maintained below 12 dB. With the inter-stage inductors and the current bleeding technique the conversion gain increased more than 8.5 dB and the NF was suppressed more than 8 dB.

Regarding linearity performance, the mixer simulations results showed a 1dB-Compression Point (CP1dB) of -10 dBm and a 1 dBm IIP3 for a 55.48 GHz LO signal. Deactivating the current-bleeding transistor, by the V_{BL} voltage value, the CP1dB is about -3.04 dBm and the IIP3 around 7.2 dBm.

Simulation results of the mixer's channel selection by LO tuning are shown in Fig. 5. The LO frequency is selected at four frequencies of 53.32 GHz, 55.48 GHz, 57.64 GHz and 59.8 GHz. With the IF at 5 GHz, the corresponding RF input frequencies for channels 1 to 4, are: 58.33 GHz, 60.48 GHz, 62.64 GHz and 64.8 GHz. The conversion gain and the NF of each channel are depicted in Fig. 5. The overall performance of the presented single-balanced down-conversion mixer is compared with a similar state-of-art mixer topology in recent literature [6], in Table I.

In Table I, we can see that the proposed single-balanced mixer achieves much higher conversion gain from the one in [6] with a similar NF value. Also, the simulation results considering the linearity parameters, CP1dB and IIP3, verify the improved linearity performance of the proposed mixer when current bleeding is deactivated. In addition, the proposed mixer consumes approximately 6 mW less power than the one proposed in [6].

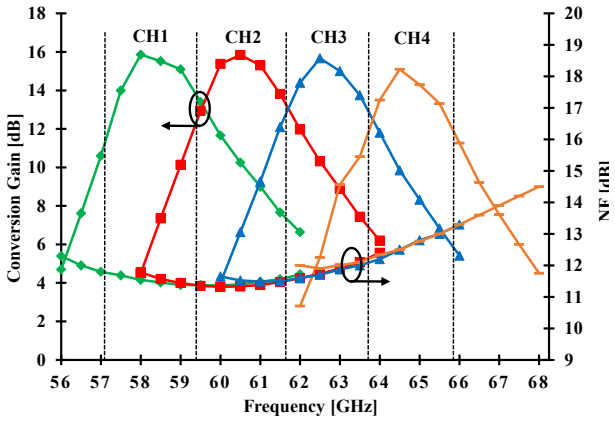


Fig. 5. Mixer channel selection by LO tuning (CG and NF).

TABLE I. SUMMARY AND COMPARISON OF MILLIMETER-WAVE MIXERS AT 60 GHZ

Main Parameters	Reference	
	[6]	**This Work**
Topology	Single-Balanced	**Single-Balanced**
Frequency [GHz]	54-65	**57-66**
Conversion Gain [dB]	9.1	**>15**
NF [dB]	12	**<12**
CP1dB [dBm]	-5	**-3.04***
IIP3 [dBm]	-	**7.2***
Power Consumption [mW]	16.8	**10.6**
Technology	65 nm CMOS	**65 nm CMOS**

**When current bleeding is deactivated.*

III. LC CROSS COUPLED VOLTAGE CONTROLED OSCILLATOR

Voltage controlled oscillators (VCO) are the most critical components of PLL-based local oscillators, because amongst the other components, VCOs are the main contributors of the phase noise of the whole system. This is why the performance of the VCO is a matter of major concern during the system design of a PLL. The VCO described in this paper is an integrated VCO designed in 130 nm technology with operating frequency of 28.46 – 33.62 GHz. In order to obtain simultaneously low phase noise and low power consumption over a wide bandwidth of operation, passive components with low losses are required. For this purpose, a Coplanar Waveguide (CPW) inductor has been designed.

The design is based on the topology of an LC cross coupled oscillator, achieving a bandwidth of about 5 GHz. The phase noise is under -100 dBc/Hz at 1 MHz away from the carrier and consumes approximately 10.92 mW. The resulting negative g_m (LC cross coupled) topology has been chosen for this design because of its simplicity, the circuit's robustness and the resulting low phase noise. An insightful approach to describe such an oscillator, is to consider it as a combination of a parallel LC tank and an active network, which serves as negative resistance to compensate for the energy loss on the tank.

Although modeling and evaluation of a VCO's phase noise is a very complex and challenging issue, Leeson's equation can be used for a rough estimations of the oscillator's single side band phase noise spectrum. The main contributors and the main factors that play significant role in oscillator's phase noise are also described in (1) below:

$$L(f_m) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_0}{2*Q_l*f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FkT}{P_s}\right)\right] \quad (1)$$

Where f_0 is the carrier frequency, Q_l is the loaded Q, f_m is the offset of the carrier frequency, fc is the 1/f corner frequency, F is the noise factor of the amplification process, P_s is the Oscillator's output power, k is Boltzmann's constant and T is the absolute temperature in Kelvin.

Most of the factors which are presented in Leeson's equation express natural constants and the frequency of operation, and therefore, they are not affected by circuit design. On the other hand, quantities like noise factor, output power and loaded Q are parameters that depend on the design of the oscillator and on the technology process used for the design of the oscillator. Especially loaded Q is a parameter of major concern, because it heavily affects the VCO's phase noise and at the same time, depends on both electrical and physical design.

One of the most critical components, considering the quality factor, is the inductor. However, it is very difficult to design a conventional inductor with low losses and high Q at the frequency of 30 GHz. For this design a CPW has been designed in order to obtain a high Q inductor. In Fig. 6, is presented the layout of this inductor. For the implementation of the CPW the top metal of the technology has been chosen in order to obtain the lowest possible losses. Under the inductor a patterned ground shield (PGS) has been placed to isolate the inductor from the substrate's noise. The structure of the shield has been designed seven metal layers below top metal and has been optimized in order to reduce the effect of Eddy Currents. Thus, the structure of the CPW achieves an inductance of 198 pH and a quality factor of 30, at 30 GHz. The implementation of the CPW inductor has been based on Electromagnetic Simulations using Advanced Design System software.

In Fig. 7, a simplified schematic diagram of the circuit is shown. The LC tank consists of the CPW inductor and a varactor, which is responsible for the frequency tuning. Nevertheless, the varactor cannot be used to cover the whole bandwidth of 5 GHz, because this choice would demand a very high gain of the VCO, which would result in degrading the phase noise. For this reason, a solution involving both discrete tuning using banks of capacitors (coarse tuning), and fine tuning with the varactor, is preferable. Following this approach, the bandwidth has been divided in sixteen bands, with every band being controlled by a switch.

Equation (2) shows the dependence of loaded Q on the on-resistance (R_{on}) of the bank of capacitor's switches, focusing again on the phase noise. It is obvious that every switch plays significant role in the overall quality factor and it may lead to phase noise degradation.

$$\frac{1}{Q_{total}} = \frac{1}{Q_L} + \frac{1}{Q_{Var}} + \frac{1}{Q_{BankCap}} \qquad (2)$$

Where $Q_{BankCap}=2*\pi*f*R_{on}*Cu$ and Cu is the capacitance unit value of the bank. Every other capacitance value of the bank of capacitors, is a power-of-two multiple of this unit value C_u. This is an effective way to maintain matching between the circuit's components.

In this design, in order to overcome the above mentioned impact of the switches on Q, four different banks of capacitors and their combinations, based on Boolean logic, have been used to implement the sixteen bands. As a result only four switches are used to control the sixteen frequency bands. Despite the fact that there are only four banks of capacitors, every one of them negatively affects the total quality factor and results in phase noise degradation. For this reason, variability in bias current is implemented by a combination of current switches.

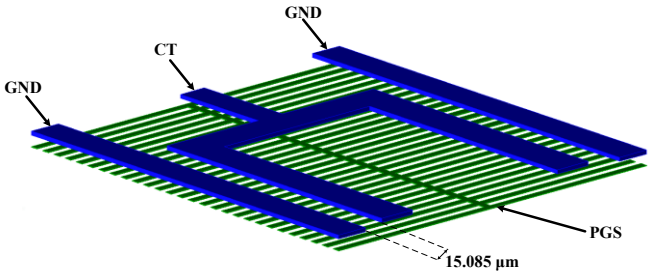


Fig. 6. Coplanar Waveguide Inductor (CPW Inductor).

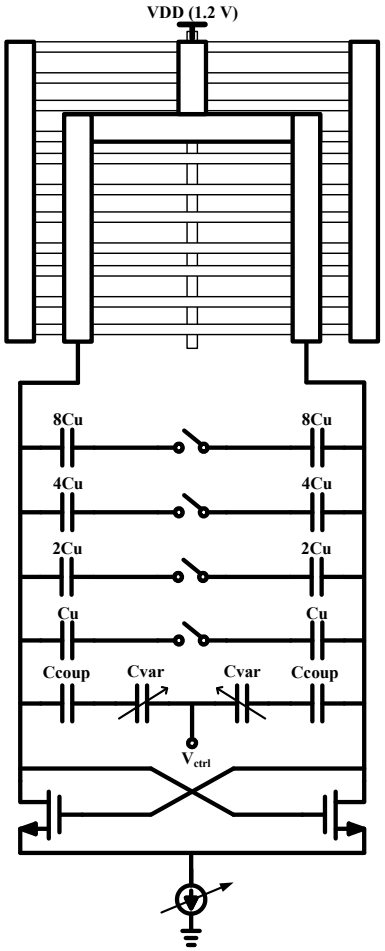


Fig. 7. LC Cross Coupled VCO schematic.

As far as the design of the bands is concerned, they are implemented with the use of capacitors of C= 14 pF. However, the technology doesn't offer capacitors suitable to implement the banks of capacitors. For this purpose, custom capacitors

have been designed in order to meet the specifications of low capacitance and high quality factor. The implementation of the capacitors has been based on Electromagnetic Simulations using Advanced Design System software.

Moreover, oscillator's frequency changes with temperature and bias current variations. These changes are primarily due to the alteration in MOSFET's intrinsic capacitance. Even if the frequency bands are carefully designed, often due to these changes in frequency, blind zones between the bands cannot be avoided. For this reason, in the proposed architecture a band overlap is chosen in order to ensure the undisrupted function of the VCO. As it's been mentioned above, phase noise highly depends on the gain of the VCO. This approach also offers the advantage that, due to the band overlap, for a specific frequency it is possible to use the band where the gain is lower, resulting in lower phase noise.

In Fig. 8 and Fig. 9, the simulations results are presented. Fig.8 shows the frequency bands of operation, where bandwidth coverage and the overlap between the bands are depicted. The phase noise of every band is shown in Fig. 9. It must be noted, that the VCO achieves a phase noise under -100 dBc/Hz at 1 MHz away from the carrier for almost the whole bandwidth of operation.

In Table II, is summarized the overall performance of the proposed VCO and compared with an alternative topology found in literature [7], at the same frequency band. The proposed VCO, achieves much lower phase noise with less power consumption.

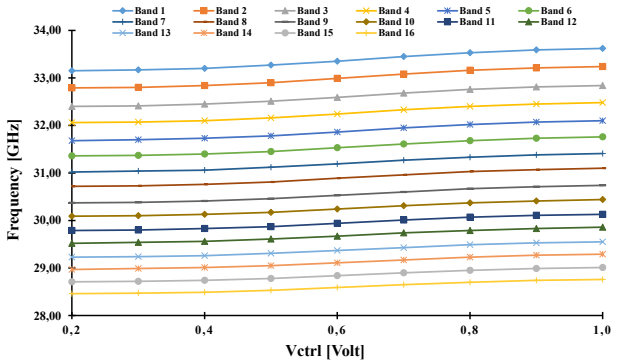


Fig. 8. Frequency Bands.

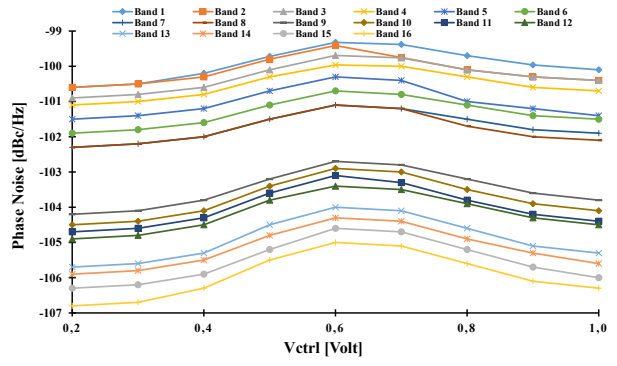


Fig. 9. Phase Noise in all bands.

TABLE II. SUMMARY AND COMPARISON OF MILLIMETER-WAVE VCOS AT 30 GHZ

Main Parameters	Reference	
	[7]	**This Work***
Topology	Differential Colpitts	**Differential LC Cross Coupled**
Frequency [GHz]	30.2-31	**28.46-33.62**
Phase Noise [dBc/Hz] @ 1MHz	-97.5	**-106.8**
Power Supply [V]	2.8	**1.2**
Power Consumption [mW]	16.8	**10.92**
FoM	174.7	**181**
Technology	0.35 μm SiGe BiCMOS	**130 nm CMOS**

**Based on simulation results.*

IV. CONCLUSION

Two very important components of a wireless receiver are presented in this paper: a single-balanced mixer topology and a cross coupled LC Voltage Controlled Oscillator (VCO). The proposed mixer achieves a conversion gain greater than 15 dB and a NF lower than 12 dB. In addition, the simulation results demonstrate that CP1dB and IIP3 is about -3.04 dBm and 7 dBm, respectively, while the mixer's power consumption is about 10.6 mW. The VCO achieves a phase noise under -100 dBc/Hz at 1 MHz offset, over a 5 GHz bandwidth with low power consumption at 30 GHz. Both of the components were designed in 130 nm CMOS technology.

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REFERENCES

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," IEEE Communications Magazine, pp. 140-147, Jan. 2002, pp. 118-121.

[2] A. Niknejad and H. Hashemi, *mm-Wave Silicon Technology: 60 GHz and Beyond*, New York: Springer, 2008.

[3] R. Daniels, R. Heath, "60 GHz wireless communications: emerging requirements and design recommendations," *IEEE Vehicular Technology Magazine*, pp. 41-50, Sep. 2007.

[4] J. Shi, L. Li, T. J. Cui, "A 60-GHz Broadband Gilbert-Cell Down Conversion Mixer in a 65-nm CMOS," in *IEEE Inter. Conf. of Electron Devices and Solid-State Circuits (EDSSC),* Jun. 2013, pp.1-2.

[5] J.-H. Tsai et al,"A 25–75-GHz broadband Gilbert-cell mixer using 90-nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 4, pp. 247–249, Apr. 2007.

[6] Kraemer. M, Ercoli. M, Dragomirescu. D and Plana. R, "A wideband single-balanced down-mixer for the 60 GHz band in 65 nm CMOS". In *Proceedings of Asia-Pacific Microwave Conference*, Dec. 2010, pp. 1849-1852.

[7] M. Hon, Y. Chen, K. Moothaan, "Design Considerations for a 30 GHz Differential Colpitts VCO with High f_{osc}/ f_T ration in 0.35 SiGe BiCMOS", in Asia Pacific Microwave Conference (APMC), pp 1573-1576, Dec. 2009.

[8] K. Giannakidis, S. Sgourenas, A. Kanteres, K. Moustakas, G. Kalivas, S. Siskos,"A 17.5-22.5 GHz Fractional–N Wideband Frequency Synthesizer in 65 nm CMOS Technology", in Proceedings of European Microwave Integrated Circuits Conference, Oct. 2016, London.