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A Novel Capacitive-to-Digital Converter Interface Based on MemCapacitors for MEMS Capacitive Sensing Applications

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***Abstract*—This paper proposes a new 10-bit fully differential capacitance-to-digital converter (CDC) used in MEMS capacitive sensing applications based on memcapacitors. The proposed digital interface circuit is the voltage based-CDC technique; this achieves a direct physical property (capacitance) conversion into a digital output. The overall proposed design eliminates repeated blocks and can be used independent of the sensor type. The proposed architecture enhances the CDC performance and realizes minimized area due to memcapacitors. A performance comparison between conventional capacitor-based circuit and the circuit using memcapacitors is presented which indicates the same behavior but with an overall huge area reduction and enhanced power consumption. Cadence and LT-SPICE simulations are done using 90nm model with 1V single ended voltage supply. The current consumption at 1 KHz is 5.9 µA.**

***Index Terms*—Analog-to-digital converter (ADC), Capacitance-to-digital converter (CDC), MEMS, Memcapacitors.**

I. Introduction

Successive approximation register (SAR) analog-to-digital converter(ADC) architectures have become the most popular technology for analog/digital conversion interface for all digital signal processing systems [1]. The goal is to acquire the sensed signal with low-power and miniaturized electronic device. Consequently, a numerous number of applications ranging from biomedical, gyroscopes and direction detection to power management applications are in continuous search for low power and low area ADCs for interface conversion purposes [2].

Recently, researchers are targeting the integration of the sensor and the electronic interface circuit together with the least possible area and least power consumption. Capacitive sensing is emerging as a popular interfacing alternative to switches and knobs in different customer electronic devices. It is simply based on the idea of sensing the capacitance electrical property that exists between any two conductive surfaces. Whereas this electric property varies due to the change in a physical property such as: pressure, temperature, position, speed and many other physical properties. There is a variety of capacitive readout circuits and techniques known as capacitance-to-digital converter (CDC) techniques[3-4]. There are methods including time-based capacitance to digital [5], frequency-based capacitance to digital[6]and voltage-based capacitance to digital converters[7-8]. The most attractive method in terms of power consumption, accuracy and reliability is the voltage-based CDC technique [7-8]. Where the sensed capacitance value is transformed into a digitalized related voltage output. One of the famous CDC architectures is the one proposed by K.Tanaka*et al.* [7], where a low power single capacitance to digital converter was realized, however, the circuit could not operate at high variation of sensor capacitance frequency. This is due to the dependency of DC level on variation frequency of sensor capacitance. Later in [8] a differential CDC was realized that eliminatedthe influence of variation of sensor capacitance to the circuit DC level at the output of the capacitor arrays. This can be used further in applications where the sensor value is varied with frequency variations. This differential CDC approach was then reported in variety of applications such as Multisensory systems [9].

In this work, a10-bit fully differential low-power and minimized area capacitance-to-digital converter (CDC) is proposed. This CDC interface circuit is realized using memcapacitors, where the memcapacitor (MemC) behavior and performance characteristics are first studied, and then further the effect of using the memcapacitors is compared with other previous different techniques. The proposed technique can be utilized as a common IC block used after different MEMS sensors to achieve low area and low power on-chip interface system.

The paper is organized as follows: Section II briefly explains the memcapcitor history and theory of operation, followed by the CDC architecture using conventional integrated capacitors in section III. Section IV presents the proposed CDC circuit based on Memcapacitors. Simulation results and comparisons with previous work are included in section V. Finally, the conclusion is stated in section VI.

II. MEMCAPACITOR TECHNOLOGY

A. Introduction

The memory-resistor (known as memristor) was first postulated by Chau in 1971 [10].It remained a postulated idea until HP published the first memristor implementation in 2008 [11].Later in January 2009 the general idea of memory circuit elements was proposed including memcapacitive and meminductive systems as well as their subsystems defined as memcapacitors and meminductors. It would operate in contrast to the memristor, as non-volatile memories with essentially lossless data reading and storing [12].

Memcapacitive system or a memcapacitor can be defined as a passive element whose capacitance is controlled by the amount of electric charge conveyed through it [12]. This charge affects the width of the dielectric. The memcapacitor circuit symbol is shown in Fig.1.

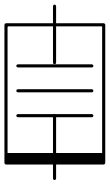

Fig. 1 Memcapacitor Circuit Symbol [12].

There are two types of memcapacitive systems: voltage-controlled and charge controlled systems [13]. According to [12], the charge controlled memcapacitor can be defined from equations (1) and (2), where $q\,(t)$ is the capacitor charge at time t, $V_C(t)$ is the corresponding voltage, $C^{-1}$is the inverse memcapacitance that depends on the system internal state, and $\dot{x}$ is the dynamic vector that represents the system internal state variable.

$$V_C(t) = C^{-1} * (x, q, t) * q(t) \quad (1)$$

$$\dot{x} = f(x, q, t) \quad (2)$$

Since the above element has gained a great focus in many research areas and fields, a lot of publications and researches were conducted to study the memcapacitor behavior and model it. So, simulation set up was implemented using a SPICE simulation model for the charge-controlled memcapacitor [14]. In these simulations, the memcapacitance value depends on the electric charge that passes through the memcapacitor and its state equation. The state variable x depends on the change of dielectric width L that can vary from L_{min} to L_{max}which correspondingly sets a limit range for both minimum and maximum memcapacitances and inverse memcapacitances as shown in equation (3):

$$x = \frac{L - L_{min}}{L_{max} - L_{min}} \in (0,1) \quad (3)$$

The memcapacitor volt-coulomb pinched hysteresis loop profile is shown in Fig.2. The memcapacitor has the following parameters:C_{min}=10nF, C_{max}=10uF, C_{int}=100nF and driven under 2V-amplitude sinusoidal wave with frequency 1KHz. This is similar to the hysteresis behavior of memristive elements illustrated in [15].

III. CDC CIRCUIT ARCHITECTURE

A. Circuit Overview

The fully differential CDC circuit is shown in Fig.3. It is composed of a MEMS capacitive sensor C_x, two exact binary weighed capacitor arrays (to eliminate the effect of MEMS capacitive sensor variation or fluctuations to output DC level),a scaling capacitor C_s , a low-voltage comparator, switches and a SAR control logic to generate the final digital code that corresponds to the sensor capacitance value.

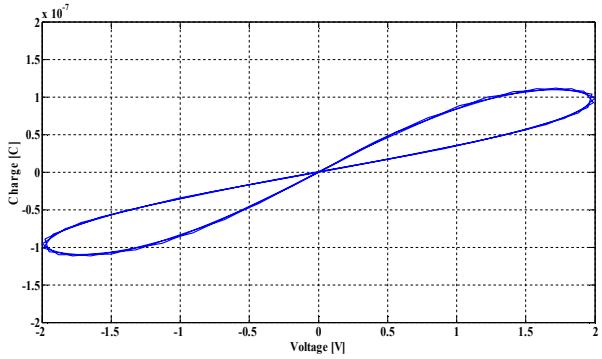

Fig. 2The Characteristic Curve of Memcapacitor.

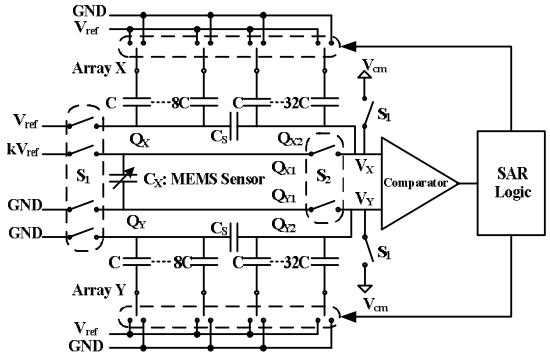

Fig. 3 Conventional CDC Circuit Architecture.

B. Operation of the Differential CDC

The CDC has two modes of operation: the sampling mode and the conversion mode; where both are based on a binary search algorithm and charge redistribution architecture.

In the first phase, switch S_1 is turned on; switch S_2 is turned off and switches of bottom plates of capacitor arrays X and Y are connected to $V_{ref}$and ground, respectively.

In the second phase, switch S_1 is turned off and switch S_2 is turned on. The conversion mode begins with the most significant bit conversion (MSB).First, the MSB switch of capacitor array X is connected to ground and all other switches in the array remain connected to V_{ref}. Whereas in array Y, all switches are connected opposite to array X. Due to the charge redistribution and the law of charge conservation in both capacitor arrays X and Y, the voltage at the input nodes of the comparator is:

$$|V_X - V_Y| = 2 * \frac{C_{MSB} - kC_X}{2C_X + C_{UPPER} + \frac{C_S C_{LOWER}}{C_S + C_{LOWER}}} * V_{REF} \quad (4)$$

Where C_{MSB} is the MSB capacitance, C_{UPPER} is the total capacitance of the upper bits capacitor array at the right side of the scaling capacitor C_S, k is a scaling factor and $C_{LOWER}$is the total capacitance of the lower bits capacitor array at the left side of the scaling capacitor C_S. The voltages V_X and V_Y are compared mutually and the comparator output determines which input voltage is at

higher level. Accordingly comparing voltages V_X and $V_Y$means comparing C_{MSB} and kC_X .If C_{MSB} is smaller thankC_X, the MSB is kept "1"and the MSB switch of array X and Y is kept connected to $V_{ref}$and ground, respectively. Else, the MSB switch is set to "0" and the MSB switch of array X and Y is reset to ground and V_{ref}respectively. When the conversion of MSB is finished, conversions of the next bits are carried out one by one in the same process described until the least significant bit (LSB), to reach a differential voltage approaching0. Finally, the output digital code indicates the most nearest approximated value of the capacitive sensor value.

IV. CDC CIRCUIT USING MEMCAPACITORS

In this paper, the CDC circuit is realized replacing the binary weighted conventional integrated capacitors by memcapacitors. The study started by replacing one capacitor in each array at a time to study the effect of the memcapacitor on the response of the CDC circuit. The memcapacitor model used is the SPICE model indicated in [14]. To replace a normal integrated capacitor by a memcapacitor, the value of the memcapacitor is determined by fixing both values C_{min} and C_{int} and only changing the value of C_{max} .

Fig.4 shows the CDC architecture after replacing all conventional capacitors by memcapacitors.

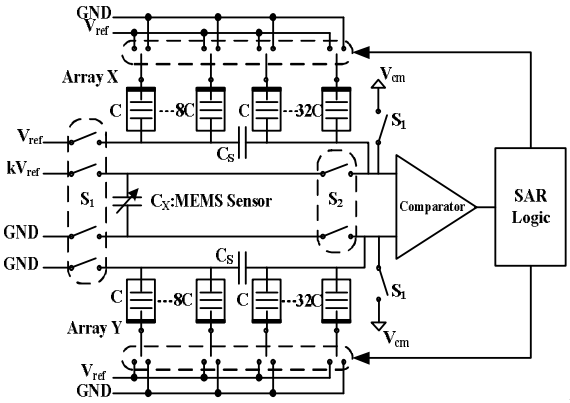

Fig. 4 CDC Circuit using Memcapacitors.

V. SIMULATION RESULTS

Simulations are done using CADENCE and LT-SPICE tools, where the MEMS sensor capacitance value is varied in the range of pF. The comparator used is realized in CMOS architecture using 90 nm transistor model. The MEMS capacitive pressure sensor is first studied and simulated using COMSOL multi-physics tool to study its behavior, and then the variation in the sensor's capacitance is modeled in CADENCE and LT-SPICE tools.

Fig.5 shows the simulation results of the CMOS comparator input voltages V_X and $V_Y$first using conventional integrated capacitors setting the capacitance sensor value to 3pF, the conversion frequency was around 10KHz. Simulation result shows that these two voltages are symmetric around the common voltage V_{cm}=0.5v which is the output of the capacitor arrays.

Also, Fig.5shows the output voltages at the capacitor arrays, after replacing the conventional integrated capacitors with memcapacitors. The simulation results show that the CMOS comparator input voltages are symmetric too around V_{cm}=0.5v.

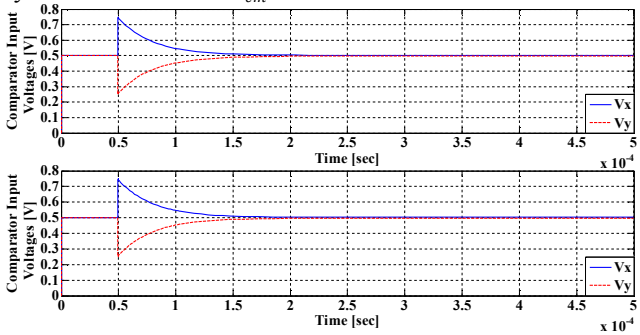

Fig. 5 CDC Comparator Input Voltages using Conventional Integrated Capacitors and Memcapacitors.

The results show that the CDC circuit performance using memcapacitors and conventional integrated capacitors are almost the same, yet the use of memcapacitors greatly reduces the design area.

Fig.6 shows the conversion results of the MEMS capacitive pressure sensor using the proposed memcapacitor based CDC architecture. In which the capacitance of the MEMS sensor is varied in the pF range and the digital output code is converted into its decimal equivalent.

In[16], a memristor was realized using a TiO_2 thin film sandwiched between two metal plates where the total area of this model was measured to be in the range of (500 $nm^2$to 2500 nm^2). In[17], a memcapacitor realization was presented where a memcapacitor can also be fabricated using a TiO_2 thin film sandwiched between two metal plates which is similar to the approach used for the memristor presented in[16].As a result, a memcapacitor area can be estimated to be in the nm^2 range ($10^{-18}m^2$).So unlike the conventional capacitor where the MOSFET realization depends on C_{OX} of the MOSFET[18]as shown in the equations below:

$$C_{eff} = C_{OX} * W * L + 2 * C_{ol} * W (5)$$

The smallest value for the capacitor used in this paper is 1 pF that requires an area of 81.1 $\mu m^2$for 90nm CMOS technology, which is highly greater than the area of memcapacitor. Table 1shows the area values of the conventional integrated capacitors with different values of capacitance compared to the estimated area of the memcapacitor as indicated in [17]. The value of thememcapacitor depends on the biasing as shown earlier in the memcapacitor section; therefore the memcapacitor area is fixed regardless of its value as shown in Table 1.

Finally, Table 1 clearly shows the great area reduction due to replacing the conventional integrated capacitors with memcapacitors. This massive area reduction is a very attractive feature for different applications including biomedical applications where the area is the main factor in implanted devices.

An overall performance comparison between the proposed CDC architecture and previous architectures is presented in Table 2.

TABLE I
MEMCAPACITORS AND CONVENTIONAL INTEGRATED CAPACITORS AREA COMPARISON

Capacitance Value	Conventional Integrated Capacitor Area	Memcapacitor Area
1 pF	81.1 μm^2	($0.0005\mu m^2$ to $0.0025\ \mu m^2$)
2 pF	162.2 μm^2	
4 pF	324.4μm^2	
8 Pf	648.8μm^2	
16 pF	1297.6μm^2	
32 pF	2595.2μm^2	

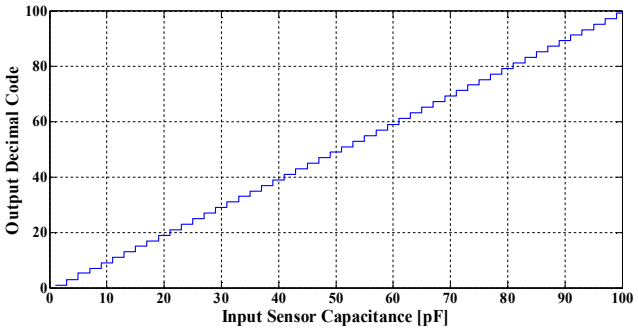

Fig. 6Conversion Results of the proposed Memcapacitor CDC.

TABLE 2
PROPOSED CDC CIRCUIT OVERALL PERFORMANCE COMPARISON

Specifications	Tanaka [7]	Vo [8]	Lai [5]	This Work
Technology	180nm	180nm	180nm	90nm
Power Supply	1.4 V	1.4 V	1.8 V	1 V
Resolution (ENOB)	8 Bit (6.83)	10 Bit	(6.7)	10 Bit (9.3)
Power/Current Consumption	360µA	29.7µA	82µW/45.6 µA	5.9 µA
Area	0.034 mm^2	0.11 mm^2 (estimated)	0.0354 mm^2	$0.0005\mu m^2$ to 0.0025 μm^2 (estimated for each MemC)
Conversion Frequency	262 KHz	262 KHz	125 KHz	10 KHz

VI. CONCLUSION

A new realization for a fully differential 10-bit capacitance-to-digital converter for MEMS capacitive sensors based on memcapacitors was proposed. The conventional integrated capacitors in the capacitor arrays were replaced by memcapacitors. The design was realized in 90nm CMOS technology under 1V single ended voltage supply for different capacitive sensor applications. The realized converter achieved an Effective Number of Bits (ENOB) of 9.3band SNR of 57.75 dB. The use of the memcapacitor instead of the conventional integrated capacitors reduced the overall area of the circuit dramatically, while maintaining a similar response to that of the conventional integrated capacitor. The proposed technique thus achieved the best of both technologies MEMS and Memcapacitors by combining them together. This enhances the digital signal processing circuit when it is integrated in any MEMS capacitive sensor system independent of the number of sensors or their types. Thus, makes it more suitable for biomedical applications, wireless sensor networks and direction detection applications.

VII. REFERENCES

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