2015 International Symposium on Nonlinear Theory and its Applications
NOLTA2015, Kowloon, Hong Kong, China, December 1-4, 2015

Realization of Fractional-Order Capacitor and Inductor Emulators Using Current Feedback Operational Amplifiers

Ilias Dimeas†, Georgia Tsirimokou†, Costas Psychalinos† and Ahmed S. Elwakil‡

†Department of Physics, Electronics Laboratory, University of Patras
GR-26504, Rio, Patras, Greece
‡ Department of Electrical and Computer Engineering, University of Sharjah, College of Engineering
P.O. Box 27272, Sharjah, Emirates
Email: iliasdimeas4@gmail.com, tsirimg@upatras.gr, cpsychal@upatras.gr, elwakil@sharjah.ac.ae

Abstract–Fractional-order capacitor and inductor emulators using Current Feedback Operational Amplifiers as active elements are presented in this paper. Both schemes have been designed by combining fractional-order differentiator or integrator topologies with a voltage-to-current converter. The realization of the fractional-order differentiation and integration blocks is performed through the employment of an integer-order multi-feedback filter topology. An important benefit, from the design flexibility point of view, is that the same topology could be used for emulating both fractional-order capacitor and inductor, and this is achieved through an appropriate selection of the time-constants and gain factors. The behavior of the proposed emulators has been studied through the OrCAD PSpice simulator, using the model of the commercially available AD844 discrete IC component as Current Feedback Operational Amplifier.

1. Introduction

The interdisciplinary nature of the fractional calculus makes it a powerful tool for biological, biochemical, medical, electrical engineering etc. applications. For example, the modeling of viscoelasticity as well as of biological cells and tissues has been performed through the utilization of the fractional-order calculus. Also, fractional-order filters as well as oscillators and control systems have been realized with attractive characteristics, compared with their conventional counterparts [1].

Fractional-order capacitors, known also as Constant Phase Elements (CPEs), and fractional-order inductors (FI) are the most important components for realizing fractional-order circuits. The impedance of a CPE is described by the formula: $Z(s) = 1/\hat{C}s^a$, where the variable a ($0<a<1$) is the order of CPE and $\hat{C}$ is its normalized capacitance, expressed in F/sec^{1-a}. The value (in Farad) of the frequency dependent capacitance (C) of a FOE will be then calculated as: $C = \hat{C}/\omega^{1-a}$. In a similar way, the impedance of a FI is given by the formula: $Z(s) = \hat{L}s^a$, and the relationship between the pseudo-inductance ($\hat{L}$), in H/sec^{1-a}, and the conventional inductance (L), in Henry, is: $L = \hat{L}/\omega^{1-a}$.

Although CPEs have been developed on the basis of electrolytic processes and fractal structures on silicon, the main problem is that these elements are not yet commercially available. Thus, efforts for approximating CPEs include the employment of infinite RC cable, appropriately configured integer-order RC ladder networks have been proposed in the literature. It should be mentioned at this point that this procedure is not easy, from the practical implementation point of view [2]-[5].

The same problem also occurs about the commercial availability in the case of FI. A way for approximating the behavior of a FI is the employment of a Generalized Impedance Converter (GIC), passive elements, and CPEs. But, this solution still suffers from the practical problems related to the approximation of a CPE [6].

In order to overcome the aforementioned drawbacks a novel scheme for emulating CPEs and FIs is presented in this work. This is based on the employment of fractional-order differentiator and integrator configurations and, also, a voltage-to-current (V/I) converter. The realization of the required fractional order differentiation and integration stages is performed using an appropriate integer-order multi-feedback topology. This has been implemented using Current Feedback Operational Amplifiers (CFOAs) as active elements, due to their design flexibility and versatility. An attractive feature of the proposed solution is that the same circuit could be used for emulating both CPE and FI and this is achieved through an appropriate selection of the values of passive elements. The validity of the proposed scheme has been verified through simulation results, using as CFOAs the commercially available AD844 discrete IC components. The paper is organized as follows: the proposed design procedure is given in Section 2, while the derived emulator is introduced in Section 3. The obtained simulation results are given in Section 4.

2. Scheme for Emulating Fractional-Order Elements

The Functional Block Diagrams (FBDs) for emulating CPE and FI are demonstrated in Figs.1a-b, respectively. Performing a routine algebraic analysis it is derived that

the emulated impedances are given by the expressions in (1) and (2), where ω_o is the unity-gain frequency of the differentiator/integrator, related with the time-constant according to the formula: $\omega_o=1/\tau$, and R_{VI} is the equivalent resistance of the *V/I* converter.

$$Z_{eq}=\frac{R_{VI}}{\left(\frac{\omega}{\omega_o}\right)^a} \tag{1}$$

$$Z_{eq}=R_{VI}\cdot\left(\frac{\omega}{\omega_o}\right)^a \tag{2}$$

Thus, the values of the pseudo-capacitance and inductance will be given by (3) and (4)

$$\hat{C}=\frac{1}{R_{VI}\cdot\omega_o^{\,a}} \tag{3}$$

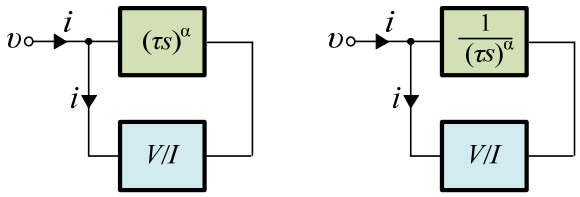
$$\hat{L}=\frac{R_{VI}}{\omega_o^{\,a}} \tag{4}$$

The values of the conventional capacitance and inductance are expressed by (5) and (6), respectively

$$C=\frac{1}{R_{VI}\cdot\omega_o^{a}\cdot\omega^{1-a}} \tag{5}$$

$$L=\frac{R_{VI}}{\omega_o^{a}\cdot\omega^{1-a}} \tag{6}$$

Note that at $\omega=\omega_o$, the expressions in (5)-(6) are simplified as: $C=1/(\omega_o R_{VI})$ and $L=R_{VI}/\omega_o$.



(a) **(b)**

Fig.1: Emulation scheme for a fractional-order **(a)** capacitor, and **(b)** inductor.

The fractional-order differentiator will be approximated by an appropriate integer-order circuitry [7]. For this purpose, the second-order approximation of the Continued Fraction Expansion (CFE) will be employed, due to its efficiency in terms of accuracy and circuit complexity. The transfer function of the differentiator becomes [8]

$$H(s)\cong\frac{\left(\frac{a^2+3a+2}{a^2-3a+2}\right)s^2+\left(\frac{1}{\tau}\cdot\frac{8-2a^2}{a^2-3a+2}\right)s+\frac{1}{\tau^2}}{s^2+\left(\frac{1}{\tau}\cdot\frac{8-2a^2}{a^2-3a+2}\right)s+\frac{1}{\tau^2}\cdot\frac{a^2+3a+2}{a^2-3a+2}} \tag{7}$$

while for the integrator

$$H(s)\cong\frac{\left(\frac{a^2-3a+2}{a^2+3a+2}\right)s^2+\left(\frac{1}{\tau}\cdot\frac{8-2a^2}{a^2+3a+2}\right)s+\frac{1}{\tau^2}}{s^2+\left(\frac{1}{\tau}\cdot\frac{8-2a^2}{a^2+3a+2}\right)s+\frac{1}{\tau^2}\cdot\frac{a^2-3a+2}{a^2+3a+2}} \tag{8}$$

Inspecting (7) and (8) it is readily obtained the similarity of both expressions. As a result, they could be realized by the same core through an appropriate selection of the coefficients values. This is very attractive feature providing design versatility and flexibility.

The well-known Follow-the-Leader Feedback (FLF) structure could be used for realizing (7) and (8). This is shown in Fig.2 and the realized transfer function is

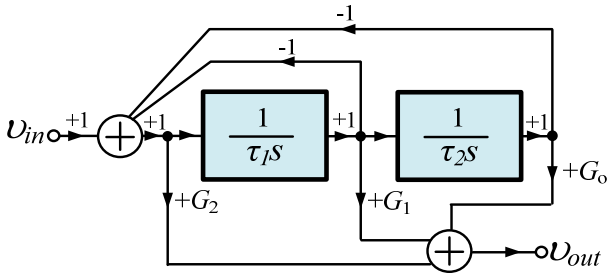


Fig.2: FLF multi-feedback structure for approximating a fractional-order differentiator/integrator.

$$H(s)=\frac{G_2s^2+\frac{G_1}{\tau_1}s+\frac{G_o}{\tau_1\tau_2}}{s^2+\frac{1}{\tau_1}s+\frac{1}{\tau_1\tau_2}} \tag{9}$$

Comparing the coefficients in (7)-(8) with these in (9), the derived design equations of the differentiator and integrator are summarized in Tables 1 and 2, respectively.

TABLE 1
DESIGN EQUATIONS FOR THE DIFFERENTIATOR

τ_1	τ_2	G_2	G_1	G_o
$\tau\cdot\left(\frac{a^2-3a+2}{8-2a^2}\right)$	$\tau\cdot\left(\frac{8-2a^2}{a^2+3a+2}\right)$	$\frac{a^2+3a+2}{a^2-3a+2}$	1	$\frac{a^2-3a+2}{a^2+3a+2}$

TABLE 2
DESIGN EQUATIONS FOR THE INTEGRATOR

τ_1	τ_2	G_2	G_1	G_o
$\tau\cdot\left(\frac{a^2+3a+2}{8-2a^2}\right)$	$\tau\cdot\left(\frac{8-2a^2}{a^2-3a+2}\right)$	$\frac{a^2-3a+2}{a^2+3a+2}$	1	$\frac{a^2+3a+2}{a^2-3a+2}$

3. Realization of Fractional-Order Elements Emulator

The realization of the FBDs in Fig.1 will be performed using CFOAs as active elements. The derived CPE and FI emulator is demonstrated in Fig.3. Inspecting this topology it is easily verified the absence of additional buffers for connecting the intermediate stages. This is originated from the fact that their outputs are derived at the O terminal of CFOAs, which is the output of the internal buffer of the active cell. As a result, they are

capable for direct cascade connection leading to reduction of the active component count in comparison with the corresponding stages where CCIIs are employed. In addition, the required *V/I* converter which provides the appropriate direction of the current is realized using only one CFOA and this is achieved through the availability of the inverted output of the differentiator/integrator, denoted as $-\upsilon_{out}$ in Fig.3. In this way, two CFOAs are saved in comparison with the case that the non-inverted output of the differentiator/integrator would be utilized.

Another benefit of the topology in Fig.3 is the requirement for only grounded capacitors. This is very attractive feature from the integration point of view, because the effect of parasitics in high-frequency applications will be minimized.

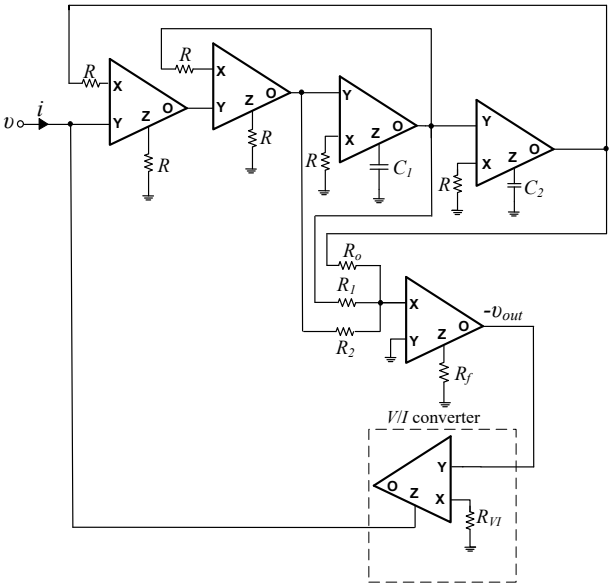


Fig.3: Proposed CPE and FI emulator using CFOAs as active elements.

The expressions for the realized time-constants and gain factors are: $\tau_i=RC_i$ (i=1,2) and $G_j=R_f/R_j$ (j=0,1,2), respectively. Therefore, the values of passive elements are calculated using the design equations in Tables 1 and 2.

4. Simulation Results

The behavior of the proposed emulator will be evaluated using the OrCAD PSpice simulator and the model of the commercially available AD844 discrete IC component. Considering that the emulated values of capacitance and inductance at 1kHz will be equal to 10nF and 2.53H and, also, that the unity-gain frequency of both differentiator and integrator will be f_o=1kHz, then according to (5)-(6) the value of resistor R_{VI} will be R_{VI}=15.9kΩ. The values of passive components of the topology in Fig.3 for emulating a CPE and a FI of order equal to 0.5 are summarized in Table 3.

The obtained magnitude and phase responses of the impedance of CPE and FI are given in Figs.4 and 5, respectively. The simulated values of capacitance and inductance at 1kHz are 9.72nF and 2.66H, respectively.

TABLE 3
VALUES OF PASSIVE COMPONENTS FOR CPE AND FI EMULATORS

Component	CPE (a=0.5)	FI (a=0.5)
C_1	1.59 nF	7.96 nF
C_2	31.8 nF	159.2 nF
R	10 kΩ	10 kΩ
R_f	10 kΩ	10 kΩ
R_o	50 kΩ	2 kΩ
R_1	10 kΩ	10 kΩ
R_2	2 kΩ	50 kΩ
R_{VI}	15.9 kΩ	15.9 kΩ

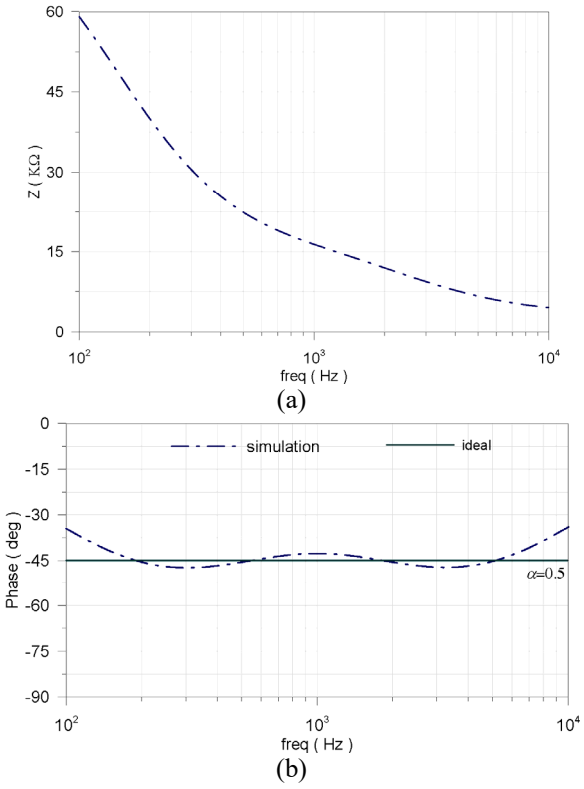
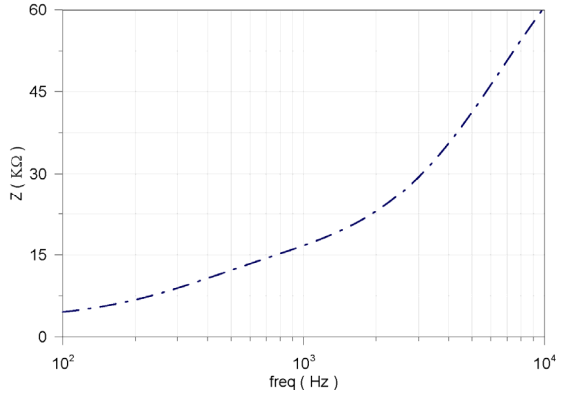


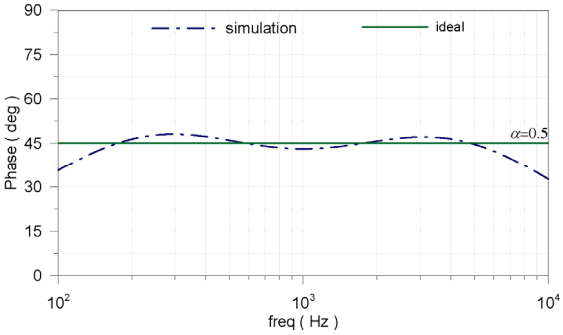
Fig.4: Simulation results about the impedance of CPE (a=0.5) **(a)** magnitude, and **(b)** phase.

In addition, a maximum ±10% deviation from the nominal values (-45° and +45°) of the impedance phases are observed within the ranges 0.14-7.12kHz and 0.13-6.72 kHz for the CPE and FI, respectively.

The time-domain behavior of the emulator has been evaluated through the stimulation by a sinusoidal input voltage of 1kHz frequency and 1V amplitude. The voltage and current waveforms, depicted in Figs.6 and 7 for CPE and FI, respectively, confirm the correct operation of the proposed scheme.



(a)



(b)

Fig.5: Simulation results about the impedance of FI (a=0.5) **(a)** magnitude, and **(b)** phase.

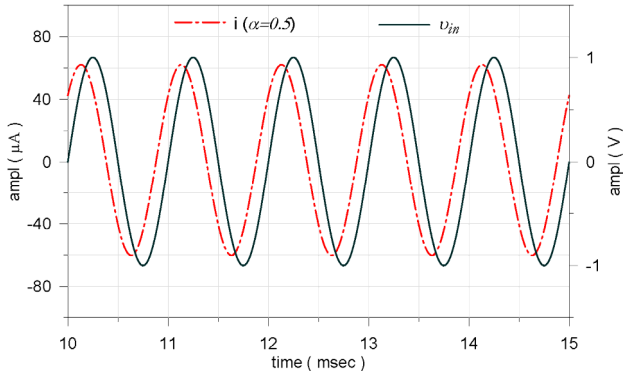


Fig.6: Time-domain behavior of the CPE emulator.

5. Conclusion

The behavior evaluation of the proposed CPE and FI emulator, implemented using CFOAs as active elements, has been performed using the PSpice model of the AD844 discrete IC component. The derived simulation results show that it can accurately approximate the corresponding fractional-order elements within the rage f_o/10 to 7f_o, where f_o is the unity-gain frequency of the differentiator/integrator. The proposed scheme could be an attractive candidate for implementing fractional-order filters and chemical-based CPE sensors, and in material measurements.

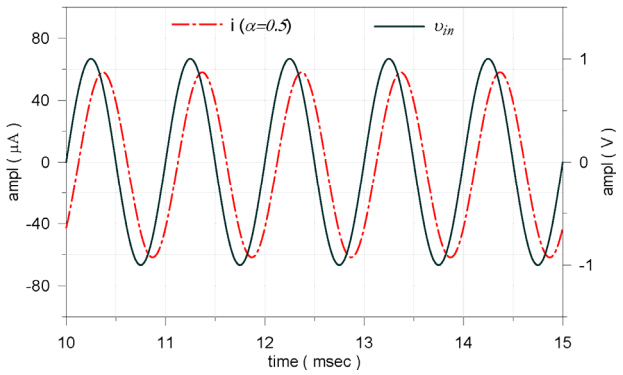


Fig.7: Time-domain behavior of the FI emulator.

Acknowledgment

This work was supported by Grant E.029 from the Research Committee of the University of Patras (Programme K. Karatheodori).

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