Probabilistic Analysis of Coupled Single-Electron Ring Oscillators

Masakazu Ishida[†], Keisuke Nagata[†], Hisato Fujisaka[†], Takeshi Kamio[†], and Kazuhisa Haeiwa[†]

†Faculty of Information Science, Hiroshima City University
Ozuka-higashi, Asa-minami-ku, Hiroshima, 731-3194 Janan
Email: m.ishida@sp.info.hiroshima-cu.ac.jp

Abstract—Ring oscillators consisting of single-electron tunneling (SET) junctions have large phase jitter. In this paper, we investigate whether coupling SET ring oscillators can reduce their phase jitter. By a probabilistic analysis and circuit simulation, we find that phase jitter of all-coupled oscillators decreases as the number of oscillators increases. On the other hand, nearest-neighbor-coupled oscillators are found not to have such characteristic. Additionally, it is realized that the nearest-neighbor-coupled oscillators take phase patterns such that their power consumption is minimized.

1. Introduction

Integrated circuit fabrication technology has constructed nano-scale circuits which control one-by-one tunneling of electrons through insulators by exploiting Coulomb blockade [1], [2]. Together with the single-electron tunneling and ordinary digital circuit architecture, high density and low power logic circuits have been invented [3], [4].

No oscillator consisting only of SET junctions has yet been proposed for clocking these logic circuits although MOS-SET hybrid ring oscillators have been reported [5]. Since SET inverters [6] are greater than 1 in voltage gain, ring oscillators can be constructed of the inverters theoretically. However, phase jitter of the ring oscillators must be large because the tunneling phenomenon is probabilistic [1], [2]. This is considered as a reason why pure SET oscillators have not been constructed.

In this paper, we investigate whether coupling the pure SET ring oscillators can reduce their phase jitter. In addition, we look into effects of the coupling on oscillation frequency and emerging phase pattern. All-coupled and nearest-neighbor-coupled oscillators will be respectively investigated in Sections 3 and 4. The investigations in the two sections will be carried out by both probabilistic analysis and circuit simulation.

2. Multi-Gate SET Inverters

Fig. 1 (a) shows a SET transistor and its gate voltage versus drain current characteristic. The current flow is caused by continuous electron tunneling. Fig. 1 (b) shows a dual-gate SET transistor. Applying voltage to another gate shifts its voltage-current characteristic horizontally as

(a) Single-electron transistor

(b) Dual-gate single-electron transistor. The I_{DS}-V_{g1} characteristic is obtained when $Cg_1 = Cg_2 = Cg$ and $Cg_2 V_{g2} = e/2$.
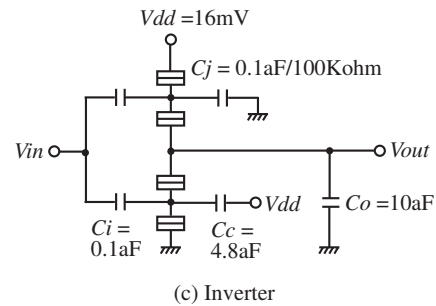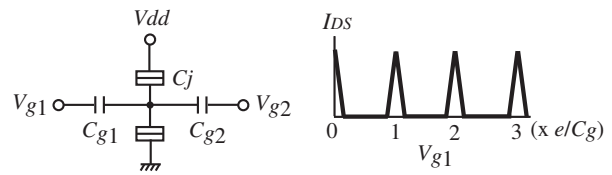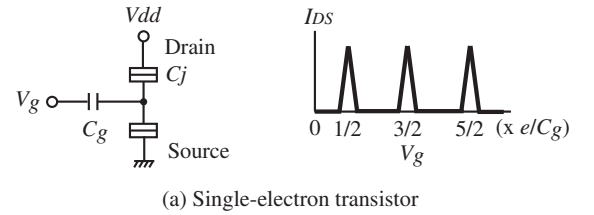
(c) Inverter

Figure 1: SET transistors and inverter.

shown in the figure. Let us take two dual-gate SET transistors through which drain current flows at different gate voltages for NMOS and PMOS transistors. Then, a SET counterpart of a CMOS inverter is constructed as shown in Fig. 1 (c) [6]. The circuit parameters may be changed depending on the number of input gates in circuit simulation.

Single-electron tunneling is a probabilistic phenomenon. The time τ at which a single-electron tunnels through a junction after its tunneling condition is satisfied has the following exponential probability density function (PDF) [1], [2]:
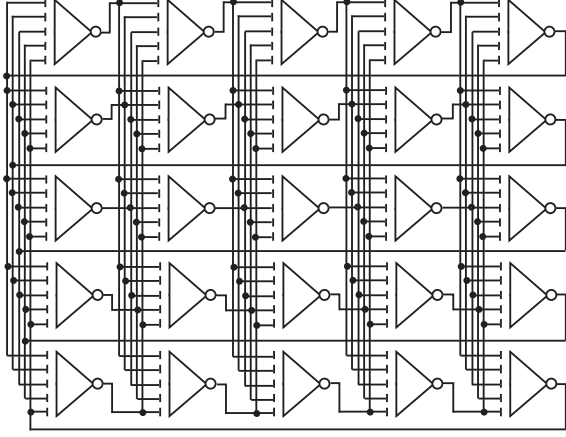
$$p_1(\tau) = \Gamma \exp(-\Gamma\tau) \tag{1}$$

Figure 2: All-coupled ring oscillators ($N = 5$, $M = 5$).

where tunneling frequency Γ of single-electrons is a function of the voltage V_j across the junction and the temperature T, as given by [1], [2]

$$\Gamma(V_j, T) = \frac{1}{eR_T} \cdot \frac{V_j - V_c}{1 - \exp\left(-\dfrac{e(V_j - V_c)}{k_B T}\right)} \qquad (2)$$

V_c : Critical voltage, R_T : Tunneling resistance,

e : Elementary charge, k_B : Boltzmann constant

Once an electron has tunneled through a junction in a SET inverter, single-electrons subsequently tunnel through other junctions in a very short time for the inverter to be in a stationary state [6]. Then, a PDF of the switching duration of the SET inverter can be approximated by Eq. (1).

3. All-Coupled SET Ring Oscillators

Since the voltage gain of the SET inverter is greater than 1, ring oscillators can be constructed of the inverters. Coupled ring oscillators are constructed of the multi-gate SET inverters which are built of two multi-gate SET transistors similar to the one in Fig. 1 (b). The parameters of the SET inverters are determined so as for the SET inverters to be equivalent to NAND gates. Fig. 2 exemplifies all-coupled ring oscillators.

Let the number of the ring oscillators and the number of SET inverters organizing each ring oscillator be denoted by M and N. A SET inverter in coupled ring oscillators is indicated by (i, j), $1 \leq i \leq 2N$, $1 \leq j \leq M$. Since all the SET inverters switch twice in an oscillation period, we let integer i take from 1 to $2N$. Physically, (i, j) and $(i + N, j)$ indicate an identical SET inverter.

Let us denote a time at which a SET inverter of jth ring oscillator switches by τ_j. Assume that all the inputs to $(1, j)$-inverters change at time 0 for all j, which is represented by using a joint PDF p_0 of τ_1, $\cdots$, τ_M of virtual $(0, j)$-inverters by

$$p_0(\tau_1, \cdots, \tau_M) = \prod_{j=1}^{M} \delta(\tau_j) \qquad (3)$$

where $\delta(\cdot)$ is the Dirac delta function. Then, the joint PDF p_1 of τ_j of $(1, j)$-inverters is given by

$$p_1(\tau_1, \cdots, \tau_M) = \prod_{j=1}^{M} p_1(\tau_j) \qquad (4)$$

Since the inverter outputs are binary sequences, tunneling frequency Γ of single-electrons in the inverters is considered to be constant. A joint PDF p_i of τ_j of (i, j)-inverters is expressed by using a joint PDF p_{i-1} of τ_j of $(i - 1, j)$-inverters as

$$p_i(\tau_1, \cdots, \tau_M) = \qquad (5)$$

$$\int_0^{l_s} \cdots \int_0^{l_s} \left\{ \prod_{j=1}^{M} p_1(\tau_j - \max(\tau_1', \cdots, \tau_M')) \right\}$$

$$\times p_{i-1}(\tau_1', \cdots, \tau_M') d\tau_1' \cdots d\tau_M'$$

$$l_s = \min(\tau_1, \cdots, \tau_M)$$

The iterative integral equation (5) can be represented by another iteration as follows:

$$p_i(\tau_1, \cdots, \tau_M) = \left\{ \prod_{j=1}^{M-1} \Gamma \exp(-\Gamma \tau_j) \right\} h_i(\tau_M) \qquad (6)$$

$$\text{for } \min(\tau_1, \cdots, \tau_{M-1}) \geq \tau_M$$

$$h_i(\tau_M) = M! \Gamma \exp(-\Gamma \tau_M) \qquad (7)$$

$$\times \int_0^{l_s} h_{i-1}(\tau_M') \int_{\tau_M'}^{l_s} \exp(-\Gamma \tau_{M-1}') \cdots$$

$$\cdots \int_{\tau_2'}^{l_s} \exp(-\Gamma \tau_1') \exp(M \Gamma \tau_1') d\tau_1' \cdots d\tau_{M-1}' d\tau_M'$$

From Eqs. (6) and (7), we obtain $p_{2N}(\tau_1, \cdots, \tau_M)$ easily for any M and N.

We computed average oscillation frequency f_{avr} and standard frequency deviation σ_f given respectively

$$f_{avr} = \int_0^\infty \cdots \int_0^\infty \tau_i^{-1} p_{2N}(\tau_1 \cdots \tau_M) d\tau_1 \cdots d\tau_M \qquad (8)$$

$$\sigma_f = \int_0^\infty \cdots \int_0^\infty (\tau_i^{-1} - f_{avr})^2 p_{2N}(\tau_1 \cdots \tau_M) d\tau_1 \cdots d\tau_M \qquad (9)$$

Fig. 3 shows f_{avr} and σ_f / f_{avr}. The values obtained with SET simulator SIMON [7] are also shown in the figure. The average frequency is normalized as $f_{avr} = 1$ for $M = 1$. From the figure, we see that all-coupling decreases the deviation of oscillation frequency or phase jitter. The phase jitter is reduced as the number M of ring oscillators increases. Notice that the average frequency also decreases with M.
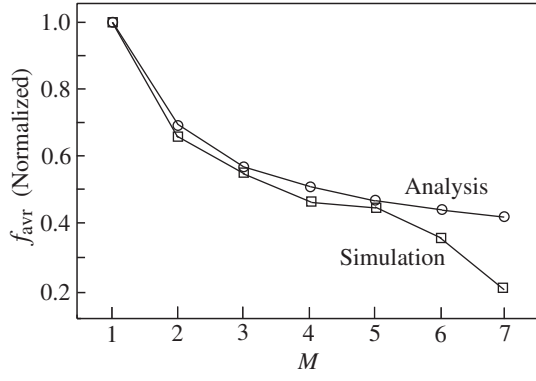
(a) Normalized average frequency
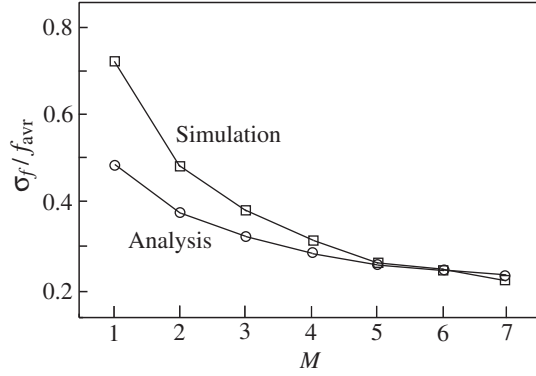
(b) Frequency deviation divided by average frequency

Figure 3: Average frequency f_{avr} and its deviation σ_f plotted against the number M of ring oscillators each of which is coupled to all the other ring oscillators.

4. SET Ring Oscillators with Nearest-Neighbor Couplings

Ring oscillators with nearest-neighbor couplings are constructed of triple-gate inverters as shown in Fig. 4. Two ring oscillators built of $(i, 1)$ and (i, M)-inverters are connected for the oscillators to be circularly coupled.

In circularly coupled ring oscillators, several phase patterns which are invariant under rotations are expected to emerge. In each of the emerged oscillation mode, the phase difference between two adjacent ring oscillators is given by

$$\Delta\theta_{avr} = \frac{2\pi k}{M}, \quad k(> 0) : \text{an integer dividing } M \qquad (10)$$

We refer to each mode with the integer k. From Eq. (10), the circular coupling condition, and that multi-gate inverters are equivalent to NAND gates, average oscillation period in mode k is given by

$$\frac{1}{f_{avr}} = \frac{2NM}{M - 2Nk} \cdot \frac{1}{\Gamma} \qquad (11)$$

Both the average drain currents of the SET transistors in the inverters and the average oscillation frequency of the
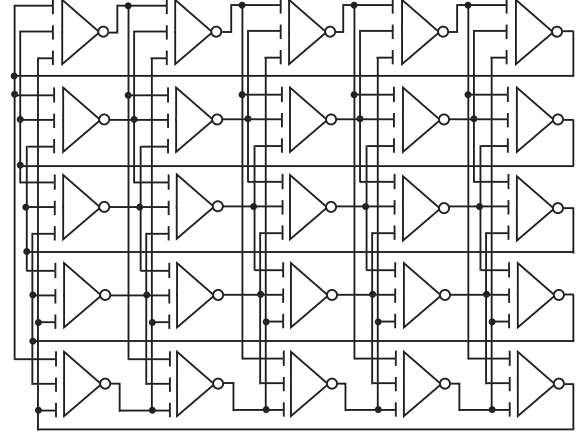

Figure 4: Circularly coupled ring oscillators with nearest-neighbor couplings ($N = 5$, $M = 5$).

ring oscillators are proportional to the frequency of signle-electron tunneling in the inverters. If the circularly coupled ring oscillators take an oscillation mode which minimizes power consumption of the coupled oscillators, the mode index k is given from Eq. (11) by

$$k = \left[\frac{M}{2N}\right] : \text{the largest integer that does not exceed } \frac{M}{2N} \qquad (12)$$

Since the couplings are nearest-neighbor couplings and have circularly symmetric structure, a joint PDF of the switching time of $(i, j-1)$, (i, j), and $(i, j+1)$-inverters satisfies

$$p_i(\tau_{j-1}, \tau_j, \tau_{j+1}) = \qquad (13)$$
$$p_i(\tau_{j-1-l} + l\Delta T_{avr}, \tau_{j-l} + l\Delta T_{avr}, \tau_{j+1-l} + l\Delta T_{avr}),$$
$$\Delta T_{avr} = \frac{1}{f_{avr}} \cdot \frac{k}{M}, \quad l : \text{integer}$$
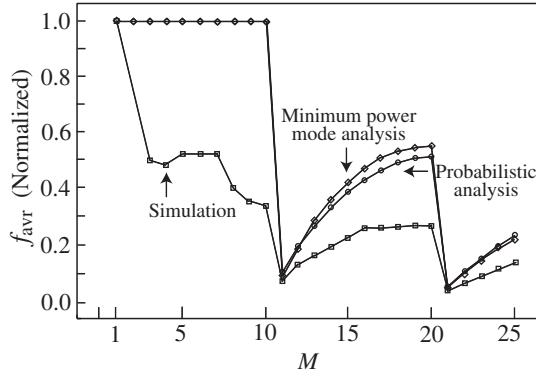
The joint PDF is expressed with conditional PDFs by

$$p_{i+1}(\tau_{j-1}, \tau_j, \tau_{j+1}) = \qquad (14)$$
$$p_{i+1}(\tau_j | \tau_{j-1}, \tau_{j+1}) p_{i+1}(\tau_{j-1} | \tau_{j+1}) p_{i+1}(\tau_{j+1})$$

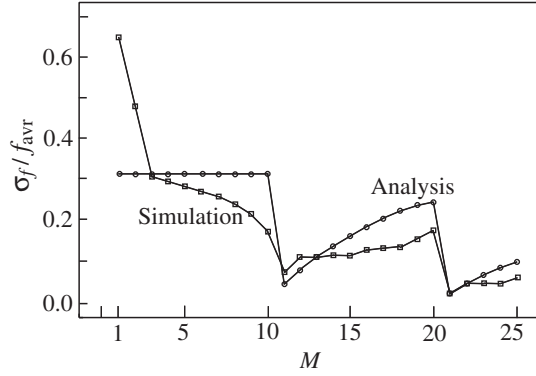The nearest-neighbor couplings also derive the following inequality:

$$\tau_j' < \min(\tau_{j-1}, \tau_j, \tau_{j+1}) \qquad (15)$$

Then, the PDFs on the right hand side of Eq. (14) can be expressed as

$$p_{i+1}(\tau_{j+1}) = \int_0^{\tau_{j+1}} \int_0^{\tau_{j+1}} \int_0^{\tau_{j+1}} \qquad (16)$$
$$p_1(\tau_{j+1} - \max(\tau_j', \tau_{j+1}', \tau_{j+2}'))$$
$$\times p_i(\tau_j', \tau_{j+1}', \tau_{j+2}') d\tau_j' d\tau_{j+1}' d\tau_{j+2}'$$

(a) Normalized average frequency

(b) Frequency deviation divided by average frequency

Figure 5: Average frequency f_{avr} and its deviation σ_f plotted against the number M of SET ring oscillators each of which is coupled to its nearest-neighbor oscillators.

$$p_{i+1}(\tau_{j-1}|\tau_{j+1}) = \int_0^{\min(\tau_{j-1},\tau_{j+1})} \int_0^{\tau_{j-1}} \int_0^{\tau_{j-1}} \quad (17)$$
$$p_1(\tau_{j-1} - \max(\tau'_{j-2}, \tau'_{j-1}, \tau'_j))$$
$$\times p_i(\tau'_{j-2}, \tau'_{j-1}, \tau'_j) d\tau'_{j-2} d\tau'_{j-1} d\tau'_j$$

$$p_{i+1}(\tau_j|\tau_{j-1}, \tau_{j+1}) = \int_0^{\tau_{j+1}} \int_0^{\min(\tau_{j-1},\tau_j,\tau_{j+1})} \int_0^{\tau_{j-1}} \quad (18)$$
$$p_1(\tau_j - \max(\tau'_{j-1}, \tau'_j, \tau'_{j+1}))$$
$$\times p_i(\tau'_{j-1}, \tau'_j, \tau'_{j+1}) d\tau'_{j-1} d\tau'_j d\tau'_{j+1}$$

From Eqs. (13), (14), (16), (17), and (18), we obtain $p_{2N}(\tau_{j-1}, \tau_j, \tau_{j+1})$ and its marginal PDF $p_{2N}(\tau_j)$.

Fig. 5 (a) shows average oscillation frequency obtained from Eqs. (11) and (12), from $p_{2N}(\tau_j)$, and by circuit simulation for $N = 5$. Frequency deviation is also obtained from $p_{2N}(\tau_j)$ and by circuit simulation. The deviation against M is shown in Fig. 5 (b). From the figures, we realize that increasing the number M of ring oscillators does not always decrease their phase jitter and that the nearest-neighbor-coupled ring oscillators take an oscillation mode which minimizes their power consumption.

5. Conclusions

We have investigated the phase jitter of coupled SET ring oscillators by probabilistic analysis and circuit simulation. This paper supposes $\Gamma(=1)$ of Eq. (2) in the probabilistic analysis. In circuit simulation Γ changes because junction voltage V_j is changed with the input capacitor of the inverters. Herewith, we thinkable that it causes the gap between the analysis and the simulation in Figs. 3 and 5.

By the analyses, we find that the phase jitter of all-coupled oscillators can be reduced by increasing the number of ring oscillators. However, the oscillation frequency decreases with the number. One of our future works is to establish a novel coupling to reduce phase jitter independently of oscillation frequency.

Another result of the analyses is that nearest-neighbor coupling does not always reduce phase jitter. We also realize through the analyses that the nearest-neighbor coupling makes the coupled ring oscillators take a phase pattern such that their power consumption is minimized. The emergence of the phase pattern will be utilized for generating multi-phase clocks as we obtain multi-phase periodic waves from coupled CMOS ring oscillators in Ref. [8]. Investigating further the relation between coupling and phase pattern is our another future work.

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