From theory to experiments in a ZAD-controlled buck converter

Daniel Burbano† Fabiola Angulo‡, and Gerard Olivar ‡

†Department of Systems and Computer Sciences, University of Naples Federico II
Via Claudio 21, 80125 Napoli, Italy
Email: danielalberto.burbanolombana@unina.it
‡Universidad Nacional de Colombia - Sede Manizales - Facultad de Ingeniería y Arquitectura -
Departamento de Ingeniería Eléctrica, Electrónica y Computación - Percepción y Control Inteligente -
Bloque Q, Campus La Nubia, Manizales, 170003 - Colombia
Emails: fangulog@unal.edu.co, golivart@unal.edu.co

Abstract—Many studies have been devoted to analyze the Zero Average Dynamics (ZAD) strategy for controlling power converters. In this paper the ideal model of the buck converter is analyzed when is controlled by ZAD strategy; however, the analog to digital process is considered in the modeling state, because all signals used to compute the duty cycle pass through analog to digital converter. In particular two different ways to quantize the signals are used. As ZAD-strategy is highly sensitivity to duty cycle values which are computed from the capacitor voltage and inductor current, this communication intends to explain why the experiments are very different from the ideal model results.

1. Introduction

In the last decade ZAD strategy has been developed for controlling DC-DC converters. This controller uses a sliding surface defined as a linear combination of the error and its derivative, which is forced to have a zero average. Previous theoretical and numerical studies have shown that ZAD strategy offers two important advantages: very low error and fixed switching frequency [1]. Implementations based on DSP and FPGA technologies use Analog to Digital (A/D) converters, which imply a quantization process. Quantization is the process by which a continuous range of values is approximated by a set of discrete symbols or values. The inclusion of quantization effects in modeling stage is not a new idea [2]-[3]; particularly, in [4]-[5] it was proven the existence of a limit cycle. As the ZAD control is sensitivity to computation of the duty cycle, small changes in it causes different behaviors on the controlled system. Some of those changes are given by quantization process. In [6] a complete explanation about the influence of the quantization effects on route to chaos in a ZAD-controlled buck converter was presented, and in [7] quantization, delay and internal resistances were taking into account to obtain good agreement between experiments and numerical results. The main difference between this work and other close works is that in this paper and with the aim to emphasize the effects of A/D converter in numerical results, two different processes of quantization are explored: by rounding to nearest integer and by rounding down. Depending on what quantization technique is used, results are very different. Major differences when bit changes are given in the duty cycle are the main obstacle to obtain very good results in experiments.

The rest of the paper is organized as follows: section 2 presents the basis of the ZAD-control and its application to the buck converter. In section 3 the main characteristics of the analog to digital conversion process are presented. Section 4 is devoted to analysis of the results. Finally, in section 5 conclusions are presented.

2. DC-DC Buck converter with ZAD strategy

A simplified diagram of the closed-loop buck converter is shown in Figure 2. Its main feature is that the output value V_o is lower than the source V_{in} (step down converter). Switches S_1 and S_2 operate in a complementary way, i.e. when S_1 is open, S_2 is closed, and viceversa.

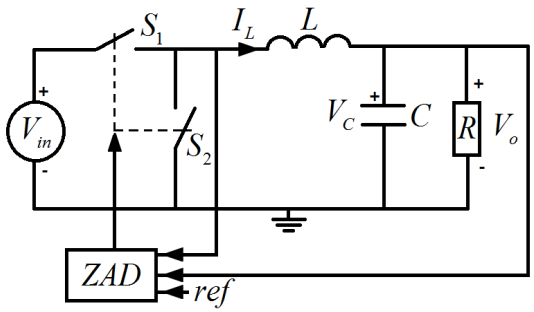

Figure 1: Scheme of a ZAD-controlled Buck converter.

The mathematical model can be expressed in compact form as:

$$\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \end{pmatrix} = \begin{pmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & 0 \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{V_{in}}{L} \end{pmatrix} u \qquad (1)$$

where $x_1 = V_C$, $x_2 = I_L$ and u belongs to $\{0, 1\}$.

The next step is to design a control strategy so that the load voltage V_0 is regulated to a desired value. To solve this regulation problem, it is necessary to compute the time

(D) when the switch S_1 is ON ($u = 1$) in each previously defined sampling time T ($D \in [0\ T]$). Time D is known as the duty cycle and it is normalized to $d = D/T$ ($d \in [0\ 1]$) and is usually presented in percentage. The control strategy we use is based on the concept of Zero Average Dynamics on the output (ZAD) [8].

The ZAD-strategy can be summarized as follows. First, choose a sampling time T and a surface $s(x) = 0$ in the state space; second, force $s(x(t))$ to have zero average in each sampling time; and finally, compute the duty cycle. As reported in [9], one of the practical possibilities for choosing the surface is to define a piecewise-linear function $s_{pwl}(t)$. Then, the zero average condition is

$$\int_{kT}^{(k+1)T} s_{pwl}(t)dt = 0 \tag{2}$$

where we can solve for the duty cycle D. If the duty cycle exceedes the limit value, then is saturated. With this duty cycle, which changes in each T-cycle, the system exhibits rich dynamic: transitions from stable 1T-periodic orbit to chaos, including period-doubling, chaotic bands merging, and period-doubling of chaotic band processes, among others, when parameter k_s is varied [1].

Table 1: Simulation parametrics values

Parameter	Value
V_{in}	$40V$
R	20Ω
L	2mH
C	40uF
Reference	32V
ks	$4.5/\sqrt{LC}$
T	50us

A simulation of the ZAD-controlled buck converter using parameter values registered in table 1 is depicted in Figure 2. With these results we can show that ZAD-strategy present a steady state error of 0.0617% and 1-periodic orbit with non-saturated duty cycle $d = 79.84\%$

3. Analog to Digital Conversion Process

A/D converter transforms a continuous signal in a set of discrete values. Since the ZAD strategy will be implemented in a digital platform, it is convenient to include the A/D conversion process in the modeling stage. Figure 3 shows the main parts of this process, which are: sample and hold, quantization and encoder processes.

3.1. Sample and hold and quantization processes

The sample and hold process consists of taking the value of the signal at a given instant kT (sampling) and holding it until the instant $kT + T$. On the other hand, the quantization

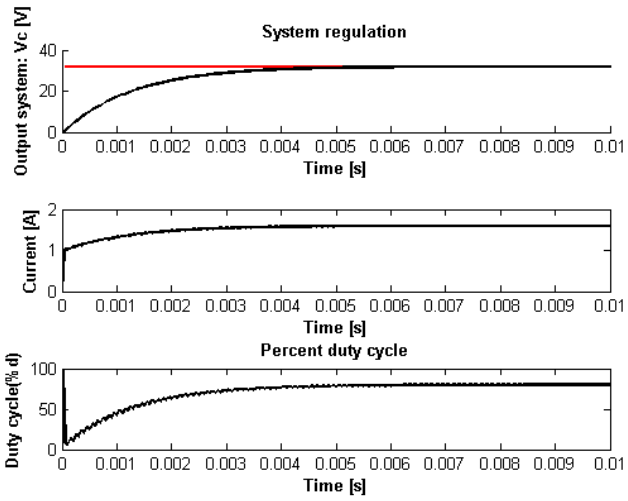

Figure 2: Dynamic close-loop buck converter system controlled by ZAD-strategy

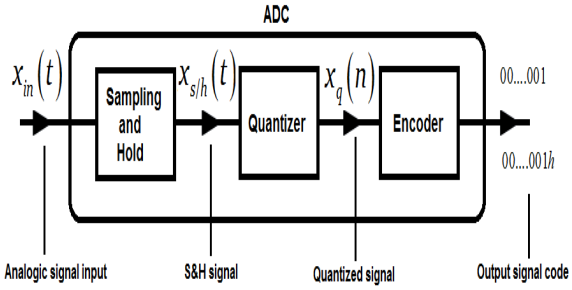

Figure 3: Scheme of the Analog-to-Digital conversion process.

process consists of transforming a continuous signal into a finite discrete set of values. The quantization is a nonlinear process and it can be expressed mathematically as

$$h = \frac{V_{refhi}}{2^n} \tag{3}$$

where h indicates the quantization level, n is the number of bits of the A/D converter, and V_{refhi} is the high voltage reference. A quantized signal is shown in Figure 4, the dashed line represents the desired linear response, and the staircase functions is the output of the quantizer.

3.2. Encoder Process

In this part, a binary code is assigned to each stair in the Figure 4. In this paper we considerate two expressions to compute the A/D converter code:

$$ADC_{Code} = round\left(\frac{2^n\left(x(n) - V_{reflow}\right)}{V_{refhi} - V_{reflow}}\right) \tag{4}$$

$$ADC_{Code} = floor\left(\frac{2^n\left(x(n) - V_{reflow}\right)}{V_{refhi} - V_{reflow}}\right) \tag{5}$$

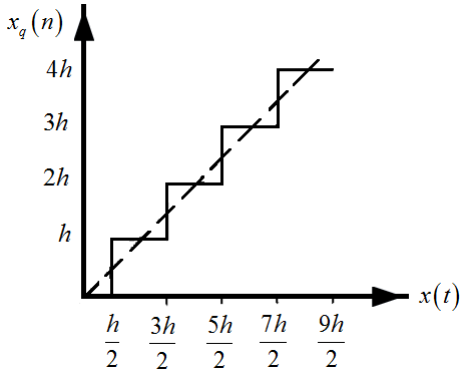

Figure 4: Quantizer characteristic

Where V_{reflow} is the low voltage reference. Equation (4) uses the function round, which rounds to nearest integer, and eq. (5) rounds down. As it is analyzed in the next section, depending on what expression is used, the response of the ZAD control is very different.

4. Results

Simulation results including the A/D process are shown in Figures 5 and 6. In all cases $V_{refhi} = 40V$, $V_{reflow} = 0V$, and n is varied to compare the behaviour of the system. Depending on the number of bits n as well as of the A/D conversion technique the duty cycle exhibits very different behaviour compared to ideal model. Figure

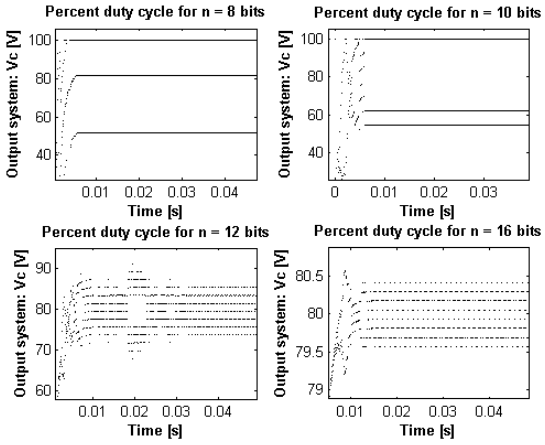

Figure 5: Percent duty cycle varying ADC resolution using equation 4 to calculate ADC_{code}

5 was obtained using Eq. (4) to compute the values of the state variables; in this case, the steady state errors (not shown here) were 2.7645%, 1.1200%, 0.0773% and 0.0635% for $n = 8$, $n = 10$, $n = 12$ and $n = 16$ bits, respectively. For $n = 8$ and $n = 10$ bits the system exhibits 4-periodic orbit with two non-saturated duty cycles $d1 = 51.95\%$, $d2 = 81.89\%$ for the first case, and

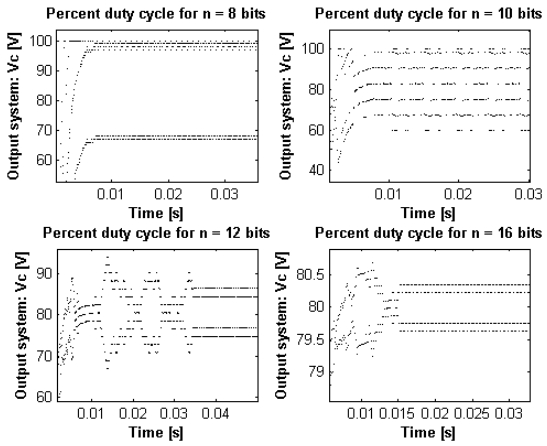

Figure 6: Percent duty cycle varying ADC resolution using equation 5 to calculate ADC_{code}

$d1 = 54.57\%$, $d2 = 62.06\%$ for the second case, and two saturated duty cycle $d3, d4 = 100\%$. For $n = 12$ and $n = 16$ the duty cycle oscillates between a maximum and minimum of non-saturated duty cycles, $dmx = 85.38\%$ and $dmn = 73.79\%$ for $n = 12$; and $dmx = 80.41\%$ and $dmn = 79.57\%$ for $n = 16$.

Figure 6 was obtained using Eq. (5) to compute the values of the state variables; in this case, the steady state errors (not shown here) were 6.2699%, 1.7872%, 0.4897% and 0.0346% for $n = 8$, $n = 10$, $n = 12$ and $n = 16$ bits, respectively. For $n = 10$ it is not clear the periodicity of the duty cycle; For $n = 12$ and $n = 16$ the duty cycle oscillates between a maximum and minimum of non-saturated duty cycles, $dmx = 86.39.38\%$ and $dmn = 74.81\%$ for $n = 12$; and $dmx = 80.35\%$ and $dmn = 79.62\%$ for $n = 16$.

5. Conclusions

It was numerically proven that depending on the rounding of the quantizer, the value of the duty cycle does not change significatively but the behaviour of the system do. For this reason, inclusion of analog to digital conversion process in the modeling of ZAD-controlled buck converter is essential to obtain better results than the ideal model; this is because the technique is high sensitive to small changes in the values of the state variables, mainly on the current value. Also, it can be seen chaotic transient dynamics in the simulations.

References

[1] F. Angulo, E. Fossas and G. Olivar, "Transition from periodicity to chaos in a PWM-controlled Buck converter with ZAD strategy," *Int. J. Bif. and Chaos*, vol.15, pp.3245-3264, 2005.

[2] J. Slaughter, “Quantization Errors in Digital Control Systems”, *IEEE Trans. on Aut. Cont.*, vol.9, no.1, pp.70–74, 1964.

[3] Y. Kuroe, and K. Okada, “Analysis of Floating-Point Quantization Errors in Digital Control Systems: Influence of The Order of Arithmetic Steps in Controller”, *American Control Conference*, pp.702–707, June 1992

[4] A. Peterchev, and S. Sanders,“Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters”, *IEEE Transactions on Power Electronics*, Vol.18, no.1, pp.301–308, 2003.

[5] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, “Modeling of Quantization Effects in Digitally Controlled DC-DC Converters”, *IEEE Trans. on Power Electronics*, vol.22, no.1, pp.208–215, 2007.

[6] J.A. Taborda, D. Burbano, and F. Angulo, “Quantization effects on period doubling route to chaos in a ZAD-controlled buck converter”, *Mathematical Problems in Engineering*, vol.2012, art id. 526394, doi:10.1155/2012/526394, pp.1–19, 2012.

[7] F. Hoyos, D. Burbano, F. Angulo, G. Olivar, N. Toro, and J.A. Taborda, “Effects of quantization, delay and internal resistances in digitally ZAD-controlled buck converter”, *Int. J. Bif. and Chaos*, vol.22, no.10, doi:10.1142/S0218127412502458, pp.1–9, 2012

[8] E. Fossas, R. Griñó, and D. Biel, “Quasi-sliding control based on pulse width modulation, zero averaged dynamics and the L_2 norm”. *in Advances in Variable Structure System, Analysis, Integration and Applications*, Ed. by Xinghuo Yu and Jian-Xin Xu, Ed. World Scientfic, pp.335–344, 2001.

[9] F. Angulo, G. Olivar and M. di Bernardo, Two-parameter Discontinuity-induced Bifurcation Curves in a ZAD-Strategy Controlled DC-DC Buck Converter. *IEEE Trans. on Circuits and Systems-I, Regular papers* **55**:2392-2401. 2008.