A Theoretical Examination of an Unexpected Transfer of Power Packets by Synchronization Failure

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Abstract—Power packet is a unit of power transmission by pulses tagged with information such as a destination of the packet. This paper examines a phenomenon in power packet dispatching system under out-of-synchronization conditions. Through theoretical study on the detection error of information tags based on developed power packet dispatching system, we show there can happen temporal change of the packet arrival point.

1. Introduction

Power packet is a unit of power transmission by pulses tagged with information about loads (destinations), power sources, and so on. The concept of power packet was proposed from a supplier's viewpoint by Toyoda in 1990s [1]. In addition, there is a proposal of an electric power distribution system based on power packet transactions [2] and a proposal of Energy Packet Networks providing energy on-demand to cloud computing servers using power pulses as units of energy transmission [3].

Our group has physically realized a power packet dispatching system by tagging power packets as their voltage wave forms. Up to the present, we have developed mixers and routers as equipments realizing power packet [4, 5]. The mixer generates power packets as time series of power pluses and information tags by switching DC power supplies, while the router dispatches the packets to loads according to the tags on the packets. We have also realized multi-path routing through broadcast of information tags in a network composed of several routers [6].

The power packet dispatching system has been developed on the assumption that synchronization can be kept between the mixer and the router. If the synchronization is failed, there should happen detection errors of tags which cause an unexpected transfer of power packets to multiple destinations [7]. In particular, in the developed power packet dispatching system, temporal change of the packet arrival point was observed at failure of synchronization. In this paper, the mechanism of this phenomenon is examined through theoretical study on the detection error, which would reveal issues in system design.

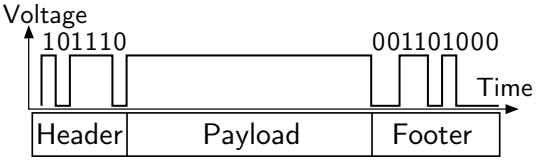

Figure 1: A configuration of a power packet.

2. Configuration of Developed System

In this section, we describe configuration of the developed power packet dispatching system. Fig. 1 shows a configuration of a power packet. The power packet consists of header, payload, and footer. The header is an information tag about a start signal and addresses of the destination and the sender, while the footer is an information tag about an end signal. The payload transfer power. The header and the footer represent information by a sequence of a bit denoted by a low voltage value ("0") and a high voltage value ("1"). The power packet is generated by the mixer.

Then, we describe configuration of the router which dispatches the packets to loads according to the tags on the packets. The router connects its input to several outputs through switching devices. The switching devices are driven to dispatch packets according to the input binary sequence detected as input voltage values at the rising edges of the router's clock.

3. Mathematical Model

In the following, we assume that the bit length and the clock period of the router are constant. Let the bit length be 1 and the clock period be $\theta \in \mathbb{R}_{>0}$. For any real number $x \in \mathbb{R}$, $\lfloor x \rfloor$ denotes the largest integer not greater than x and $\lceil x \rceil$ denotes the smallest integer not less than x. Define $x \mod 1 \stackrel{\text{def}}{=} x - \lfloor x \rfloor$.

We consider infinite binary sequences. For $\theta \in \mathbb{R}_{>0}$ and $\phi \in \mathbb{R}$, define $C_{\theta,\phi} \in \mathbb{R}^{\mathbb{Z}}$ as

$$C_{\theta,\phi}[j] = \theta j + \phi \text{ for } j \in \mathbb{Z}. \tag{1}$$

$C_{\theta,\phi}$ denotes time instants of rising edges of the clock with period θ. As a representation of rising edges in steady state, we also define the following set:

$$Clk(\theta,\phi) \stackrel{\text{def}}{=} \left\{ C_{\theta,\phi}[j] \;\middle|\; j \in \mathbb{Z} \right\}. \tag{2}$$

For $k \in \mathbb{Z}$, let the k-th bit be inputted at $t \in [k, k+1)$. In other words, the $\lfloor t \rfloor$-th bit is given at $t \in \mathbb{R}$. Let $N \in \mathbb{Z}_{\geq 1}$. N denotes length of a single power packet. For $i \in \mathbb{Z}$, let the i-th packet be inputted at $t \in [iN, (i+1)N)$. In other words, the $\lfloor t/N \rfloor$-th packet is given at $t \in \mathbb{R}$.

4. The First Bit with Error in Each Packet

A detection error occurs at bits where the router's clock rises more than twice or does not rise. We can obtain a following property that specifies bits at which detection errors occur.

Property 1 *Let $\phi \in \mathbb{R}$. Then, the following equations hold for all $k \in \mathbb{Z}$:*

in the case of $0 < \theta \leq 1/2$*:*

$$|Clk(\theta, \phi) \cap [k, k+1)| \geq 2, \tag{3}$$

in the case of $1/2 < \theta < 1$*:*

$$|Clk(\theta, \phi) \cap [k, k+1)| = \begin{cases} 2, & \text{if } k \in \left\{ \left\lfloor \dfrac{\phi/\theta - n}{1/\theta - 1} \right\rfloor \,\middle|\, n \in \mathbb{Z} \right\} \\ 1, & \text{otherwise}, \end{cases} \tag{4}$$

in the case of $\theta = 1$*:*

$$|Clk(\theta, \phi) \cap [k, k+1)| = 1, \tag{5}$$

in the case of $\theta > 1$*:*

$$|Clk(\theta, \phi) \cap [k, k+1)| = \begin{cases} 0, & \text{if } k \in \left\{ \left\lceil \dfrac{n - \phi/\theta}{1 - 1/\theta} \right\rceil - 1 \,\middle|\, n \in \mathbb{Z} \right\} \\ 1, & \text{otherwise}. \end{cases} \tag{6}$$

□

To focus on the i-th packet, treat time with $t_i = t - iN$. For $N \in \mathbb{Z}_{\geq 1}$, $\theta \in \mathbb{R}_{>0}$, and $0 \leq \phi_0 < \theta$, define a real-valued sequence $\psi_{N,\theta,\phi_0} \in \mathbb{R}^{\mathbb{Z}}$ as

$$\psi_{N,\theta,\phi_0}[i] = \min Clk(\theta, \phi_0) \cap [iN, \infty) - iN. \tag{7}$$

$\psi_{N,\theta,\phi_0}[i]$ denotes the time instance when the first clock after $t_i = 0$ rises in the coordinate t_i, which implies phase information of the i-th packet.

According to Property 1, the detection error occurs in each bit in the case of $\theta \leq 1/2$, while no detection error occurs in each bit in the case of $\theta = 1$. In the case where $1/2 < \theta < 1$ or $\theta > 1$, we investigate the bit number at which the first detection error after $t_i = 0$ occurs as following.

4.1. The case where $1/2 < \theta < 1$

For $N \in \mathbb{Z}_{\geq 1}$, $1/2 < \theta < 1$, and $0 \leq \phi_0 < \theta$, define $\xi_{N,\theta,\phi_0} \in \mathbb{R}^{\mathbb{Z}}$ as

$$\xi_{N,\theta,\phi_0}[i] = \min \left\{ \left\lfloor \frac{\psi_{N,\theta,\phi_0}[i]/\theta - n}{1/\theta - 1} \right\rfloor \,\middle|\, n \in \mathbb{Z} \wedge \left\lfloor \frac{\psi_{N,\theta,\phi_0}[i]/\theta - n}{1/\theta - 1} \right\rfloor \geq 0 \right\}. \tag{8}$$

From Property 1, $\xi_{N,\theta,\phi_0}[i]$ implies the bit number at which the first detection error after $t_i = 0$ occurs. Substituting Eq. (7) into Eq. (8), we obtain the following form of $\xi_{N,\theta,\phi_0}[i]$:

$$\xi_{N,\theta,\phi_0}[i] = \left\lfloor \left(\frac{\phi_0 - iN}{\theta} \mod 1 \right) \frac{\theta}{1-\theta} \right\rfloor. \tag{9}$$

Letting

$$\Delta_+\xi = \left(-\frac{N}{\theta} \mod 1 \right) \frac{\theta}{1-\theta}, \tag{10}$$

$$\Delta_-\xi = \left(1 - \left(-\frac{N}{\theta} \mod 1 \right) \right) \frac{\theta}{1-\theta}, \tag{11}$$

we obtain

$$\xi_{N,\theta,\phi_0}[i+1] = \begin{cases} \left\lfloor \left(\dfrac{\phi_0 - iN}{\theta} \mod 1 \right) \dfrac{\theta}{1-\theta} + \Delta_+\xi \right\rfloor \\ \qquad \text{if } \left(\dfrac{\phi_0 - iN}{\theta} \mod 1 \right) + \left(-\dfrac{N}{\theta} \mod 1 \right) < 1, \\ \left\lfloor \left(\dfrac{\phi_0 - iN}{\theta} \mod 1 \right) \dfrac{\theta}{1-\theta} - \Delta_-\xi \right\rfloor \\ \qquad \text{if } \left(\dfrac{\phi_0 - iN}{\theta} \mod 1 \right) + \left(-\dfrac{N}{\theta} \mod 1 \right) \geq 1. \end{cases} \tag{12}$$

Thus, we obtain the following:

$$\xi_{N,\theta,\phi_0}[i+1] - \xi_{N,\theta,\phi_0}[i] = \lfloor \Delta_+\xi \rfloor \text{ or } \lceil \Delta_+\xi \rceil, \tag{13}$$

if $\left(\frac{\phi_0 - iN}{\theta} \mod 1 \right) + \left(-\frac{N}{\theta} \mod 1 \right) < 1$ holds; otherwise, we obtain the following:

$$\xi_{N,\theta,\phi_0}[i+1] - \xi_{N,\theta,\phi_0}[i] = -\lfloor \Delta_-\xi \rfloor \text{ or } -\lceil \Delta_-\xi \rceil. \tag{14}$$

$\xi_{N,\theta,\phi_0}[i]$ normally increases or decreases by about $\min\{\Delta_+\xi, \Delta_-\xi\}$, and occasionally decreases or increases by about $\max\{\Delta_+\xi, \Delta_-\xi\}$. This result indicates the detection error appears recursively.

4.2. The case where $\theta > 1$

For $N \in \mathbb{Z}_{\geq 1}$, $\theta > 1$, and $0 \leq \phi_0 < \theta$, define $\eta_{N,\theta,\phi_0} \in \mathbb{R}^{\mathbb{Z}}$ as

$$\eta_{N,\theta,\phi_0}[i] = \min \left\{ \left\lceil \frac{n - \psi_{N,\theta,\phi_0}[i]/\theta}{1 - 1/\theta} \right\rceil - 1 \,\middle|\, n \in \mathbb{Z} \wedge \left\lceil \frac{n - \psi_{N,\theta,\phi_0}[i]/\theta}{1 - 1/\theta} \right\rceil - 1 \geq 0 \right\}. \tag{15}$$

From Property 1, $\eta_{N,\theta,\phi_0}[i]$ implies the bit number at which the first detection error after $t_i = 0$ occurs. Substituting Eq. (7) into Eq. (15), we obtain the following form of $\eta_{N,\theta,\phi_0}[i]$:

$$\eta_{N,\theta,\phi_0}[i] = \left\lceil \left(1 - \left(\frac{\phi_0 - iN}{\theta} \mod 1\right)\right) \frac{\theta}{\theta - 1} \right\rceil - 1. \quad (16)$$

Letting

$$\Delta_+\eta = \left(1 - \left(-\frac{N}{\theta} \mod 1\right)\right) \frac{\theta}{\theta - 1}, \quad (17)$$

$$\Delta_-\eta = \left(-\frac{N}{\theta} \mod 1\right) \frac{\theta}{\theta - 1}, \quad (18)$$

we obtain

$$\eta_{N,\theta,\phi_0}[i+1] = \begin{cases} \left\lceil \left(1 - \left(\frac{\phi_0 - iN}{\theta} \mod 1\right)\right) \frac{\theta}{\theta - 1} - \Delta_-\eta \right\rceil - 1 \\ \quad \text{if } \left(\frac{\phi_0 - iN}{\theta} \mod 1\right) + \left(-\frac{N}{\theta} \mod 1\right) < 1, \\ \left\lceil \left(1 - \left(\frac{\phi_0 - iN}{\theta} \mod 1\right)\right) \frac{\theta}{\theta - 1} + \Delta_+\eta \right\rceil - 1 \\ \quad \text{if } \left(\frac{\phi_0 - iN}{\theta} \mod 1\right) + \left(-\frac{N}{\theta} \mod 1\right) \geq 1. \end{cases} \quad (19)$$

Thus, we obtain the following:

$$\eta_{N,\theta,\phi_0}[i+1] - \eta_{N,\theta,\phi_0}[i] = -\lfloor \Delta_-\eta \rfloor \text{ or } -\lceil \Delta_-\eta \rceil \quad (20)$$

if $\left(\frac{\phi_0 - iN}{\theta} \mod 1\right) + \left(-\frac{N}{\theta} \mod 1\right) < 1$ holds; otherwise, we obtain the following:

$$\eta_{N,\theta,\phi_0}[i+1] - \eta_{N,\theta,\phi_0}[i] = \lfloor \Delta_+\eta \rfloor \text{ or } \lceil \Delta_+\eta \rceil. \quad (21)$$

Therefore, $\eta_{N,\theta,\phi_0}[i]$ normally increases or decreases by about $\min\{\Delta_+\eta, \Delta_-\eta\}$, and occasionally decreases or increases by about $\max\{\Delta_+\eta, \Delta_-\eta\}$. This result indicates the detection error appears recursively.

5. Discussion with a Concrete Example

In this section, we reproduce the temporal change of the packet arrival point through a concrete example. We consider a router which has two outputs α and β. The router dispatches packets to the output α or β according to the algorithm of reading header shown in Fig. 2. Let the identical packets with length $N = 100$ bit be repeatedly inputted into the router. Each packet's header is "101110", payload's length is 85 bit, and footer is "001101000". The header is designed to dispatch the packet to the output α. Let $6/7 < \theta < 1$ for simplicity. Under this condition, clock rises 6 or 7 times in 6-bit header, so that detection error occurs less than once in each header. In addition, the state in Fig. 2 is reset to S_0 at each packet's end as a result of reading the end of the packet "000" more than 3 times.

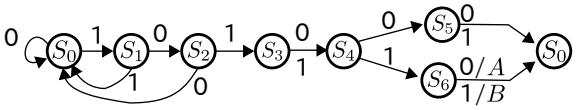

Figure 2: The algorithm of reading header. The command A makes the router dispatch the packet to the output α, while the command B makes the router dispatch the packet to the output β.

Table 1: The 0-th~10-th bits of detected signal and the corresponding packet arrival point for each value of $\xi_{N,\theta,\phi_0}[i]$. The payload is detected as "1" at each rising edge.

$\xi_{N,\theta,\phi_0}[i]$	Detected signal	Packet arrival point
0	11011101111	β
1	10011101111	β
2	10111101111	β
3	10111101111	β
4	10111101111	β
5	10111001111	α
>5	10111011111	α

Table 2: The 0-th~20-th values of ξ_{N,θ,ϕ_0} with $\phi_0 = 0$.

θ	0-th~20-th values of ξ_{N,θ,ϕ_0}
0.91	**0 1 2 3 4** 5 6 7 8 10 **1 2 3 4** 5 6 7 8 9 **0 2**
0.95	**0** 14 9 **4** 18 13 8 **3** 17 12 7 **2** 16 11 6 **1** 15 10 5 **0** 14

Tab. 1 shows detected signal of the i-th packet and the corresponding packet arrival point for each value of $\xi_{N,\theta,\phi_0}[i]$. According to Tab. 1, the i-th packet does not appear at the original destination α but the output β if $\xi_{N,\theta,\phi_0}[i] \in \{0, 1, \cdots, 4\}$. Tab. 2 shows the values of ξ_{N,θ,ϕ_0} with $\theta = 0.91, 0.95$ and $\phi_0 = 0$, where the highlighted values in $\{0, 1, \cdots, 4\}$ correspond to the packet which appears at the output β. We find about 5 out of 10 packets arrive at the output β in the case of $\theta = 0.91$ and about 1 out of 4 packets arrive at the output β in the case of $\theta = 0.95$. The result implies the temporal change of the packet arrival point.

6. Concluding Remarks

In this paper, we discussed an unexpected transfer of power packets under out-of-synchronization condition. Assuming that the bit length and the clock period are constant and the identical packets are successively given to the router, it is clarified that the destination failure appears recursively. The result is explained in the relationship to the detection error caused by synchronization failure in the power packet dispatching system.

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