

Inter-connection of Parallel Connected Class D Amplifiers Operated at Different Switching Frequencies

Yusuke Ishikawa[†], Ryuta Yamamoto[†], Hiroyuki Uchiyama[†], Xiuqin Wei[‡], Hiroo Sekiya[‡], and Tadashi Suetsugu[†]
[†]Department of Electronics Engineering and Computer Science
 Fukuoka University, Fukuoka, Japan
[‡]Chiba University, Chiba, Japan
 suetsugu@fukuoka-u.ac.jp

Abstract—This paper researches about influence of multi-frequency operation of parallel connected class D amplifiers. It can be seen that variation in dc supply voltage of one amplifier leg does not influence to output waveform of another amplifier leg. However, parallel connection of two amplifiers influences output power of both amplifiers due to change in impedance of output filter. It is proposed to insert decoupling filter to the output of higher frequency amplifier to reduce the coupling. It is shown that decoupling filter successfully improved coupling between amplifiers.

I. INTRODUCTION

Class D amplifier is one of next generation power source for plasma generator due to its high efficiency characteristics [1][2]. In the plasma generators, RF power is often imposed with combination of several frequency components. For

example, an RF generator for semiconductor processing inputs 2 MHz and 13.56 MHz RF power to the chamber [3]. In order to impose RF powers with several frequencies, several power amplifiers with different operating frequencies are operated in parallel. If power amplifiers are connected in parallel, there is electric coupling between the amplifiers. Operation of class D amplifier [4] is strongly influenced by condition of load impedance. It is important to investigate the influence of parallel operation of amplifiers with different frequencies. However, this influence is not well researched for class D amplifiers yet. In this paper, parallel connected two class D amplifiers which are operated at different frequencies is simulated with PSPICE to obtain influence of coupling of different frequencies.

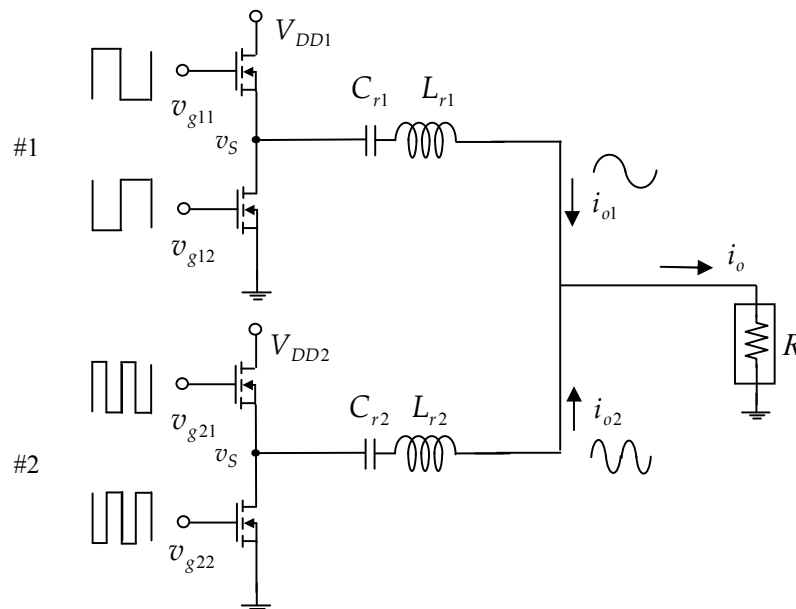


Fig. 1. Parallel connected class D amplifier with different operating frequencies.

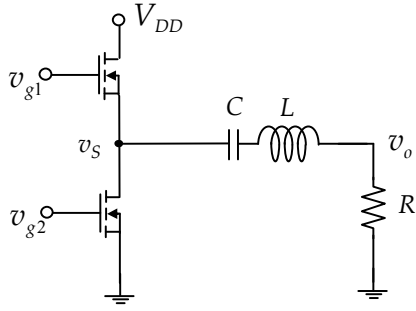


Fig. 2. Basic circuit of the class D amplifier.

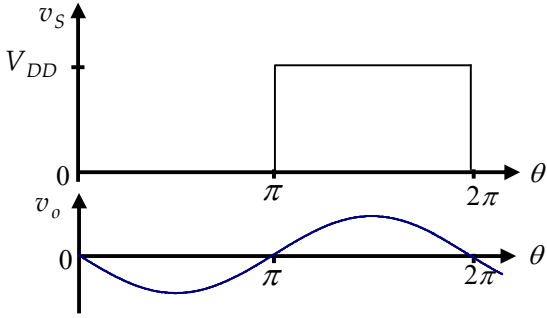


Fig. 3. Theoretical waveforms of switch voltage and output current.

II. PARALLEL CONNECTED CLASS D AMPLIFIERS WITH DIFFERENT OPERATING FREQUENCIES

Parallel connected class D amplifier analyzed in this paper is shown in Fig. 1. Two class D amplifiers with different operating frequencies are connected in parallel. One leg of class D amplifier is a voltage switching type class D amplifier shown in Fig. 2. The class D amplifier is composed of dc supply voltage V_{DD} , two MOSFET transistor switches, output resonant LC filter $C-L$, and load resistance R . The output LC filter $C-L$ has a high loaded quality factor and a resonant frequency f_o near the switching frequency f so that the output current can be pure sinusoid at the switching frequency. The MOSFET transistors switch in turn periodically and it produce rectangular voltage excitation at drain voltage v_s . The output LC filter $C-L$ extracts the fundamental frequency component of drain voltage and output to the load resistance R .

Fig. 3 shows drain voltage waveform and output voltage waveform of the class D amplifier. When the duty ratio is 0.5, the circuit parameters are [2]

$$R = \frac{2V_{DD}^2 \cos^2 \varphi}{\pi^2 P} \quad (1)$$

$$C = \frac{1}{\omega_o QR} \quad (2)$$

$$L = \frac{QR}{\omega_o} \quad (3)$$

where P is output power (100% power efficiency is supposed), φ is phase angle of output current, Q is loaded quality factor of output LC filter, and ω_o is

$$\omega_o = 2\pi f_o = \frac{4\pi f}{\frac{\tan \varphi}{Q} + \sqrt{\frac{\tan^2 \varphi}{Q^2} + 4}} \quad (4)$$

In general f_o is set to less than f in order to ensure inductive load current in transistor. If $\varphi = 30 \text{ deg}$, $V_{DD} = 250 \text{ V}$, $P = 190 \text{ W}$, and $Q = 10$ at 13.56 MHz, circuit parameters are calculated as follows; $C = 24.2 \text{ pF}$, $L = 6.0 \text{ } \mu\text{F}$, and $R = 50 \text{ } \Omega$. And at 27.12 MHz, $C = 12 \text{ pF}$, $L = 3 \text{ } \mu\text{F}$, and $R = 50 \text{ } \Omega$. At 40.68 MHz, $C = 8 \text{ pF}$, $L = 2 \text{ } \mu\text{F}$, and $R = 50 \text{ } \Omega$. At 60.00 MHz, $C = 5.5 \text{ pF}$, $L = 1.4 \text{ } \mu\text{F}$, and $R = 50 \text{ } \Omega$.

III. SIMULATION RESULTS

In the simulation, 3 circuits who have different patterns of frequency combinations were tested; they are (1) 13.56 MHz + 27.12 MHz, (2) 13.56 MHz + 40.68 MHz, and (3) 13.56 MHz + 60.00 MHz. Simulated circuit has $50 \text{ } \Omega$ load resistance. In this simulation, IXYS DEI375-102N12A was used for MOSFET.

In the first, supply voltage of leg #1, V_{DD1} was varied from 0 V to 250 V. Fig. 4 shows time domain waveforms of drain voltage of S1 v_{S1} , drain voltage of S2 v_{S2} , and output voltage v_o when leg #1 was operated at 13.56 MHz and leg #2 was operated at 27.12 MHz. It can be seen waveform of v_{S1} was proportional to V_{DD1} . However, waveform of v_{S2} was not varied with V_{DD1} . Waveform of output current i_o was superimposing of two different frequency sinusoids. Fig. 5 shows FFT of waveforms in Fig. 4. It can be seen that spectrum of v_{S1} has third harmonic component but does not have second harmonic component. Therefore, there is very low influence between v_{S1} and v_{S2} . It can be also seen that on frequency component of i_o at 13.56 MHz varied with V_{DD1} . But, frequency component at 27.12 MHz was not varied with V_{DD1} . Namely, input voltage (input power) of low frequency component did not influence to the output power of high frequency component when 13.56 MHz and 27.12 MHz were imposed.

Same simulations were done for circuit (2) and (3). Fig. 6 shows plots of FFT results of (a) 13.56 MHz components and (b) 27.12 MHz, 40.56 MHz, and 60.00 MHz components of output current i_o of (1), (2), and (3) circuits. As seen in Fig. 6(a), 13.56 MHz component was proportional to V_{DD1} . (Some plots were not obtained due to PSpice convergence problem.) From Fig. 6(b), it can be seen that frequency components at 27.12 MHz, 40.56 MHz, and 60.00 MHz did not varied with V_{DD1} . These two plots indicate that variation of input voltage

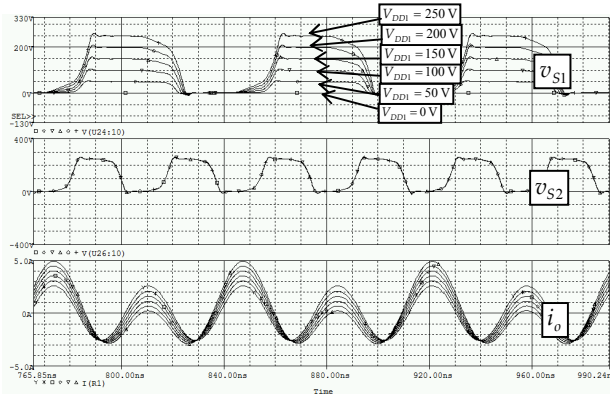


Fig. 4. Simulated waveforms drain voltage of S1 v_{S1} , drain voltage of S2 v_{S2} , and output voltage v_o when leg #1 was operated at 13.56 MHz and leg #2 was operated at 27.12 MHz, for selected values of V_{DD1} .

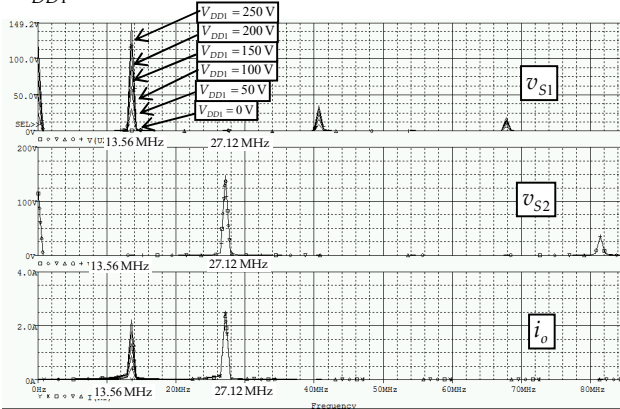
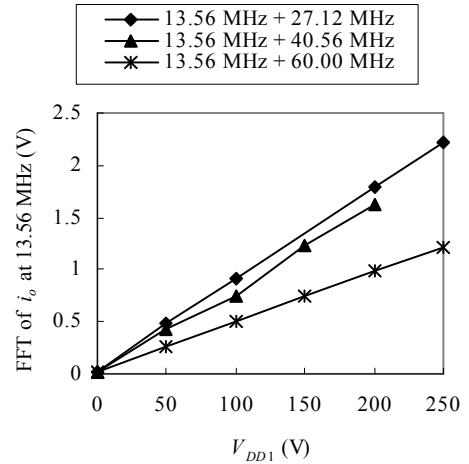


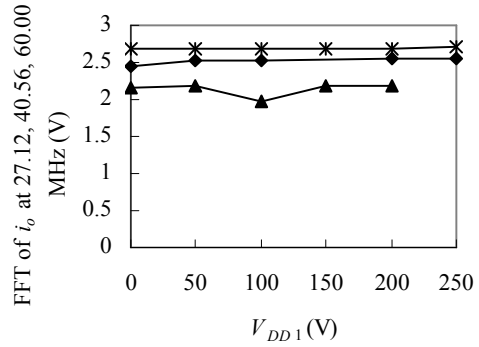
Fig. 5. FFT results of drain voltage of S1 v_{S1} , drain voltage of S2 v_{S2} , and output voltage v_o when leg #1 was operated at 13.56 MHz and leg #2 was operated at 27.12 MHz, for selected values of V_{DD2} .

V_{DD1} for 13.56 MHz did not influence to output power of other amplifier leg. However, three plots in Fig. 6(a), i.e., 13.56 MHz + 27.12 MHz, 13.56 MHz + 40.56 MHz, and 13.56 MHz + 60.00MHz, have different values. This difference is due to change in impedance of output filter of amplifier #1. Namely, connection of amplifier #2 influences impedance of output filter seen from amplifier #1.

Similar simulation were done for variation of V_{DD2} . Fig. 7 shows plots of FFT results of (a) 13.56 MHz components and (b) 27.12 MHz, 40.56 MHz, and 60.00 MHz components of output current i_o of (1), (2), and (3) circuits when V_{DD2} was varied from 0 V to 250 V. From Fig. 7(a), it can be seen that frequency components at 13.56 MHz did not varied with V_{DD2} . This plot indicates that variation of input voltage V_{DD2} did not influence to output power of other amplifier leg.



(a)



(b)

Fig. 6. FFT results of (a) 13.56 MHz components and (b) 27.12 MHz, 40.56 MHz, and 60.00 MHz components of output current i_o of (1), (2), and (3) circuits, versus V_{DD1} .

IV. REDUCTION OF COUPLING BETWEEN PARALLEL CONNECTED AMPLIFIERS

In order to reduce coupling between parallel connected amplifiers, it is proposed to insert decoupling filter to the output of one amplifier which has higher output frequency. Fig. 8 shows proposed circuit which has decoupling filter. Decoupling filter is a band cut filter which has notch frequency 13.56 MHz, i.e., output frequency of amplifier #1. Fig. 9 shows FFT results of 13.56 MHz component of output current i_o of improved circuits. In this simulation, values of decoupling filter were $C_C = 23\text{pF}$, $L_C = 6\ \mu\text{F}$. Comparing with Fig. 6(a), difference between three plots are reduced.

V. CONCLUSIONS

This paper influence of multi-frequency operation of parallel connected class D amplifiers were researched. It can be seen that variation in dc supply voltage of one amplifier leg does not influence to the output waveform of another amplifier.

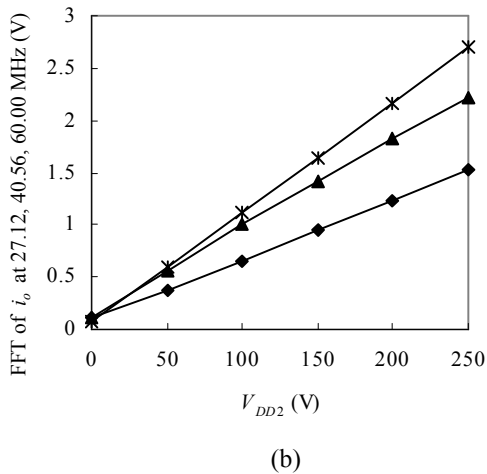
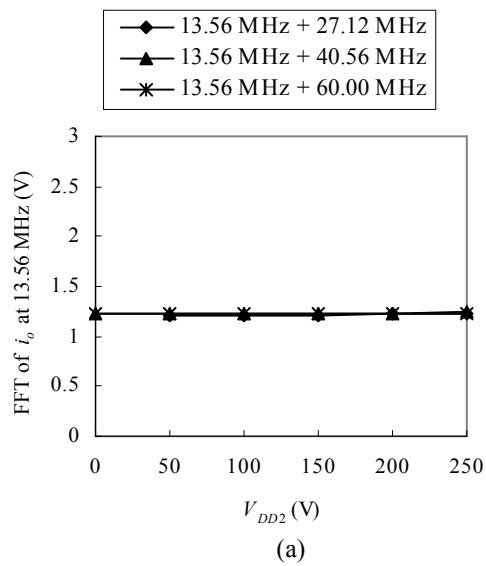


Fig. 7. FFT results of (a) 13.56 MHz components and (b) 27.12 MHz, 40.56 MHz, and 60.00 MHz components of output current i_o of (1), (2), and (3) circuits, versus V_{DD2}

However, parallel connection of two amplifiers influence output power of both amplifiers due to change in impedance of output filter. It was proposed to insert decoupling filter to the output of higher frequency amplifier to reduce the coupling. It was seen that decoupling filter successfully improved coupling between amplifiers.

VI. REFERENCE

- [1] Robert Porter and Michael Mueller, "Method and Apparatus for Stabilizing Switch-Mode Powered RF Plasma Processing," US Patent 5747935, 1998.
- [2] John Evans and Patrick Pribyl, "Plasma Production Device and Method and RF Driver Circuit," US Patent 7132996, 2006.

- [3] H. Nagahama, "Effect of Applying Two Kinds of R.F. Fields on Capacitively Coupled R.F. Discharges with ring-like Electrodes," Research Bulletin of Fukui University of Technology, Vol. 35, pp.15-21, 2005. (in Japanese)
- [4] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, New York: John Wiley & Sons, Inc., 1995.

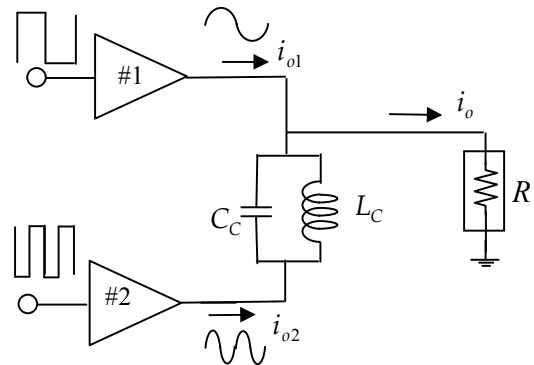


Fig. 8. Improved parallel connected class E amplifier with different operating frequencies.

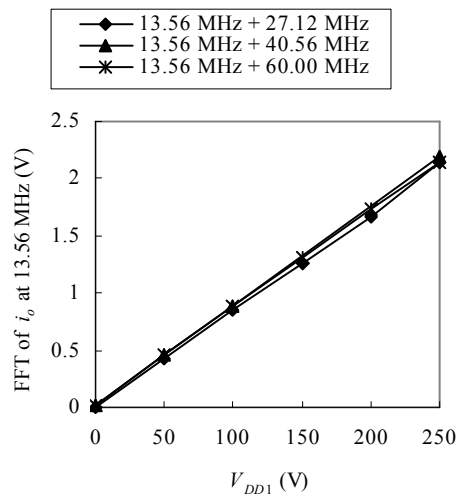


Fig. 9. FFT results of (a) 13.56 MHz components and (b) 27.12 MHz, 40.56 MHz, and 60.00 MHz components of output current i_o of improved circuits, versus V_{DD1} .