Characteristic of On-Chip Dipole Antennas Considering Conductive layer on the Surface of Silicon Substrate

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Abstract

The EM modeling for silicon substrate was discussed for on-chip dipole antenna. It was found that the effect of Conductive layer is very large and it must be modeled in the EM simulation. The calculated reflection considering Conductive layer is closer to the measured one.

Keywords : On-chip dipole antenna, Millimeter-wave, CMOS substrate, Conductive layer, electromagnetic modeling

1. Introduction

Recent progress in silicon CMOS technology realizes the high speed MOSFET [1]. The CMOS technology can be applied to chips for wireless systems at 60GHz band. On-chip antennas on a CMOS chip are highly desired for mass-production at low cost. It is also important to reduce connection loss between the CMOS chip and the antenna. On-chip antennas have been studied by many researchers [2]-[4]. However, electromagnetic (EM) modeling, especially for the surface of the CMOS chip, has not been investigated well.

In this paper, on-chip dipole antennas are studied by measurement and simulation. There are highly conductive materials on the surface of the silicon substrate of the CMOS chip, such as wells and Conductive layer which are compounds that have silicon and metals. The EM modeling for silicon substrate is discussed in this paper, and the results are compared by measured one.

2. Structure of On-Chip Dipole Antenna

Figure 1 shows the structure of the on-chip dipole antenna. The Length of the dipole antenna is L1. A silicon chip is 5mm square and the thickness of silicon substrate is 400 μm. Relative permittivity and conductivity of the silicon substrate are 11.9 and 100 S/m, respectively. The thickness of the Conductive layer t is very thin, typically around 400 nm up to 1000 nm. The material of metals is aluminum and they are supported by SiO_2 insulator. There is passivation on the top surface of the chip. Figure 2(a) shows the micrograph of the fabricated on-chip dipole antenna with a pad for 100 μm-pitch GSG probe. Figure 2(b) shows the analysis model for Figure 2(a).

3. Results

The finite element method (FEM) based EM simulator, Ansoft HFSS Ver.11, is used for simulation throughout the paper. The lamped port with 50Ω internal impedance is used for source modeling.

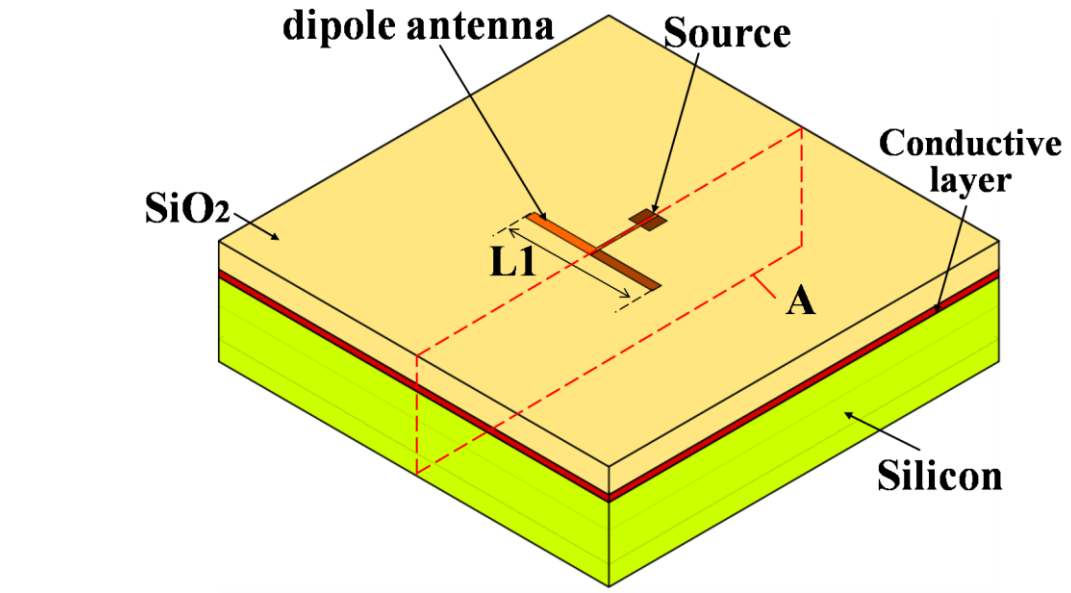
Figure 3 shows frequency characteristic of reflection coefficient (L1=840μm). Figure 3 (a) shows and the variation of conductivity of Conductive layer when t=400 nm. The amplitude of the

reflection becomes larger as the conductivity increases. Typical conductivity of Conductive layer is around 10×10^4 S/m, and it is shown that Conductive layer must be considered in EM modeling although it is electrically very thin. The calculated result considering Conductive layer is closer to the measured one. Figure 3 (b) shows and the variation of thickness of Conductive layer when conductivity of Conductive layer is 10×10^4 S/m. The amplitude of reflection increases as the thickness of Conductive layer increases. The calculated radiation efficiency without Conductive layer is 0.404% and that with Conductive layer (conductivity: 10×10^4 S/m, t=800 nm) is 0.025%.

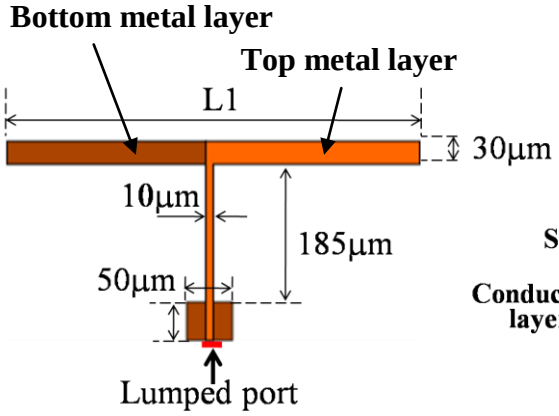
Figure 4 shows frequency characteristic of reflection coefficient (L1=2200 μm). Similar results as Fig. 3 are shown. The calculated radiation efficiency without Conductive layer is 0.277% and that with Conductive layer (conductivity: 12×10^4 S/m, t=800 nm) is 0.045%.

4. Conclusion

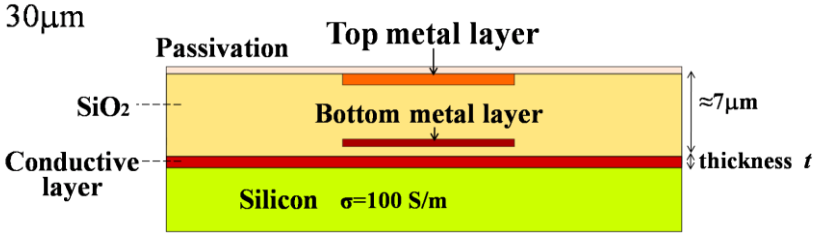
The EM modeling for silicon substrate was discussed for on-chip dipole antenna. It was found that the effect of Conductive layer is very large and it must be modeled in the EM simulation. Further verification of EM modeling and radiation characteristic will be studied in future.



(a) Antenna structure

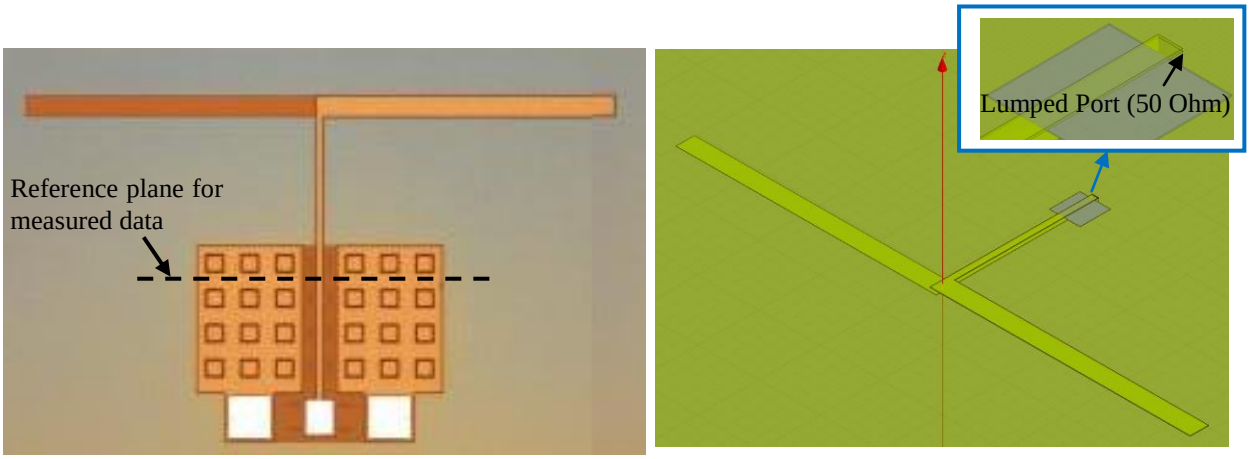


(b) Dipole antenna



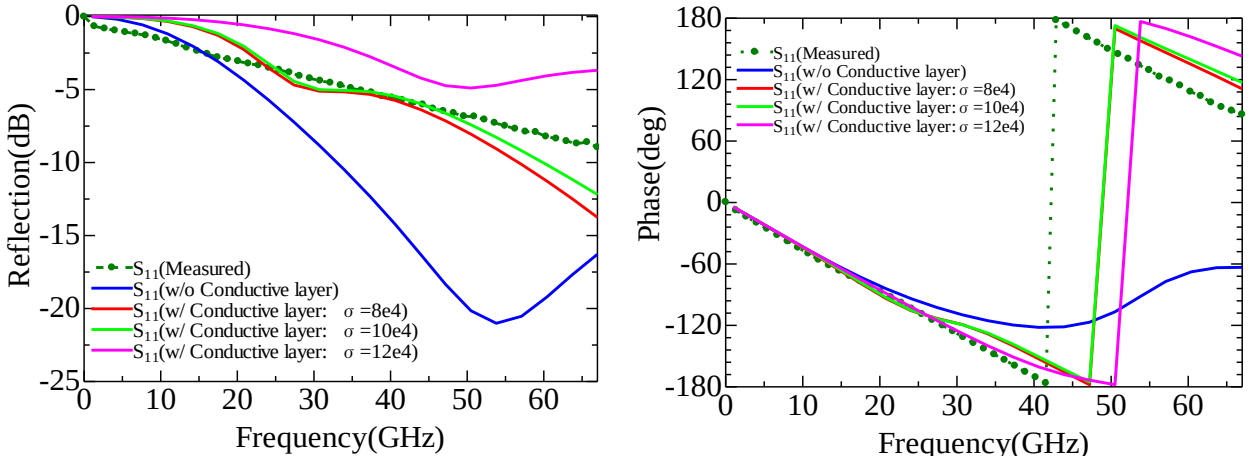
(c) Cross-sectional view(plane A in (a))

Figure 1: Structure of the on-chip dipole antenna

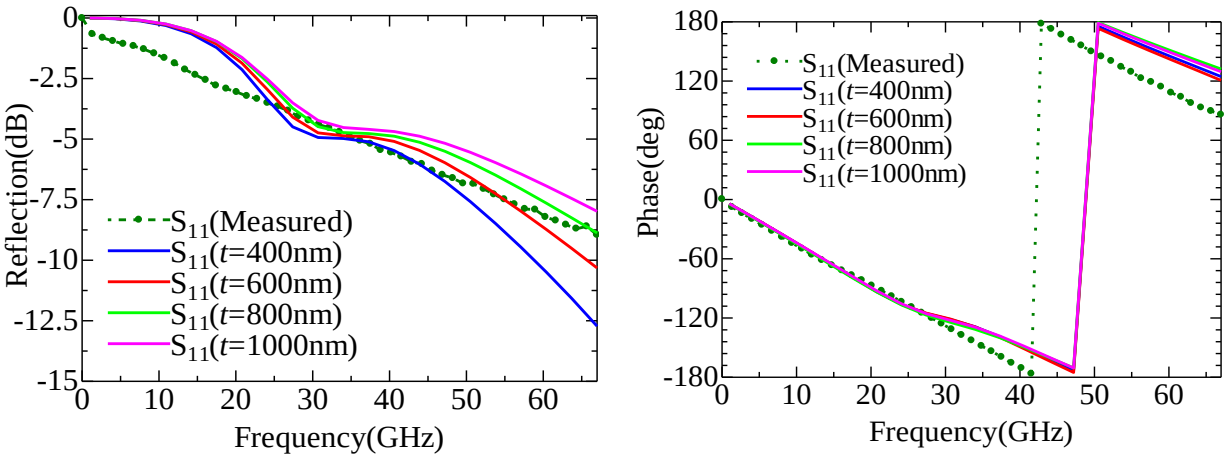


(a) Micrograph (b) Analysis model

Figure 2: Micrograph and analysis model of the silicon on-chip dipole antenna on a silicon CMOS substrate

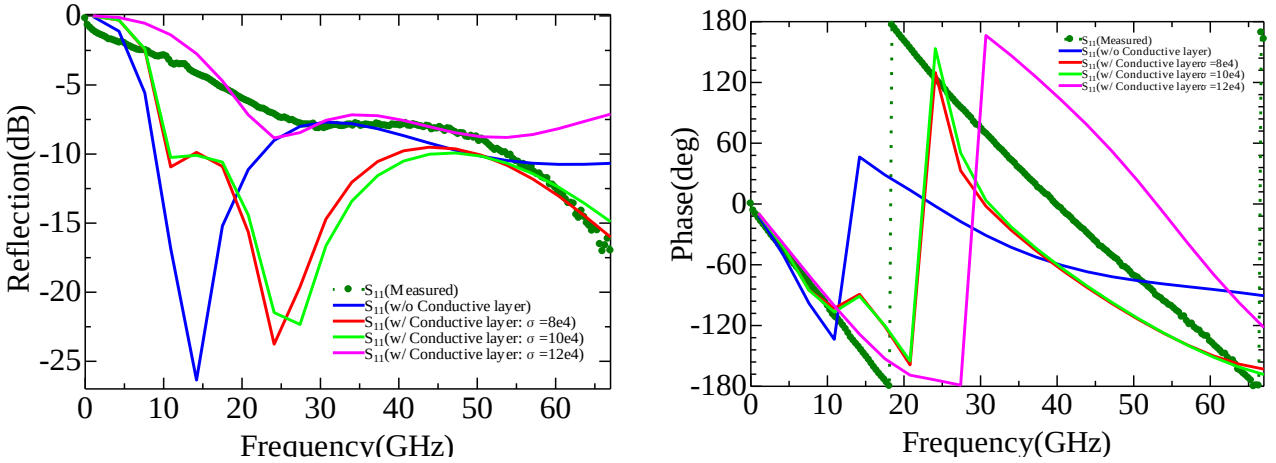


(a) Variation of conductivity of conductive layer (t=400 nm)

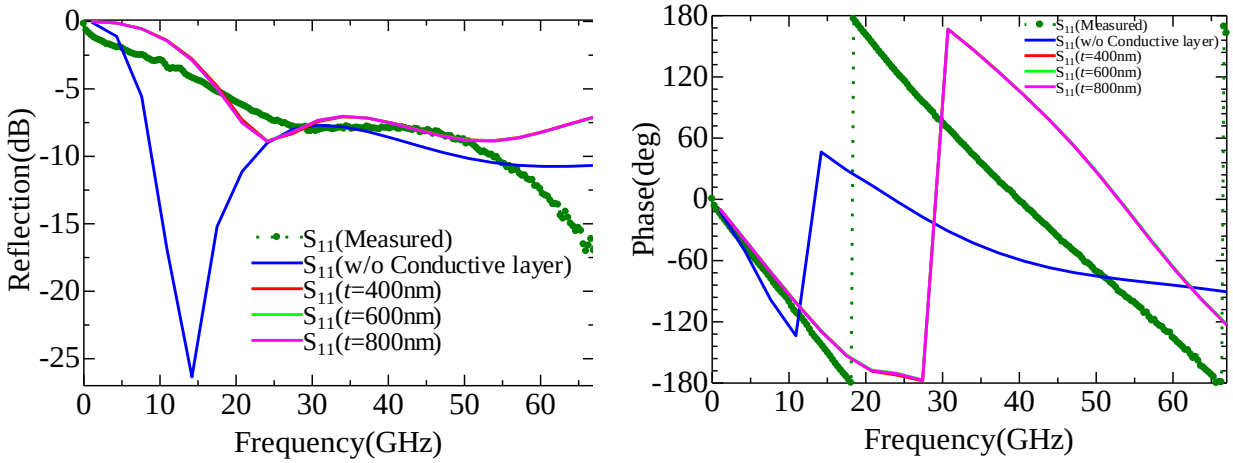


(b) Variation of thickness t (conductivity of conductive layer: 10×10^4 S/m)

Figure 3: Frequency characteristic of reflection coefficient (L1=840 μm)



(a) Variation of conductivity of conductive layer (t=400 nm)



(b) Variation of thickness t (conductivity of conductive layer: 12×10^4 S/m)

Figure 4: Frequency characteristic of reflection coefficient (L1=2200 μm)

Acknowledgments

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