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Studies on Couplings of SET Ring Oscillators for In-Phase Oscillation and Clock Distribution

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Abstract—Coupling among ring oscillators constructed of single-electron tunneling (SET) junctions decreases their large phase noise. However, the coupled oscillators have a problem that their spatial phase pattern varies depending on the number of oscillators. In addition, coupling structures proposed in the past are not suitable for distributing clock signals to SET logic circuits. This paper presents two types of coupled ring oscillators. Coupled oscillators proposed at first oscillate in-phase independently of the number of the oscillators. Second coupled oscillators extend spatially to distribute clock two-dimmensionally. The circuit simulation shows that the presented circuits oscillate as intended.

1. Introduction

Ring oscillators have long been used in micro-processors and communication circuits. CMOS ring oscillators are sometimes coupled in order to make their oscillation frequency higher, to generate multi-phase clock set with small phase difference, and to decrease phase noise [1]. In addition to improve oscillator performances, the coupling technique is also applied as a clock distribution scheme on digital LSI chips. The scheme makes variation of distribution delay small [2].

Ring oscillators can be built of single-electron tunneling (SET) junctions. SET [3] is a probabilistic quantum effect. Therefore, their phase noise is large. Recently, it was reported that coupling SET ring oscillators decreased the phase noise [4] as coupling CMOS ring oscillators does. However, the nearest-neighbor coupling presented in [4] causes a few problems. One of them is that frequency and spatial phase pattern of the coupled SET ring oscillators depend greatly on the number of the oscillators. Moreover, in-phase oscillation can not be induced when the number is large. Another problem is that the presented coupling method connects oscillators one-dimensionally. Two-dimensional coupling is indispensable for clock distribution since clock distribution with long wiring influences the oscillation.

In this paper, we will present two structures of coupled SET ring oscillators for in-phase oscillation and two-dimensional clock distribution. The structures have a virtue that oscillation frequency and phase noise are almost independent of the number of oscillators. Circuit simulation of the presented coupled SET ring oscillators will be carried out to confirm their functions and evaluate their performances.

2. SET Logic Gates

Figure 1(a) shows a SET transistor and its gate voltage versus drain current characteristic. The current flow is caused by continuous single-electron tunneling. Figure 1(b) shows a dual-gate SET transistor. Applying voltage to another gate shifts its voltage-current characteristic horizontally as shown in the figure.

Let us take two dual-gate SET transistors through which drain currents flow at different gate voltage for NMOS and PMOS transistors. Then, a SET counterpart of a CMOS inverter is constructed as shown in Fig. 1(c) [5]. Adding input terminals to the inverter as presented in Fig. 1(d), we build a multi-gate SET inverter which functions as a NAND gate [4]. The same circuit can operate as a NOR gate by adjusting input capacitance values.

Another way to build NAND and NOR gates is to use linear threshold gate (LTG) [6] shown in Fig. 1(e). Generally, $(K_p + K_n)$-input LTGs with binary variables function as

$$y = \mathrm{Sign}(\sum_{i=1}^{K_p} x_{p,i} - \sum_{i=1}^{K_n} x_{n,i} - Th), \quad x_{p,i}, x_{n,i}, y \in \{+1, -1\} \tag{1}$$

By adjusting bias voltage V_b or capacitance C_b, its threshold level Th changes. Then, many different logic functions are realized with the LTGs. Since the LTG circuit is passive, the output of it can not drive several SET circuits in parallel. Thus, the inverter in Fig. 1(c) is connected at the output of the LTG as a driver circuit. The dual stage logic gate built of a LTG and an inverter may be slow in switching. However, its fun-in is smaller than that of the multi-gate inverter.

3. Nearest-Neighbor-Coupled SET Ring Oscillators

We construct nearest-neighbor-coupled ring oscillators as shown in Fig. 2 [4]. NAND-equivalent multi-gate inverters are employed in the oscillators. The nearest-neighbor

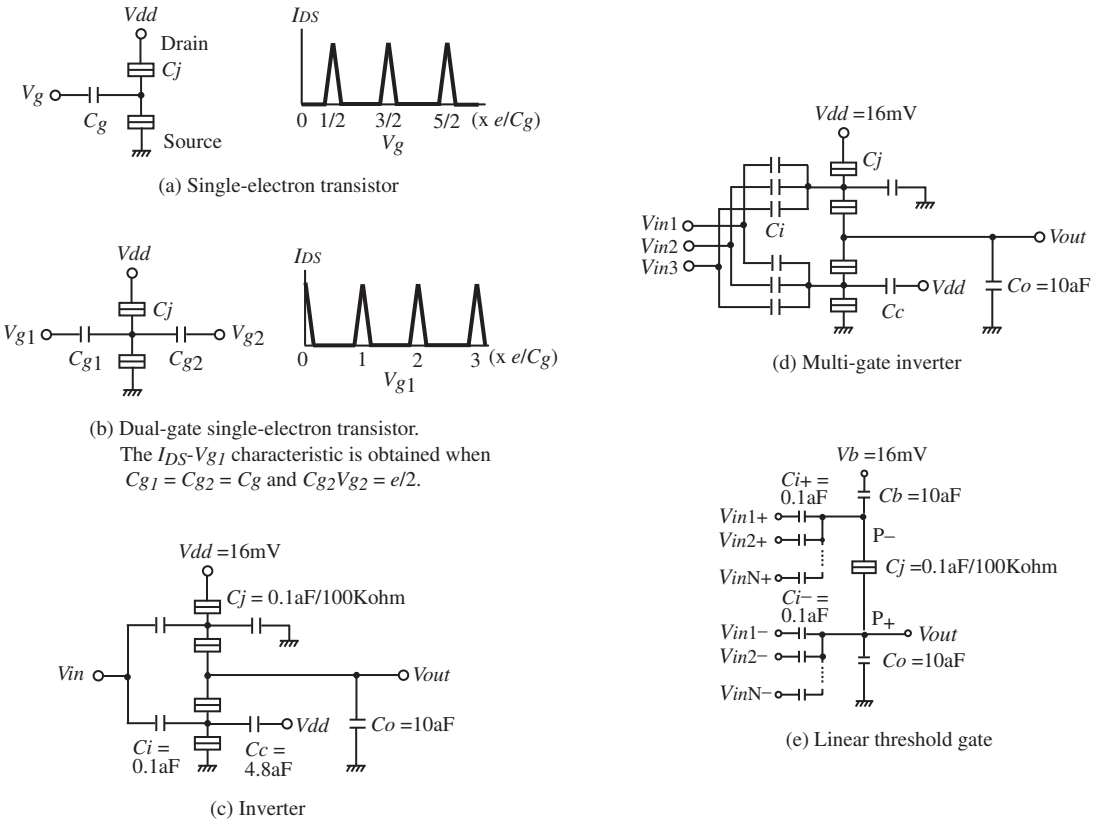

Figure 1: SET transistors, inverters and a linear threshold gate.

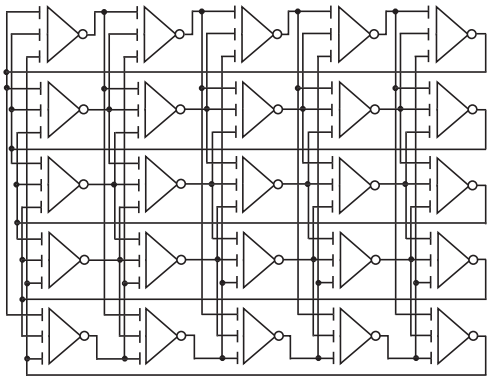

Figure 2: Nearest-neighbor-coupled SET ring oscillators ($N = 5$, $M = 5$).

coupling decreases phase noise. However, average oscillation frequency f_{avr} and average phase difference $\Delta\theta_{avr}$ between two adjacent oscillators vary depending on the number of coupled oscillators, as given by

$$\frac{1}{f_{avr}} = \frac{2NM}{M - 2N\,[M/2N]} \cdot \frac{1}{\Gamma} \tag{2}$$

and

$$\Delta\theta_{avr} = \frac{2\pi\,[M/2N]}{M} \tag{3}$$

where N, M denote the number of inverters used for one oscillator and the number of the coupled oscillators, and Γ^{-1} denotes switching delay of the inverters. In these equations, $[a]$ stands for the largest integer which does not exceed real or rational number a. From Eq. (2), we see that the oscillation frequency depends on the number of oscillators. From Eq. (3), it is found that the phase difference also depends on M and can not be zero if $M \geq 2N$.

4. Coupling for In-Phase Oscillation

Figure 3 shows coupled oscillators which oscillate in phase. They are built of LTG-based NAND gates with small fun-in because each gate output must be connected to three other gate inputs. Integers N and M in this section also denote the numbers of NAND gates and oscillators as defined in section 2. Integer N may take both even and odd number.

A nearest-neighbor coupling in the figure is the connections between an output of a gate at (i, j) and an input of a vertically adjacent gate at $(i, j - 1)$ or $(i, j + 1)$. Then, the two gates compose an SR-latch. When $M = 2$, the coupled

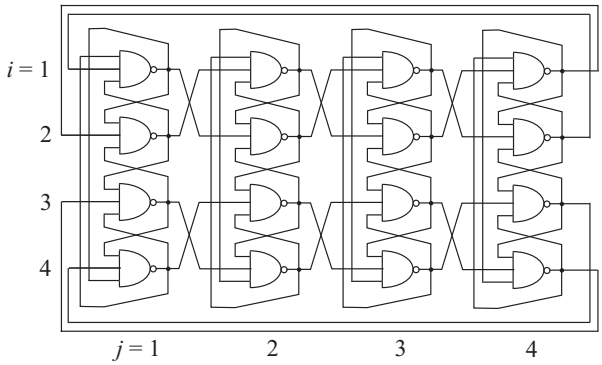

Figure 3: In-phase coupled SET ring oscillators ($N = 4$, $M = 4$).

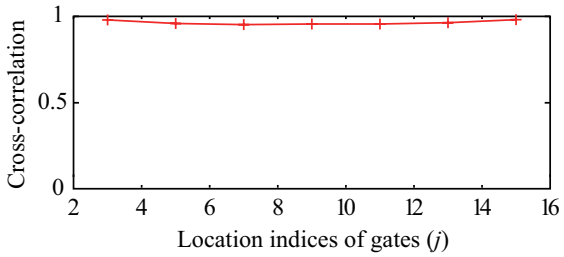

Figure 4: Cross-correlation between outputs of gates in in-phase coupled SET ring oscillators.

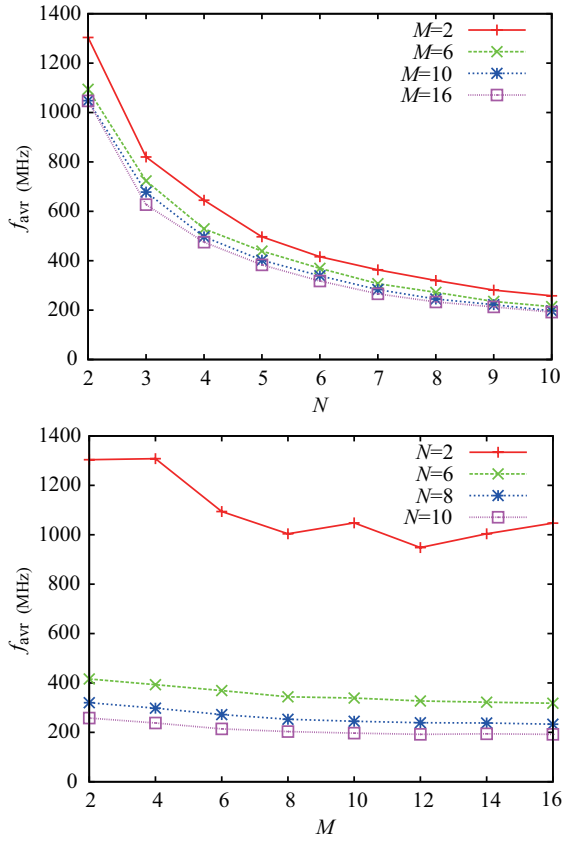

Figure 5: Average frequency f_{avr} of in-phase coupled SET ring oscillators.

oscillators are considered as a round-formed free-running N-stage shift register. Let us take up two shift registers from larger coupled oscillators with $M > 2$. One consists of NAND gates at $(i, j-1)$ and (i, j), $i \in \{1, 2, \cdots, N\}$. Another is built of NAND gates at (i, j) and $(i, j+1)$. Since the two SR-latches of two registers share a gate at (i, j), two gates at $(i, j-1)$ and $(i, j+1)$ switch at almost the same timing. Then, two logic signals go round in step on the two shift registers. In this way, the coupled oscillators achieve in-phase oscillation.

We evaluated some properties of the coupled in-phase oscillators by circuit simulation with SIMON [7]. Figure 4 shows cross-correlation between two outputs of gates at $(1, 1)$ and $(1, j)$, $j = 3, 5, \cdots, M-1$ when $N = 10$ and $M = 16$. The figure shows that phase difference between any two oscillators is small. Figures 5 and 6 show average oscillation frequency f_{avr} and standard frequency deviation divided by the average frequency σ_f / f_{avr} for the in-phase coupled oscillators of various network size, i.e., various N and M. We see that the frequency and the phase noise are almost independent of M when N is large.

5. Two-Dimensional Coupling

A two-dimensional oscillator network is constructed of SET ring oscillators built of $3(2n+1)$ inverters, $n = 0,1,2, \cdots$, as shown in Fig. 7. The figure presents a part of a network of oscillators with $n = 1$ and location indices (i, j), $i = 1, \cdots, M_h$, $j = 1, \cdots, M_v$.

We obtained average oscillation frequency and normalized standard frequency deviation of oscillator networks of various M_h and M_v by circuit simulation and show them in Table. 1. The normalized standard frequency deviation of a single ring oscillator is nearly 0.5 [4]. Then, we see that this type of coupling also decreases phase noise. In addition, it is also found that the dependency of the oscillation frequency on M_h and M_v is small.

6. Conclusions

This paper has presented two types of coupled SET ring oscillators. Coupled oscillators presented at first oscillate in phase and independently of the number of the oscillators. Second coupled oscillators extending two-dimensionally is suitable for clock distribution. Each oscillator can supply a clock signal of desired phase to its neighbor circuits. The oscillators presented first can also be coupled two-dimensionally to supply a clock set of both even and odd phases.

Our future works include theoretical analysis of the oscillation frequency and the phase noise of the two types of coupled oscillators.

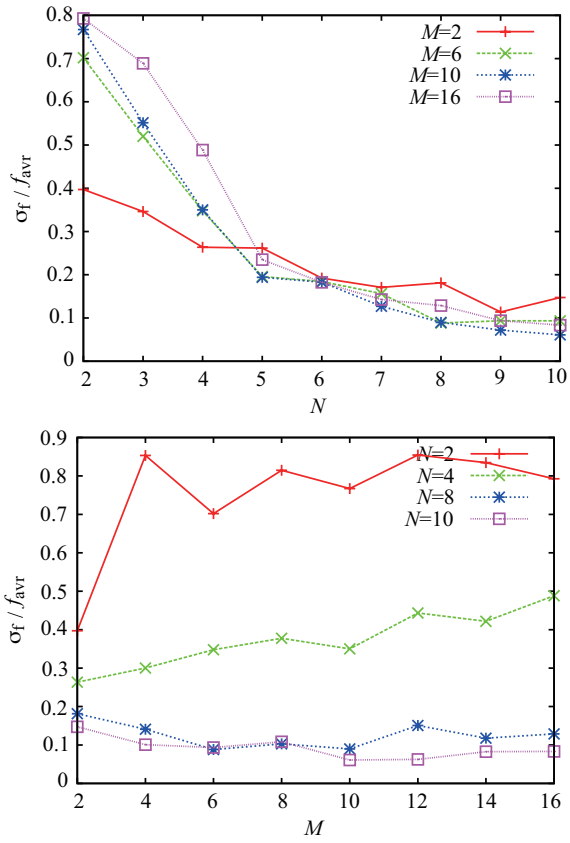

Figure 6: Normalized standard frequency deviation σ_f / f_{avr} of in-phase coupled SET ring oscillators.

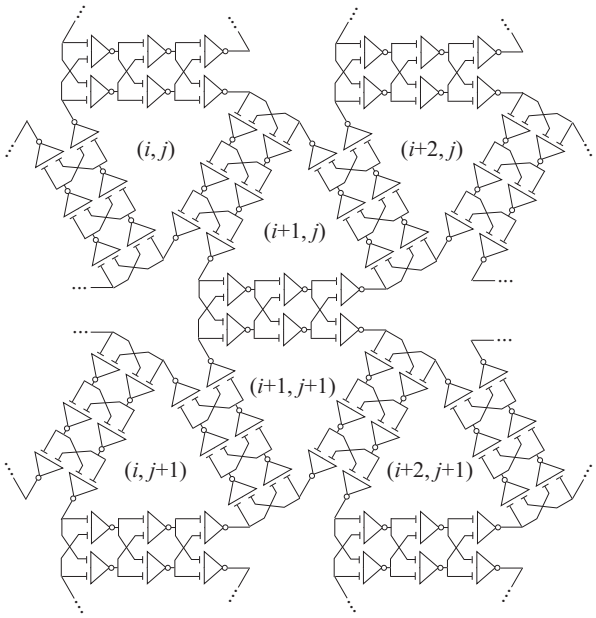

Figure 7: Two-dimensionally extended coupled SET ring oscillators.

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Table 1: Average frequency f_{avr} and normalized standard frequency deviation σ_f / f_{avr} of two-dimensionally extended coupled SET ring oscillators.

Frequency (MHz)		*Mh*	
		3	6
Mv	2	402	387
	4	383	372
	6	378	373

Normalized standard deviation		*Mh*	
		3	6
Mv	2	0.208	0.154
	4	0.181	0.147
	6	0.164	0.130