

# The Multi-Scale Method Combined to the GEC Modeling for the Study of Pre-Fractal Structures with Incorporated PIN Diodes

#MILI Sonia <sup>1</sup>, LARBI AGUILI Chiraz <sup>1</sup>, AGUILI Taoufik <sup>1</sup>

<sup>1</sup> SYS'COM Laboratory, National Engineering school of Tunis, ENIT  
 ENIT B.P 37 Le belvédère 1002 Tunis Tunisia, sonia.mili.sayah@gmail.com  
 ENIT B.P 37 Le belvédère 1002 Tunis Tunisia, Taoufik.aguili@enit.rnu.tn

## 1. Introduction

Since 1975 when Benoit Mandelbrot has defined fractals for the first time [1], many new shapes and applications for fractals continue to emerge [2]. The most well known examples are fractal-shaped antennas and frequency selective surfaces (FSS). Recently, PIN Diodes have been integrated in active FSS to obtain tunable frequency response [3-6]. Using classical methods, the study of such complex structures requires long CPU time and huge memory resources. When these structures contain fine details, the high aspect ratio leads to badly scaled matrices and convergence problems. In this paper, a multi-scale (MS) approach combined to the Generalized Equivalent Circuit (GEC) Modeling is applied to simplify the electromagnetic study of pre-fractal structures. The idea is to split the complex structure into sub-structures which are again split into smaller sub-structures until the smallest one is reached. For each sub-structure is associated a scale level and scale level 1 is attributed to the smallest sub-structure. The computation starts from scale level 1:  $N$  active modes illuminate the considered level in order to compute its surface impedance Matrix from which an impedance operator is deduced. The transition to the next level is done by replacing the previous level by its impedance operator. The previous steps will be done for each level till the highest one. In this paper, the MS-GEC technique is applied to compute the surface impedance of a pre-fractal structure with incorporated PIN diodes. The results of the MS-GEC method converge to those of the MoM method when a sufficient number of active modes are used at each scale level.

## 2. Description of the Multi-Scale approach

The multi-scale approach is based on the self similarity nature of studied structures. To explain the concept, the structure to be considered is depicted Fig. 1.

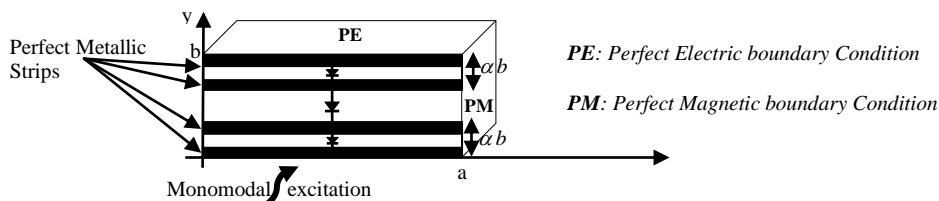


Figure 1: Cantor iris at scale 2 with incorporated PIN Diodes

The first step of the multi-scale (MS) method is to define the sub-domains. Once partitioned, the computation starts from the smallest scale level ( $s=1$ ) for which, convenient boundary conditions have to be considered. Next,  $N^i$  active modes of the contour enclosing the studied scale level  $S^i$  are used to compute the corresponding surface impedance matrix which will be converted to an impedance operator  $\hat{Z}_{S^i}$ . The transition to the next scale level  $S^{i+1}$  is done by replacing the previous scale level  $S^i$  by its impedance operator and so on. The number of active modes is an important criterion of the MS method since they describe the electromagnetic coupling between two subsequent levels: a precise  $\hat{Z}_{S^i}$  requires many active modes. In this paper, the accuracy of the MS method versus the MoM is evaluated with the number of active modes.

### 3. Application of the Multi-Scale approach

#### 3.1 Partitioning process

The considered structure of Fig. 1 is partitioned into sub-domains as shown in Fig. 2.

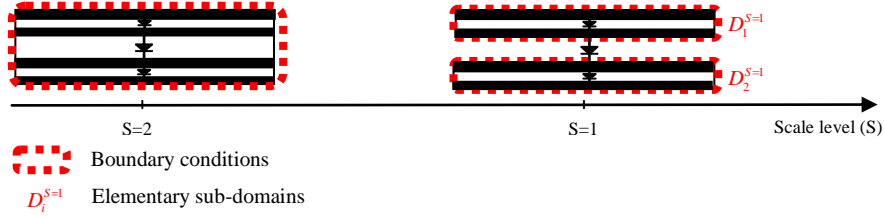


Figure 2: partitioning process

The structure is composed of two identical domains  $D_1^{S=1}$  and  $D_2^{S=1}$  called generator pattern. To apply the GEC approach, the incorporated PIN diodes have been modeled as detailed in section 3.2.

#### 3.2 PIN Diode

Fig. 3 shows the equivalent circuit models of a PIN Diode in forward and reverse bias modes [4]. Fig. 3(a) and (b) show the forward and the reverse bias equivalent circuits. Fig. 3(c) presents a converted series RLC reverse bias equivalent circuit. In this paper, the values used for forward bias are  $R = 5 \Omega$  and  $L = 0.4 \text{ nH}$ . For reverse bias, a capacitance  $C = 0.27 \text{ pF}$  is added.

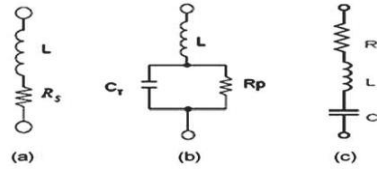


Figure 3: The PIN Diode (a) Forward bias equivalent circuit, (b) Reverse bias equivalent circuit, (c) Reverse bias equivalent series RLC circuit

According to its ON/OFF state, each PIN diode can be replaced by a surface impedance  $ZD$  of width  $w$  and height  $d$  expressed using its intrinsic (R, L, C) characteristics.

$$ZD = \begin{cases} \frac{w}{d}(R + jL\omega) & : \text{forward bias} \\ \frac{w}{d}\left(R + jL\omega - \frac{j}{C\omega}\right) & : \text{reverse bias} \end{cases} \quad (1)$$

#### 3.3 Multi-Scale Method

The steps needed to compute the surface impedance of the structure Fig.1 using the MS method are detailed in Fig. 4.

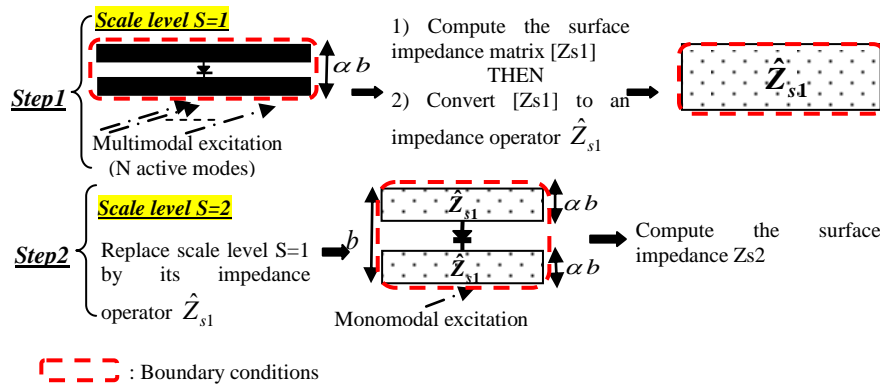


Figure 4: Illustration of the multi-scale method for the case of Cantor Iris at scale level2

### 3.4 Surface impedance of scale level 1

The sub-structure of scale level 1 is called the generator pattern. Its surface impedance matrix is computed using the Generalized Equivalent Circuit (GEC [7-11]) Model shown in Fig. 5.

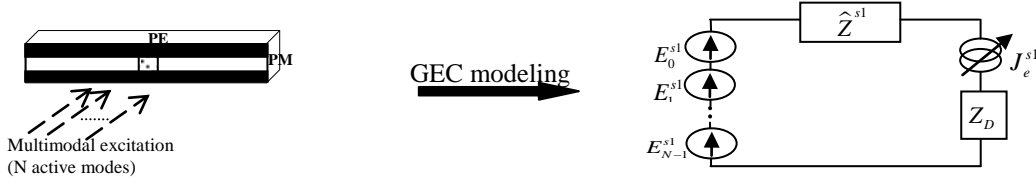


Figure 5: The generator pattern and its GEC

Let  $(f_m^{s1})$  be the local modal basis of the EMEM waveguide enclosing the generator pattern.

$E_i^{s1} = V_i^{s1} f_i^{s1}$  are the excitation sources where  $f_i^{s1}, i \in [0..N-1]$  represents the active modes useful to describe the coupling between two subsequent scale levels. The impedance operator  $\hat{Z}^{s1}$  is expressed as a function of higher-order modes. These localized modes are needed to describe the electromagnetic behavior within discontinuities.  $Z_D$  stands for the diode surface impedance localized in the diode domain. The problem's unknown  $J_e^{s1}$  is expressed as a series of known test functions  $g_p^{s1}$  weighted by unknown coefficients  $x_p^{s1}$ .  $J_e^{s1}$  exists along the metallic and the diode domains and is zero on the lossless dielectric domain. The surface impedance of scale level 1 is expressed Eq. 2.

$$Z_{S1} = \frac{1}{2} ([A][Z]^{-1}[A]^T)^{-1} \quad \text{where } [A] = \begin{bmatrix} \langle f_0^{s1} | g_p^{s1} \rangle \\ \langle f_1^{s1} | g_p^{s1} \rangle \\ \vdots \\ \langle f_{N-1}^{s1} | g_p^{s1} \rangle \end{bmatrix} \quad \text{and } [Z] = \begin{bmatrix} \langle g_p^{s1} | (\hat{Z}^{s1} + Z_D) g_q^{s1} \rangle \end{bmatrix} \quad (2)$$

### 3.5 Surface impedance of scale level 2

The surface impedance of scale level 2 is computed using the GEC depicted Fig. 7.  $E_0^{s2} = V_0^{s2} f_0^{s2}$  is the mono-modal excitation source where  $f_0^{s2}$  represents the first active mode. The surface impedance matrix  $Z_{S1}$  of the previous scale level is converted to an impedance operator  $\hat{Z}_{S1}$  expressed by  $\hat{Z}_{S1} = \sum_{i=1}^N \sum_{j=1}^N |f_{i-1}^{s1}\rangle Z_{S1}(i,j) \langle f_{j-1}^{s1}|$  where  $(f_j^{s1})$  are the active modes used in the previous scale level (scale level 1).

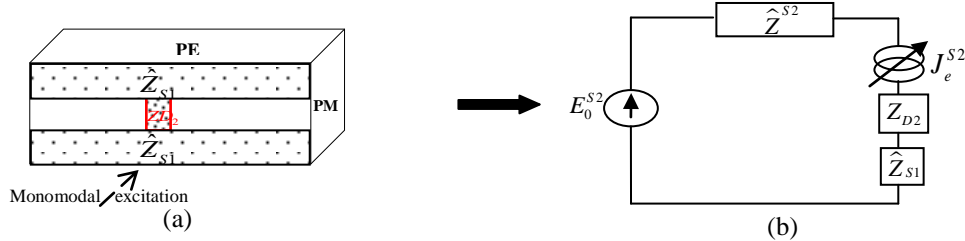


Figure 7: a) equivalent structure at scale level2, b) GEC of the equivalent scale level2

The impedance  $Z_{D2}$  is located in the PIN diode domain while the impedance operator  $\hat{Z}_{S1}$  is defined in  $D_1^1$  and  $D_1^2$  domains. The current  $J_e^{s2}$  exists all over  $D_1^1$ ,  $D_1^2$  and Diode domains.

The surface impedance expression of the equivalent structure Fig. 7.a) is given below:

$$Z_{S2\_MS} = \frac{1}{2} \left( \frac{1}{[A][Z]^{-1}[A]^T} \right) \quad \text{where } [A] = \begin{bmatrix} \langle f_0^{s2} | g_p^{s2} \rangle \end{bmatrix} \quad \text{and } [Z] = \begin{bmatrix} \langle g_p^{s2} | (\hat{Z}^{s2} + \hat{Z}_{S1} + Z_{D2}) g_q^{s2} \rangle \end{bmatrix} \quad (3)$$

## 4. Results

The surface impedance of the structure Fig.1 is computed using the MoM and the MS methods at 2.45GHz. Let  $\xi = \frac{Z_{S2\_MoM} - Z_{S2\_MS}}{Z_{S2\_MoM}} (\%)$  be the relative error between the two impedances. When using one active mode at scale level 1, the relative error is important: 23% for the real part and 11.7% for the imaginary part. In fact, one active mode is unable to fully describe the coupling between scale levels. To perform a better transition from a scale toward another, an accurate coupling needs to be computed by adding more active modes at lower scale levels.

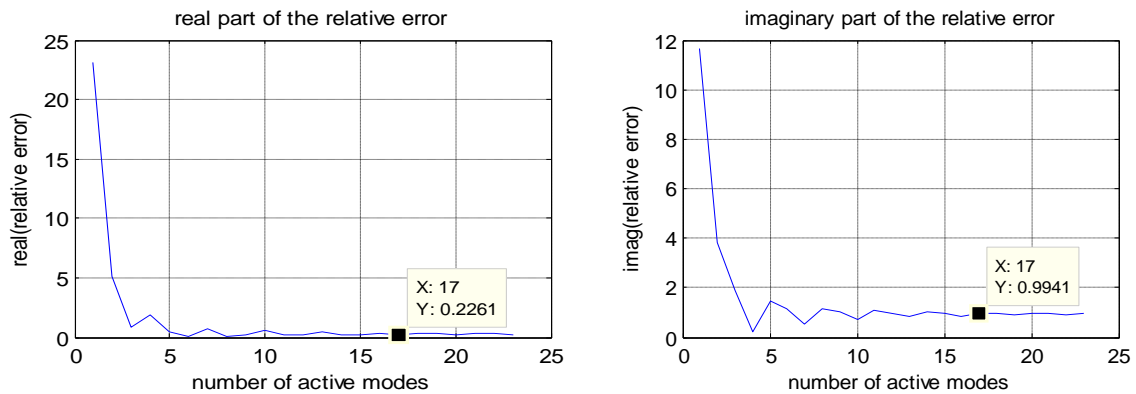


Figure 8: relative error variation with the number of active modes at lower levels  
Structure dimensions: a=10.2mm, b=22.9mm,  $\alpha = 1/3$ . f=2.45GHz, diode width=0.5mm, diode ON

Fig. 8 shows that the results obtained by the MS approach converge to those obtained by the MoM method when a sufficient number of active modes are used at each scale level. In our case, starting from 17 active modes, the relative error is less than 0.23% for the real part of the total surface impedance and less than 1% for the imaginary part.

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