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A gap-junction-connected silicon neuronal network

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Abstract—We developed a low-power consuming electronic circuit that is endowed with dynamics similar to a class of neurons whose gap-junction-connected networks can produce distinctive complex and synchronized behaviors (Class I*). The developed circuit was evaluated using circuit simulators and numeric calculation and indicated to have ability producing complex and synchronized behaviors very similar to them.

1. Introduction

The nerve system provides animals with intelligent and quick responses to both internal and external perturbations, powerful tools to maintain their homeostasis and survive in the environment. Electrical activity in the nerve system, which is believed to be playing crucial roles in such information processing ability, is mainly generated and controlled by the network of neuronal cells connected each other via synapses. The membrane potential in the neuronal cell is one of its sources and mediators. Each neuronal cell has capability to intrinsically produce spikes, pulse-like electrical activities, in its own rhythmical or chaotic dynamics. In the recent neuroscientific field, it is common understanding that various behaviors invoked by interaction between rhythmic and chaotic activities in neuronal cells mediated by synapses are the key to elucidate the mechanism under information processing in the nerve system. There exist various types of such behaviors including rhythmic patterns generated by motion pattern generator networks [1] and more complex ones in cerebral cortex that may contribute to higher functions.

The silicon neuron and synapse are electronic circuits that reproduce the electrical activity in the neuronal cell and the synapse. They are in most cases implemented using analog very-large-scale integrated (aVLSI) circuit technology to simulate the dynamics of the membrane potential in real time by more compact and lower-power consuming systems than current digital computers. The silicon neuronal network, a network of silicon neurons connected via silicon synapses, is expected to provide similar ability to neuronal networks by compact and low-power consuming circuits and thus be applied to implantable biomedical devices, real-time simulators of large-scale neuronal networks, brain-like information processing systems that can be integrated in such as mobile robots.

In this article, we focus on a model of an interneurons' network connected by gap junctions (GJs) [2]. The GJ is a tiny direct connection between the intracellular fluids of two neuronal cells, which is electrically a linear resister whose conductance depends on various factors including concentration of neuromodulators. This model is a simple GJ-connected network of a two-variable qualitative neuron model that belongs to Class I*, a subclass of Class I in the Hodgkin's classification [3]. It was reported to produce synchronized spiking, spatio-temporally chaotic behaviors, and complex alternation between them depending on the conductance of the GJs. This raised the possibility that GJ-connected interneuron networks are one of the sources of complex activities in the brain. We designed a network of Class I* silicon neurons connected via GJ circuits, which is expected to be an interneuron network subsystem in future possible "silicon brains" and a signal source with tunable complexity applicable for example to associative memories whose dynamics can be altered between switching and converging. In the next section, the circuitry, model, and simulation results of our silicon neuron and GJ are explained. Simulation results of a GJ-connected silicon neuronal network is reported in section 3.

2. A Class I* silicon neuron and a silicon GJ

2.1. Circuit and Model

In our previous works [4][5], we developed a design approach for silicon neuron models that allows construction of silicon-implementation-oriented qualitative neuron models. It is a solution to the inefficiency in the circuitries of the silicon neurons that originates from incompatibility between electrical characteristics of biological elements such as ionic channels and the transistors: copying complex dynamics in a neuronal cell requires complex circuitry [6], whereas realizing simple circuitry has to sacrifice compatibility of dynamics for example by introducing jump of the system state [7]. The basic idea of our approach is re-constructing the bifurcation and the phase-plane structures in an ordinary polynomial-based qualitative models into another model composed of the characteristics curve functions of elemental circuits.

Elemental circuits in our silicon neuron are differential pairs composed of Metal-Oxide-Semiconductor Field-

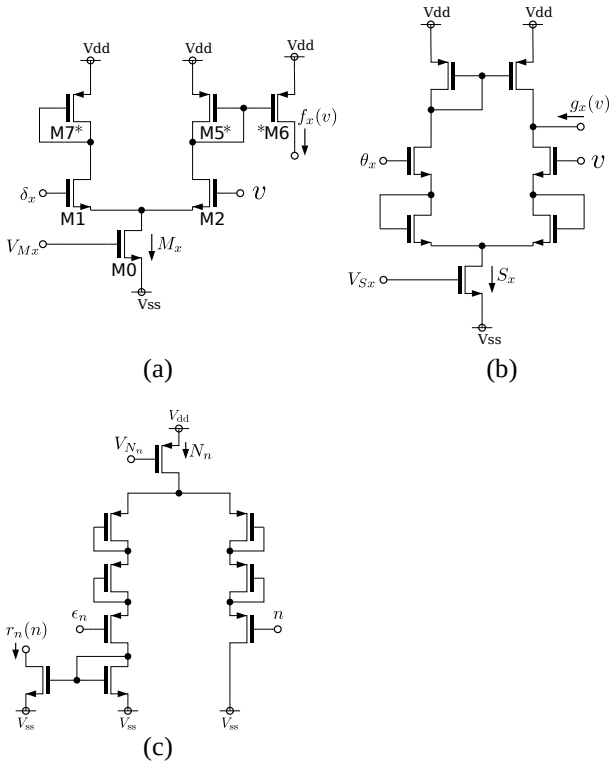


Figure 1: Elemental circuits in our silicon neuron. Circuits for (a) $f_x(v)$, (b) $g_x(v)$, and (c) $r_n(n)$.

Effect Transistors (MOSFETs) operated in their subthreshold domain. Their circuits are simple and compact (see Fig. 1) and consume very low-power below several nano watts. These curves are similar to hyperbolic tangent and have minor variations depending on supplementary circuits. The equations of our model is as follows:

$$C_v \frac{dv}{dt} = -g_v(v) + f_m(v) - r_n(n) + I_a + I_{stim}, \quad (1)$$

$$C_n \frac{dn}{dt} = -g_n(v) + f_n(v) - r_n(n), \quad (2)$$

where v and n respectively represent the membrane potential and a recovery variable. Two constants C_v and C_n represent capacitance responsible for the time constants of these variables. Currents I_{stim} and I_a are an external stimulus and a constant bias currents. Functions f_x ($x = m$ and n), g_x ($x = v$ and n) and r_n are the ideal characteristics curves of the circuits whose schematics are depicted in Fig. 1. Their equations are

$$f_x(v) = \frac{M_x}{2}\{\tanh(\frac{\kappa}{U_T}\frac{v-\delta_x}{2}) + 1\}, \quad (3)$$

$$g_x(v) = S_x \tanh(\frac{\kappa}{U_T}\frac{v-\theta_x}{4}), \quad (4)$$

$$r_n(n) = \frac{N_n}{2}\{\tanh(\frac{\kappa}{U_T}\frac{n-\epsilon_n}{6}) + 1\}, \quad (5)$$

where U_T is the thermal voltage (approximately 26mV) and κ is the capacitive-coupling ratio that is dependent

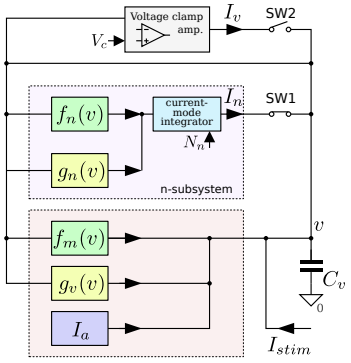


Figure 2: Block diagram of our silicon neuron.

on the fabrication process and the operating condition of MOSFETs (between 0.6 and 1.0 in most cases). Parameters M_x, δ_x, S_x, θ_x, N_n, and ϵ_n as well as I_a are specified by externally applied voltages to the circuit.

This model can be implemented by a circuit whose block diagram is illustrated in Fig. 2. Here, blocks labeled $f_m(v)$ and $f_n(v)$ correspond to the circuit in Fig. 1(a) and those labeled $g_v(v)$ and $g_n(v)$ to one in Fig. 1(b). The current-mode integrator block is composed of the circuit in Fig. 1(c) and a capacitor C_n, whose output current I_n codes value of $r_n(n)$. Two switches SW1 and SW2 are closed and open in normal operation as a silicon neuron. The voltage-clamp amp block allows drawing the nullclines after circuit fabrication by a similar principle to the voltage-clamp experiment in the electrophysiological field. This function provides a powerful tool for tuning the externally applied parameter voltages to cancel the effect of the inevitable fabrication variation [5]. The nullclines are drawn by opening SW1 and closing SW2 (nullcline mode) and then sweeping V_c in a desired range sufficiently slowly. Plotting I_v and I_n for each v value draws the v- and the r_n-nullclines in the v-r_n phase plane. For tractability of the model, we rewrite Eqs. (1) and (2) as follows by redefining r_n as new n.

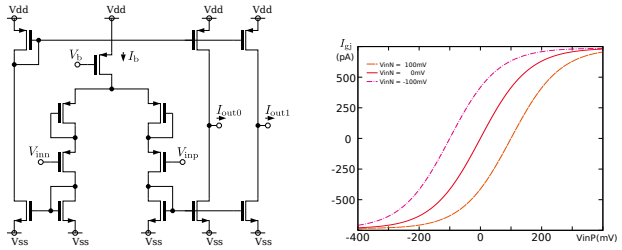
$$C_v \frac{dv}{dt} = -g_v(v) + f_m(v) - n + I_a + I_{stim}, \quad (6)$$

$$C_n \frac{dn}{dt} = \frac{\kappa}{U_T}\frac{n(N_n-n)}{3N_n}(-g_n(v) + f_n(v) - n). \quad (7)$$

For GJ circuit, a transconductance amplifier is used to simulate GJ's linear response to the difference between v in two neurons, whose model is as follows:

$$I_{ij} = G_{gj}\tanh(\frac{\kappa}{U_T}\frac{v_j - v_i}{4}), \quad (8)$$

where I_{ij} is current flows into the i-th neuron from the j-th neuron, and G_{gj} is the conductance of the silicon GJ. Because v ranges between -100 mV and 50 mV, difference between v can be at most 150mV. A pair of source degeneration transistors are inserted at the input stage (Fig. 3(a)) to expand linearity of the response curve and avoid saturation of I_{ij}. This does not increase power consumption and requires only two additional transistors.



(a) (b)

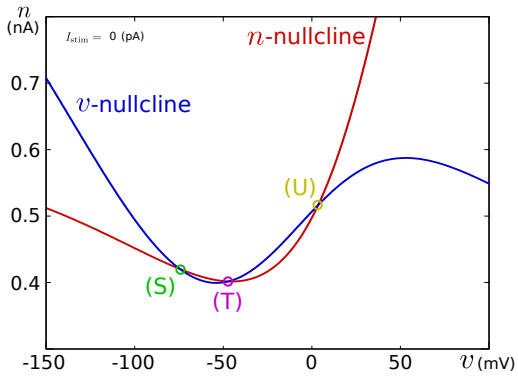
Figure 3: A transconductance amplifier used as silicon GJ. (a) Schematics. (b) characteristics curves calculated by SPECTRE circuit simulator.

2.2. Simulation results

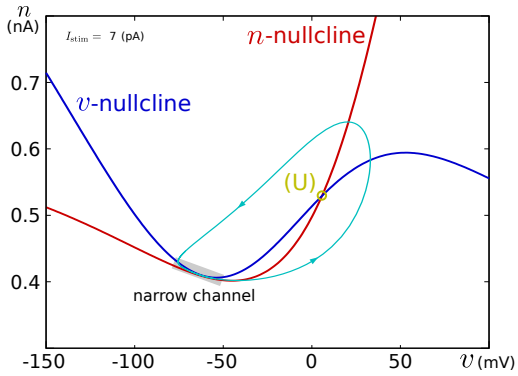
We verified behavior of our silicon neuron circuit using SPECTRE circuit simulator with TSMC .25μm CMOS process design library. Based on the *v*- and the *n*-nullclines drawn in the nullcline mode and time-series data obtained by normal operation mode, value of the parameters are decided so that our silicon neuron belongs to Class I*. Figure 4(a) illustrates the nullclines when no external stimulus is applied. They have three intersections and stability of these equilibrium points (S), (T), and (U) were estimated to be stable, a saddle, and unstable by transient simulation with several initial states sufficiently near them. If sustained excitatory stimulus is applied, the *v*-nullcline is displaced upward, which causes a saddle-node bifurcation and generate a stable limit cycle (Fig. 4(b)). Stability of the limit cycle could be estimated by transient simulation in the same way as for the equilibrium points. It is well known that such a bifurcation scenario induces periodic spiking in response to sustained excitatory stimulus, whose frequency is very low at its onset and increased in response to the strength of the stimulus (Class I) [8]. This phenomenon was confirmed in our circuit by transient simulation as shown in Fig. 5. In Fig. 4(b), we can confirm that there exists a narrow channel, a region where both of the nullclines stay very close to each other, which is the key condition that discriminates the Class I* neurons from the rest of Class I neurons.

3. A GJ-connected silicon neuronal network

Conditions of Class I* are necessary but not sufficient ones for the distinctive chaotic behaviors in its GJ-connected network. Simulation of a GJ-connected network of our silicon neurons were performed to confirm its ability to produce such behaviors. The results in this section were obtained by numerical simulation of the system equations (6), (7), and (8) by XPPAUT and scilab softwares because amount of calculation is too large for circuit simulators in our computer environment. In this network model, 6 silicon neurons are connected via silicon GJs in ring topology where each neuron is connected with two neighborhoods. In Fig. 6, 8 largest Lyapunov exponents per sec-

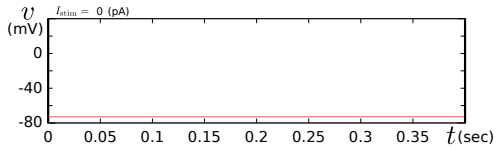


(a)

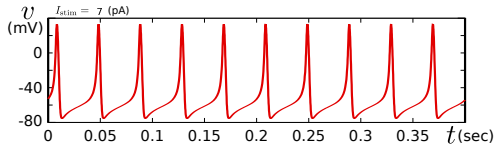


(b)

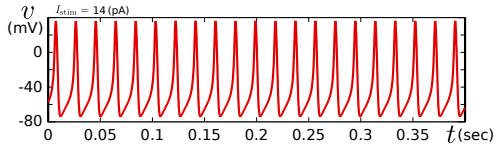
Figure 4: The *v*-*n* phase plane drawn in the nullcline mode using SPECTRE circuit simulator. (a) $I_{\mathrm{stim}} = 0$. There are three equilibrium points (S), (T), and (U). (b) $I_{\mathrm{stim}} \sim 14$ pA. An equilibrium point (U) and a stable limit cycle exist.



(a)



(b)



(c)

Figure 5: Nullclines in of our silicon neuron circuit when (a) $I_{\mathrm{stim}} = 0$, (b) $I_{\mathrm{stim}} \sim 7$ pA, (c) $I_{\mathrm{stim}} \sim 14$ pA. Calculated by SPECTRE circuit simulator.

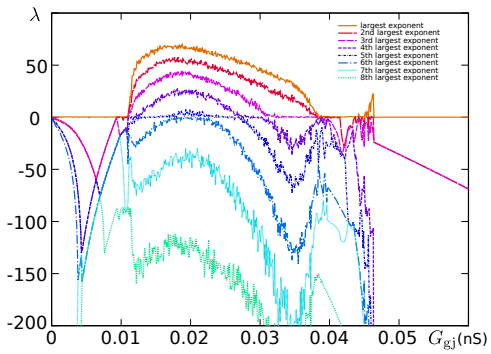


Figure 6: Lyapunov spectrum of a GJ-connected network of 6 silicon neurons.

ond of this network calculated by Wolf's method [9] where its linearized system was given analytically. While the silicon GJ's conductance, G_{gj}, is sufficiently strong, the largest exponent stays around 0 and the others are negative. In this situation, all the neurons are synchronized (Fig. 7(a)). As G_{gj} is decreased, the second largest exponent reaches 0 where quasiperiodic behaviors are observed (Fig. 7(b)), and then the two largest ones becomes positive where alternation between spatio-temporally chaotic and synchronized behaviors are observed (Fig. 7(c)). When more exponents have positive value, synchronized phase becomes rare (Fig. 7(d)). After another domain of two largest zero exponents, the largest one becomes the sole zero exponent, where anti-phase synchronization between two groups of staggered 3 neurons is observed (Fig. 7(e)). Every silicon neuron spikes in its own phase depending on the initial condition when G_{gj} is arbitrarily zero.

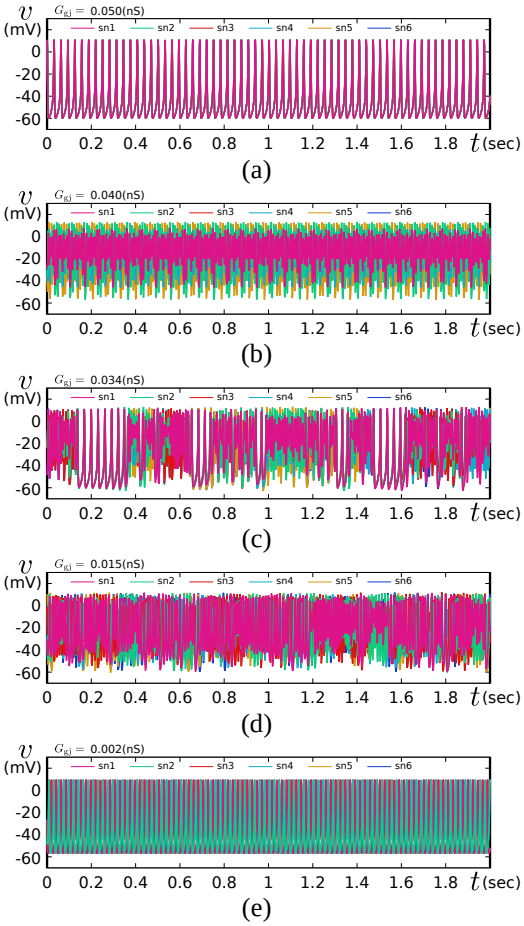


Figure 7: Behaviors of a GJ-connected network of 6 silicon neurons. Every v in the silicon neurons are superimposed.

4. Concluding remark

We have developed a simple Class I* silicon neuron and verified its ability to generate distinctive complex and synchronized activities in a GJ-connected network. Power consumption of this silicon neuron circuit is about 30 nW in SPECTRE simulation. Circuit experiments will be performed and reduction of power consumption down to about 15 nW by careful parameter tuning will be tried.

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