

Towards a Neuromorphic Computing Hardware System

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Abstract—Despite recent worldwide attempts to realize an elaborate brain-inspired computer hardware system, novel brain-inspired architectures, which try to approach the brain especially in performance using a non von Neumann architecture, are not fully established yet. In order to solve current problems in realizing truly brain-inspired computing systems, we proposed a brainmorphic hardware paradigm as a natural extension of the neuromorphic paradigm. In this paradigm, the brainmorphic hardware (1) processes information mimicking the anatomical and physiological mechanisms of cranial nervous system; (2) naturally uses physical and dynamical characteristics of the constituent devices especially through analog circuits; (3) reflects the latest knowledge from brain science, in particular, that for high-order brain functions including consciousness; and (4) considers and utilizes the bodily and environmental constraints, and evolutionary gain-of-function. This paper focuses on a novel “Whole Organism Computing” framework, which exploits bodily constraints and uses the homeo-dynamics as so called referenced-self.

1. Introduction

The impending collapse of the Moore’s law [1] expects novel system architecture for further intelligent and efficient computational hardware. One of such “Beyond Moore” candidates is a non von Neumann-type brain-inspired hardware system, e.g., a neural network based VLSI system. The advanced CMOS semiconductor device and integrated circuit technologies have fueled recent developments of large-scale neural network VLSI systems [2]–[6]. Key ingredients of the booming are ultra-low-power technologies for CMOS circuits, and asynchronous high-speed pulse communication technologies for a large number of synaptic connections.

Although some brain-like architecture such as fine-grained local memories and in-situ learning were employed, current brain-inspired VLSI hardware systems are far from the real brain. For example, their system architecture is not really non von Neumann or brain-like in the sense that information is not really distributed and integrated for representation, processing, and storage. In addition, complexity from multi-scale and multi-level dynamics, which are found to be important for higher-order brain functions [7]–[9], is largely ignored. Bodily and environmental constraints, which may lead to a unique and efficient information processing paradigm of the brain [10], are not

considered enough.

In order to get one step closer to the brain, we proposed a “brainmorphic” hardware paradigm [11, 12], which is a natural extension of the neuromorphic paradigm [13]. In this paradigm, the brainmorphic hardware should

1. process information mimicking the anatomical and physiological mechanisms of cranial nervous system,
2. naturally use physical and dynamical characteristics of the constituent devices especially through analog circuits,
3. reflect the latest knowledge from brain science, in particular, that for higher-order brain functions including consciousness, and
4. consider and utilize the bodily and environmental constraints, and evolutionary gain-of-function.

Nano devices will greatly contribute to the brainmorphic integrated hardware. In particular, tiny non-volatile analog memristive devices such as the spin-orbit torque device [14] are important key components for synaptic devices with learning and memory capabilities to fulfill the items 1. and 2. above.

For items 2. and 3., high-order complex physical dynamics from analog circuits are important and efficient. For example, the dynamics/algorithm hybrid neural hardware systems to solve optimization problems are illustrated in Refs. [15, 16], which are inspired by sub-conscious/conscious processes in the brain as a meta-level analogy.

In this paper, to fulfill item 4., we propose a novel “Whole Organism Computing” framework [11, 12] focusing on the bodily and environmental constraints as an embodiment [10], which is one of the key elements for a unique and efficient information processing paradigm of the brain.

2. Whole Organism Computing Framework

We proposed the whole organism computing framework [11, 12] to overcome the problems in recent brain-inspired computers. We are aiming at a small and low-power integrated circuit implementation of brainmorphic hardware based the whole organism computing framework.

Required elements for such brainmorphic hardware would be;

- A Generation of stable neural patterns that represent “self” or “referenced-self” in some sense.

- B Dynamical generation of sensitive neural patterns that represent corresponding external objects.
- C Internal state changes by mutual interactions between A and B above, which correspond to emotions or core-consciousness.
- D Mechanisms for the embodiment and interactions with external objects.
- E Conscious and sub-conscious processes, and high-order functions arisen from the mutual interactions of them.
- F Memory creations through a macroscopic learning mechanism.
- G Global regulations to control and modify processing.

The whole organism computing can be constructed with subsystems, “core-self subsystem,” “body subsystem,” and “conscious/subconscious hybrid subsystem” as shown in Fig. 1. As shown in the figure, the core-self subsystem realizes items A–C above, while the body subsystem is in charge of item D. The items E–G are taken care of by the conscious/subconscious hybrid subsystem.

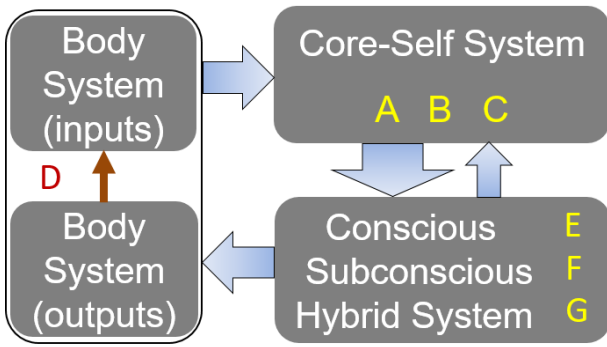


Figure 1: A possible architecture of the whole organism computing framework with constituent subsystems.

3. Hardware Architecture

In this section, basic considerations for hardware realization of each subsystem in Fig. 1 are described.

3.1. Core-self subsystem

This subsystem consists of three elements, that is, ① retention of a neural pattern that represents “self” (internal state), ② neural pattern generation in response to the external object, and ③ mutual interactions of ① and ② resulting a novel neural pattern.

A possible hardware architecture suitable for the core-self subsystem is shown in Fig. 2. As shown in the figure, the core-self subsystem is constructed with neural networks (NNs), which correspond to ① to ③ above, that is, ① a self-reference internal state NN, ② an object representation NN, and ③ a state-change detection NN.

The NN for ① robustly maintains the self-reference internal state. The integrated-and-fire (IF) based spiking neuron circuit would be used for small and low-power IC implementation. The network structure will be pre-defined,

but some fluctuations will be introduced in neuron and network characteristics for rich spatio-temporal spike patterns.

In contrast, the NN for ② should rapidly respond to the external input, and change its neural pattern. Therefore, we employ chaotic itinerancy [17] for the default state, and use infinite number of low-dimensional quasi-attractors to represent external objects. For this purpose, we introduce time-domain chaotic neuron (TDCN) circuit such as in Ref. [18]. Network structure will be random, but sparse.

Finally, ③ will have a triple NN structure with (i) a NN that retains a copy of the reference state of ①, and whose internal state is altered by ②, (ii) a NN that extracts the change in the NN of (i), and (iii) a NN that produces a neural pattern according to (ii). The NN in (i) uses the same neuron circuit as that in ①, while a simple IF based spiking neuron circuit would be used in (ii). The TDCN would be suitable for the NN in (iii) for a variety of complex spatio-temporal spiking patterns.

In the core-self subsystem, network structures (weights) of ① and (i) of ③ will be simultaneously modified if the change detected by (ii) is large enough. This learning signal will be provided by the conscious/subconscious hybrid subsystem.

3.2. Body subsystem

The body subsystem realizes the embodiment and interactions with external objects. Because high-performance sensor and actuator technologies are readily available, we use these advanced sensor and actuator devices as shown in Fig. 3. However, we newly define a general asynchronous pulse-mode in-system communication protocol to incorporate these external devices. In addition, we will develop inherent interfaces ($\boxed{I/F}$ in Fig. 3) specific for each device.

3.3. Conscious/subconscious hybrid subsystem

The conscious/subconscious hybrid subsystem consists of (1) conscious and sub-conscious processes, (2) a high-order processing through interactions between them, and (3) a global control with macroscopic learning rule.

A possible hardware configuration for this subsystem is shown in Fig. 4. As shown in the figure, this hardware includes:

1. Working memory for high-order information manipulations, predictions, and optimizations.
2. A large-capacity memory for an episodic memory.
3. A memory-based processing system for associations, predictions/evaluations, and optimizations.
4. A learning system for the episodic memory.
5. An output signal generation to the body system through the feedback of the results in 3. above.
6. A global control system which enhances the necessary patterns.

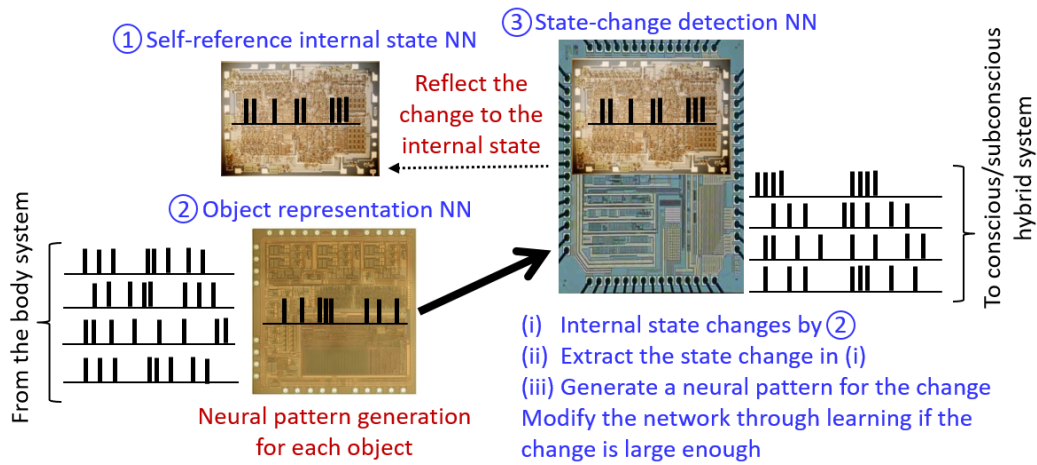


Figure 2: A possible hardware architecture for the core-self subsystem.

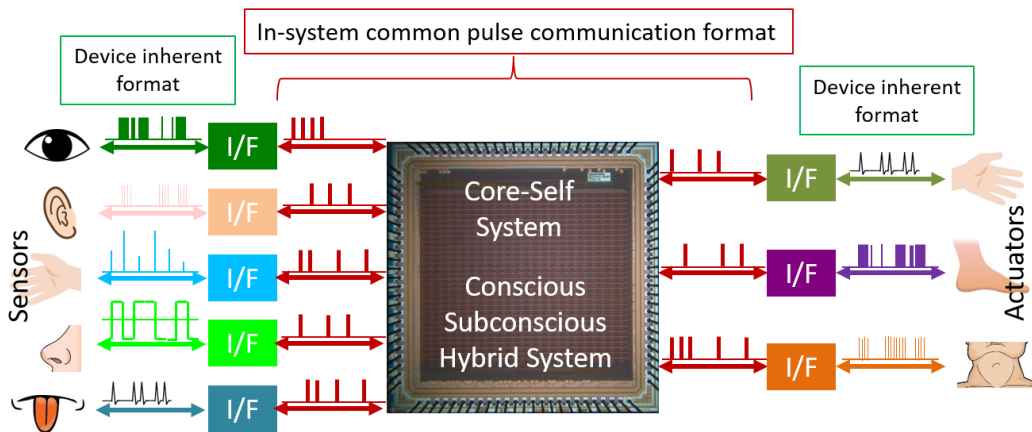


Figure 3: A possible hardware architecture for the body subsystem.

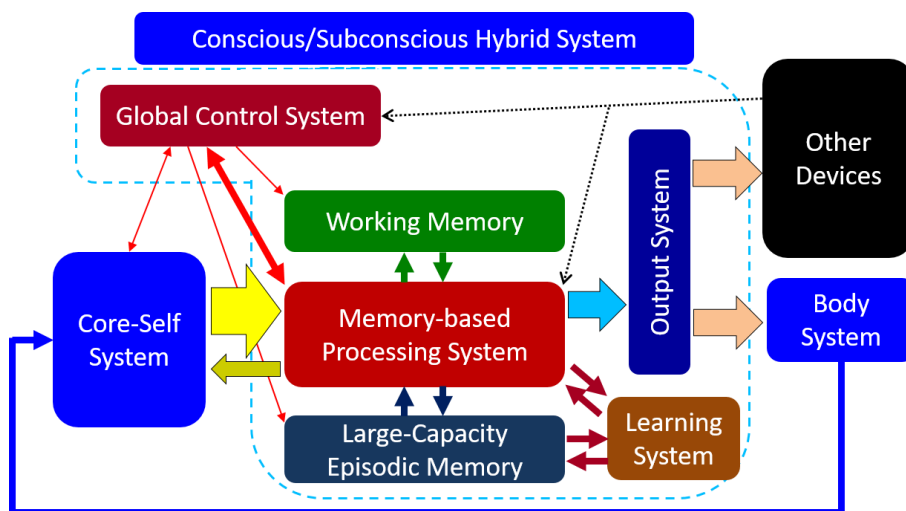


Figure 4: A possible hardware architecture for the conscious/subconscious hybrid subsystem.

4. Conclusions

We proposed the whole organism computing framework, which utilizes bodily constraints and bodily states as referenced-self, and its possible hardware architecture.

The whole organism computing system would make autonomous and spontaneous information collection/processing/learning possible through embodiment, emotions, feelings, consciousness, and self. In addition, it would also realize natural interactions with users of the system and environment. Therefore, a computational system that does not depend on the skill level of the users is expected. In addition, it will be possible to segregate high-order and autonomous processes, so that we can assign more resources to higher-order processing. This will lead to emergence of attention mechanisms. Efficient recognition and learning through natural weighting of processes, and rapid transition among different processes would also be possible by introducing the global control and learning mechanisms.

Because of these properties, the brainmorphic computers would acquire “self” in a sense. In addition, they would recognize the objects and learn their specific characteristics by actively using the direct interactions with external objects, such as their users and environment. Such a brainmorphic computational hardware will highly contribute to realize a “User Dependent, Personalized Computer (UDPC),” which autonomously execute specific processing adaptively to each object. The UDPC would be directly applicable to robots, autonomous cars, space and deep-sea explorations and so on, in which spontaneous learning of the user or environment, and autonomous decision-making are mandatory. Furthermore, the UDPC would be quite useful to implement easier-to-use and more flexible artificial intelligence as a partner for an aging society.

The details of the proposed architecture and hardware are currently under development. We will report the results for a practical hardware system elsewhere.

Acknowledgments

This work is supported by JSPS KAKENHI Grant Numbers 16K00340 and 17H0693. Part of this work was carried out under the Cooperative Research Project Program of the Research Institute of Electrical Communication, Tohoku University.

References

- [1] A. Huang, “Moore’s law is dying (and that could be good),” *IEEE Spectrum*, vol. 52, no. 4, pp. 43–47, 2015.
- [2] P.A. Merolla et al., “A million spiking-neuron integrated circuit with a scalable communication network and interface,” *Science*, vol. 345, issue 6197, pp. 668–673, 2014.
- [3] S.B. Furber, F. Galluppi, S. Temple, and L.A. Plana, “The SpiNNaker project,” *Proc. IEEE*, vol. 102, no. 5, pp. 652–665, 2014.
- [4] B.V. Benjamin et al., “Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations,” *Proc. IEEE*, vol. 102, no. 5, pp. 699–716, 2014.
- [5] <http://BrainsScaleS.eu>
- [6] J. Schemmel et al., “A wafer-scale neuromorphic hardware system for large-scale neural modeling,” in *Proc. IEEE Int. Symp. on Circuits and Syst.*, pp. 1947–1950, 2010.
- [7] A. Damasio, “Feeling of What Happens,” *Harcourt Brace*, ISBN: 0156010755, 1999.
- [8] G. Edelman and G. Tononi, “A Universe of Consciousness,” *Basic Books*, ISBN: 0465013775, 2000.
- [9] A. Damasio, “Self Comes to Mind –Constructing the Conscious Brain–,” *Pantheon*, ISBN: 13: 9780307378750, 2010.
- [10] J. Hawkins, “What intelligent machines need to learn from the neocortex,” *IEEE Spectrum*, vol. 54, no. 6, pp. 33–37 and 68–69, June 2017.
- [11] Y. Horio, “Towards a brainmorphic whole organism computing system,” in *Abstracts of The 4th International Symposium on Brainware LSI*, p. 13, 2017.
- [12] Y. Horio, “Towards a brainmorphic hardware system,” in *Abstracts of The AIMR International Symposium 2017*, p. 41, 2017.
- [13] C. Mead, “Neuromorphic electronic systems,” *Proc. IEEE*, vol. 78, no. 10, pp. 1629–1636, 1990.
- [14] W.A. Borders et al., “Analogue spin-orbit torque device for artificial-neural-network-based associative memory operation,” *Applied Physics Express*, DOI:10.7567/APEX.10.013007, 2017.
- [15] Y. Horio and K. Aihara, “Analog computation through high-dimensional physical chaotic neurodynamics,” *Physica-D*, vol. 237, no. 9, pp. 1215–1225, 2008.
- [16] Y. Horio, T. Ikeguchi, and K. Aihara, “A mixed analog/digital chaotic neuro-computer system for quadratic assignment problems,” *Neural Networks*, vol. 18, no. 5-6, pp. 505–513, 2005.
- [17] K. Kaneko and I. Tsuda, “Chaotic itinerancy,” *AIP Chaos*, vol. 13, no. 3, pp. 926–936, 2003.
- [18] Y. Horio, T. Taniguchi, and K. Aihara, “An asynchronous spiking chaotic neuron integrated circuit,” *Neurocomputing*, vol. 64, pp. 447–472, 2005.