2017 International Symposium on Nonlinear Theory and Its Applications,
NOLTA2017, Cancun, Mexico, December 4-7, 2017

IC Prototyping of a Switched-Current A/D Converter Circuit Based on the Golden Ratio Encoder

Yoshihiko Horio† and Takayoshi Fujino‡

†Research Institute of Electrical Communication, Tohoku University
2–1–1 Katahira, Aoba-ku, Sendai 980-8577, Japan
‡LSI Development Headquarters, LAPIS Semiconductor Co., Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
Email: horio@riec.tohoku.ac.jp

Abstract—A golden ratio analog to digital (A/D) converter (golden ratio encoder; GRE) was proposed as a special case of a β-encoder, which encodes an analog signal to a digital bit sequence with a real number radix of $\beta = \phi$ (golden ratio). The β-encoder family was mathematically proved to be robust against variations in circuit and environmental parameters, and noise, so that it is suitable for an integration with the latest mixed-signal ultra-small semiconductor process. This paper presents a proof-of-concept IC prototyping of a switched-current GRE A/D converter circuit using a 180 nm CMOS semiconductor process. Simulation results for the prototype circuit extracted from the layout are shown.

1. Introduction

In the advanced ultra-small microfabrication process, analog-to-digital (A/D) converters are difficult to realize with high accuracy due to low-supply-voltage, low intrinsic gain, variations in component characteristics, and noise from the environment and a vast number of digital components on the same substrate. To alleviate these problems, for example, an A/D converter circuit architecture based on a comparator without using an operational amplifier has been proposed [1]. However, in general, for high-performance A/D converter circuits, it is necessary to secure the accuracy of elements, and to introduce error correction techniques such as a digital compensation.

For robust implementation of high-performance A/D converters under such an unfavorable situation for analog circuits, a β-encoder has been proposed, which converts a real number to a digital bit sequence by using a real number radix based on the β-expansion [2]. One of the advantages of the β-encoder is robustness against variations in circuit component characteristics, temperature, and noise [2–4]. By exploiting this robustness, it is possible to realize an accurate A/D converter even with poor-characteristic analog circuit elements available in an advanced nanometer semiconductor fabrication process [5].

To further improve the robustness, the golden ratio encoder (GRE) was proposed as a special case of the β-encoder in which the radix value is the golden ratio $\phi = (1 + \sqrt{5})/2$ [6]. The GRE inherits all the advantages of the β-encoder [7]. Moreover, we can always use the fixed radix value of the golden ratio for GRE; in contrast, the β-encoder is necessary to estimate the effective value of radix of β from the output bit sequence.

We have proposed a circuit implementation technique for an A/D converter circuit based on the GRE using switched-capacitor (SC) and switched-current (SI) circuit techniques [8, 9].

In this paper, we present a proof-of-concept IC implementation of an improved SI GRE A/D converter circuit, which is suitable for an advanced low-voltage microfabrication process, using 180 nm CMOS semiconductor process. We confirm the functionality and robustness of the prototype circuit with SPICE simulations of the extracted circuits from IC layout.

2. The Golden Ratio Encoder

The conversion algorithm of GRE [6, 7] is as follows:

$$u_n = \lambda_1 u_{n-1} + \lambda_1\lambda_2 u_{n-2} - b_n, \tag{1}$$

$$b_n = Q_\nu^\alpha(\tilde{u}_{n-2}, \tilde{u}_{n-1}), \tag{2}$$

$$Q_\nu^\alpha(\tilde{u}_{n-2}, \tilde{u}_{n-1}) = \begin{cases} -1, & \tilde{u}_{n-2} + \alpha\tilde{u}_{n-1} < \nu, \\ 1, & \tilde{u}_{n-2} + \alpha\tilde{u}_{n-1} \geq \nu, \end{cases} \tag{3}$$

where an integer n is a discrete-time index, u_n is an internal state, $u_{-1} = x_{\text{input}} \in [-1, 1]$ is an analog input, $u_0 = 0$ is the initial internal state value, α is the coefficient, ν is the threshold value of the quantizer $Q_\nu^\alpha(\cdot,\cdot)$, and $b_n \in \{0, 1\}$ is the digital output bit. As shown in Fig. 1, λ_1 and λ_2 are non-unity coefficients considering non-ideal transfer characteristics of the delay circuits.

On the other hand, the analog value $\hat{x}_{\text{input}}$ from the L-bit output bit sequence b_n can be retrieved as

$$\hat{x}_{\text{input}} = \sum_{n=0}^{L} b_n \phi^{-n}. \tag{4}$$

Because the GRE is based on the β-encoder, we can derive it from the equations for the β-encoder with $\beta = \phi$ [6, 7]. In the course of derivation, it is shown that the real number expansion of radix ϕ can be performed without using any multiplier unit to generate u_n if we use the relation of $\phi^2 = \phi + 1$ [7]. In addition, calculation of the internal state value u_n can be constructed with unit delay elements only [6, 7].

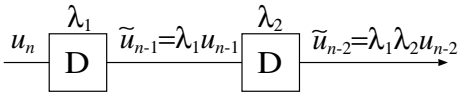

Figure 1: Non-ideal transfer characteristic of the delay elements with non-unity gains of λ_1 and λ_2.

It was also shown that variations in the values of ν and α are allowed if the threshold value ν and the coefficient α are within a certain range [7]. This property guarantees further robustness of GRE.

3. Switched-Current A/D Converter Circuit Based on GRE

We proposed a circuit configuration for an A/D converter based on GRE [9] as shown in Fig. 2. As shown in the figure, the A/D converter consists of two stages as a loop, and each conversion stage takes the one- and two-previous internal state values from the other conversion stage. After that, each stage outputs a single digital bit b_n^k, where k represents the number of the stage, that is, $k = 1$ or 2. The consolidated output bit sequence $b_1^1, b_1^2, b_2^1, \ldots, b_{L/2}^1$, and $b_{L/2}^2$ is obtained by alternately interpolating b_n^k such as $k = 1, 2, 1, 2, \ldots$, as many times as the bit length L.

Figure 3 shows possible structure of the conversion stages in Fig. 2. As shown in the figure, each stage is composed of SI delay circuits, a weighted 2-input adder, a current comparator (CP), and a current multiplexer (MUX). The current delay circuit operates based on the trans-linear principle with analog inverters shown in Fig. 4. The input and output of analog inverters A1 and A2 in Fig. 3 are short-circuited so that they work as a trans-resistance, while ordinary analog inverters A3, A4 and A5 are trans-conductance amplifiers. The comparator is composed of a trans-linear inverter chain, and serves as the quantizer $Q_\nu^\alpha(\cdot,\cdot)$. The current multiplexer is a simple current switching circuit followed by a trans-linear inverter-pair as a current buffer.

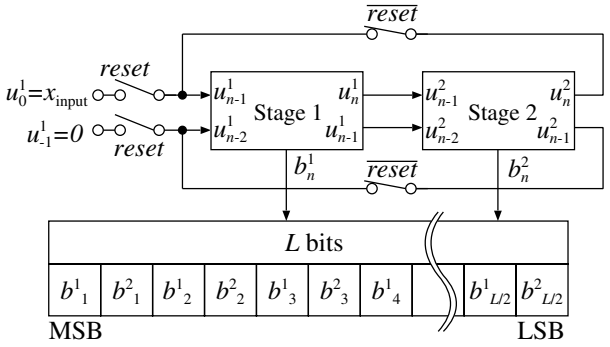

Figure 2: Block diagram of the GRE A/D converter [9].

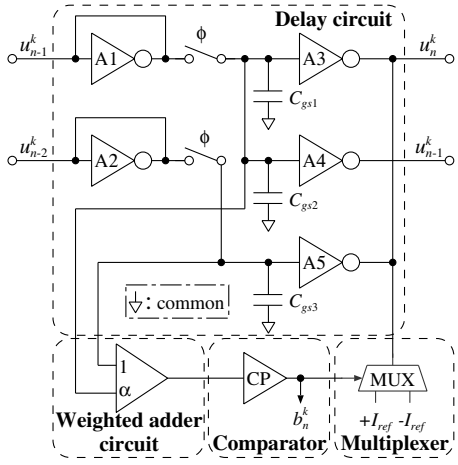

Figure 3: Possible structure of conversion stages in Fig. 2.

3.1. Improved weighted adder circuit

We proposed a voltage-mode weighted adder circuit for the conversion stage in Ref. [9]. However, a large error was observed because the proposed circuit was voltage-mode, and it did not match to the lest of the current-mode trans-linear circuits. Therefore, we newly propose, in Fig. 5, a current-mode weighted adder circuit. The ratio of addition can be determined by that of the numbers of inverters X and Y, which is denoted as W_X and W_Y, respectively, that is, $I_{out} = W_X I_x + W_Y I_y$. Figure 5 shows the case where $W_X = 2$ and $W_Y = 3$ as an example, so that $I_{out} = 2I_x + 3I_y$. If we assign $I_x = u_{n-1}$, and $I_y = u_{n-2}$, then from eq. (3), we can determine the value of α by the ratio of W_X and W_Y. From eq. (3), $W_X : W_Y = 1 : \alpha$; therefore, $\alpha = W_Y/W_X$. The value of α can fluctuate in a certain interval [7], therefore, mismatches in inverter characteristics are tolerable.

4. Prototype for SI GRE A/D Converter Circuit

Figure 6 shows a SI circuit realization of the A/D converter based on GRE shown in Fig. 2 based on the trans-linear principle with simple CMOS analog inverters shown

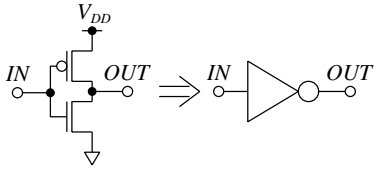

Figure 4: CMOS analog inverter used as a basic circuit element, and its symbol.

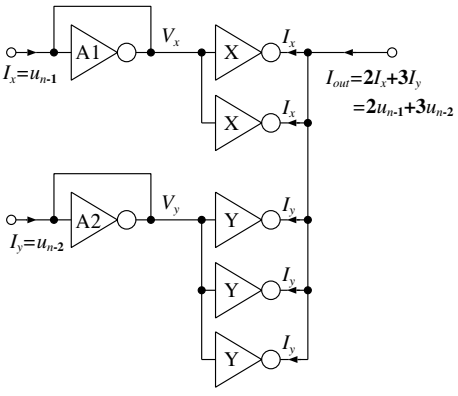

Figure 5: The weighted current adder circuit.

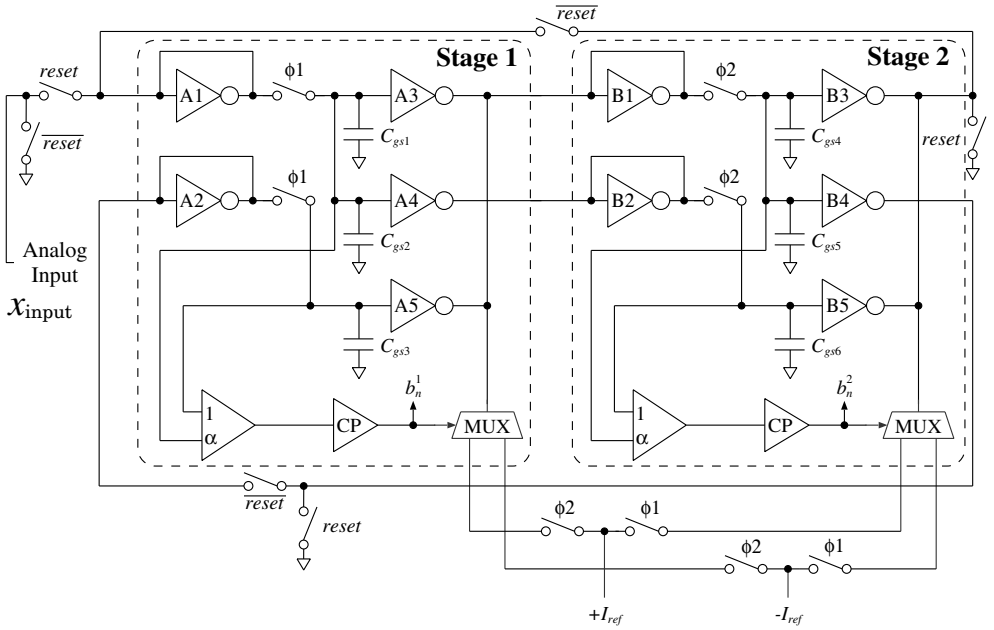

Figure 6: Switched-current A/D converter circuit based on GRE.

in Fig. 4. The triangle symbol with α corresponds to the weighted adder circuits of Fig. 5. In the IC implementation, parasitic capacitors are used as the sample-and-hold capacitors in Fig. 6 to save the area.

The circuit in Fig. 6 is driven by non-overlapping two phase clock waveforms $\phi 1$ and $\phi 2$. However, at the initial phase of conversion, the "reset" signal inputs the analog signal x_{input}; at the same time, it sets all internal states to zero value.

A proof-of-concept prototype chip was designed for ROHM 180 nm CMOS semiconductor process. Figure 7 shows the layout of the chip that integrates the SI GRE A/D converter in Fig. 6 (marked with a red rectangular; the size is about 210 μm $\times$ 78 μm), and auxiliary circuits to test and evaluate circuit components.

Design specifications of the SI GRE circuit are as follows: The nominal supply voltage is 1.3 V, the conversion rate is 15.8 kSamples/Sec., the analog input current range is $\pm 10\ \mu A_{\text{p-p}}$, and the bit length $L = 13$, which is equivalent to 9 bits for binary expansion.

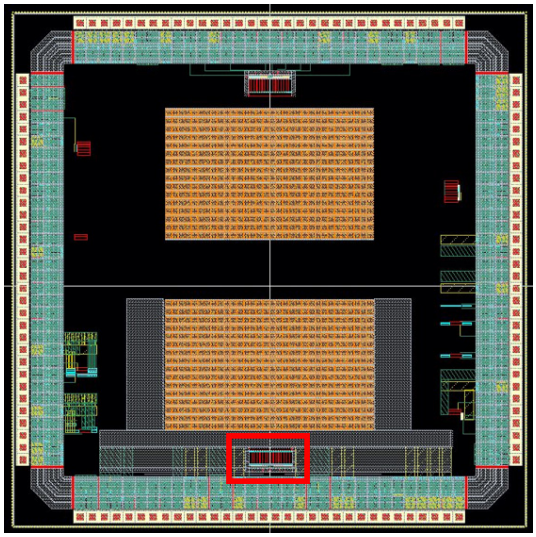

Figure 7: The layout of the proof-of-concept chip for the SI A/D converter circuit based on GRE.

5. Simulation Results from the Layout

The operation of the proposed circuit was confirmed by SPICE simulations using the extracted circuit from the layout in Fig. 7. In the following evaluation examples, we show the spectrum of decoded sinusoidal signal $\hat{x}_{\text{input}}$ with frequency f_{in} of 976.5625 Hz, the effective number of bits (ENOB) estimated from the spectrum with sampling frequency f_s of 15.8730159 kHz, ENOBs for different temperatures, and ENOBs for supply voltage changes.

5.1. Spectrum and ENOB

Figure 8 shows the power spectrum of the decoded signal $\hat{x}_{\text{input}}$ from the output bit-sequence of the circuit according to eq. (4). From the result, we estimated the signal-to-noise and distortion ratio (SNDR) as 52.73 dB. Therefore, the circuit gives 8.467 bit of ENOB, which satisfies the design specification.

5.2. ENOBs for different temperatures

We changed temperature from -30 C° to 100 C° in 10 C° steps, and estimated ENOB for each temperature. The result is shown in Fig. 9. This result confirms the robustness of the proposed circuit against large temperature changes.

5.3. Effect of supply voltage changes

Figure 10 shows ENOBs when we change the value of supply voltage from 1 V to 1.8 V with 0.1 V steps while

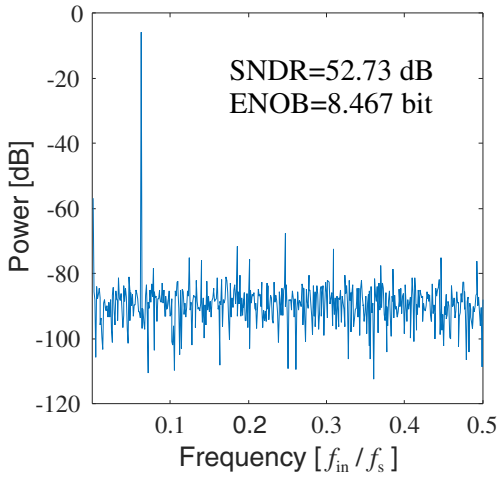

Figure 8: The power spectrum of the decoded signal $\hat{x}_{\text{input}}$.

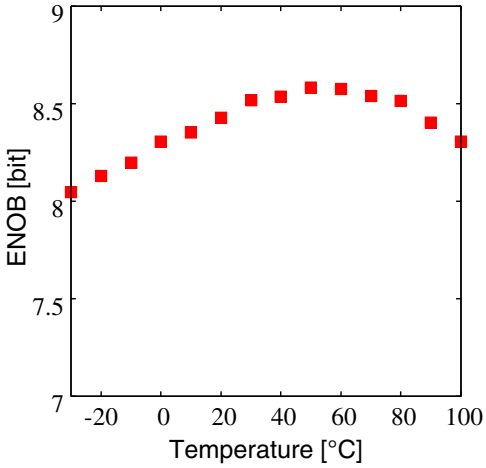

Figure 9: ENOBs for different temperatures.

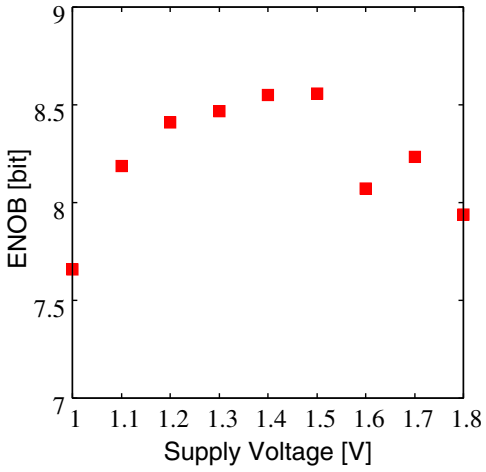

Figure 10: ENOBs obtained with different supply voltages.

nominal supply voltage is 1.3 V. The result demonstrates the robustness of the proposed circuit against supply voltage changes.

6. Conclusion

We have designed the proof-of-concept IC chip for the SI A/D converter circuit based on GRE. The operation and robustness of the proposed circuit were confirmed by circuit simulations with extracted circuit from the layout. The chip is under fabrication, so that we will present measured results from the chip elsewhere.

Acknowledgments

Part of this work was carried out under the Cooperative Research Project Program of the Research Institute of Electrical Communication, Tohoku University. This work is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

[1] Y. Nishida, "The feedforward ΔΣ ADC employing an adder comparator," in Proc. Int. Conf. on Signals and Electron. Syst., pp. 173–176, 2010.

[2] I. Daubechies, R.A. DeVore, C.S. Güntürk, and V.A. Vaishampayan, "A/D conversion with imperfect quantizers," IEEE Trans. IT, vol. 52, no. 3, pp. 874–885, 2006.

[3] T. Kohda, Y. Horio, Y. Takahashi, and K. Aihara, "Beta encoders: Symbolic dynamics and electronic implementation," Int. J. Bifurcation and Chaos, vol. 22, issue 9, DOI:10.1142/SO218127412300315, 2012.

[4] T. Kohda, Y. Horio, and K. Aihara, "β-expansion attractors observed in A/D converters," AIP Chaos, vol. 22, no. 4, DOI:10.1063/1.4758813, 2012.

[5] R. Suzuki, T. Matsuura, H. San, K. Aihara, and M. Hotta, "Robust cyclic ADC architecture based on β-expansion," IEICE Trans. Electron., vol. E96-C, no. 4, pp. 553–559, 2013.

[6] I. Daubechies, C.S. Gunturk, Y. Wang, and O. Yilmaz, "The golden ratio encoder," IEEE Trans. IT, vol. 56, no. 10, pp. 5097–5110, 2010.

[7] R. Ward, "On robustness properties of beta encoders and golden ratio encoders," IEEE Trans. IT, vol. 54, no. 9, pp. 4324–4334, 2008.

[8] H. Fukushima, Y. Horio, and K. Aihara, "Switched-capacitor circuit implementation of golden-ratio-encoder: Effects of the offset voltage and finite gain of an op-amp," Tech. Rep. IEICE, vol. 111, no. 395, pp. 23–28, 2012 (in Japanese).

[9] T. Fujino and Y. Horio, "A switched-current golden ratio encoder circuit," in Proc. of Int. Symp. on Nonlinear Theory and Its Applications, pp. 526–529, 2016.