2005 International Symposium on Nonlinear
Theory and its Applications (NOLTA2005)
Bruges, Belgium, October 18-21, 2005

# Modeling of a Chaotic Third-order Log-domain Filter

Alon Ascoli*, Paul Curran* and Orla Feely*

* Department of Electronic Engineering, University College Dublin,
Belfield, Dublin 4, Ireland
E-mails: alon.ascoli@ucd.ie, paul.curran@ucd.ie and orla.feely@ucd.ie

**Abstract–**Log-domain filters are generally regarded as externally-linear internally-nonlinear current-mode circuits, in which the large-signal forward-active mode exponential current-voltage relationship of the bipolar junction transistor is used to map the input currents to the logarithmic domain before any analog processing is carried out. The filtered voltages are then converted back to the linear domain using the exponential mapping once again. When a common integrated circuit design practice is applied to such internally-nonlinear circuits, the resulting filters lose external linearity. Transistor parasitics play a crucial role in the emergence of such externally-nonlinear behavior. In this paper a transistor dynamic model is used to explain the chaotic behavior recently observed in a third-order log-domain filter for zero input.

## 1. Introduction

Log-domain filters [1-2] are generally regarded as externally-linear internally-nonlinear current-mode circuits, in which a compression stage is first employed to convert the input currents to logarithmic form before analog processing is carried out. At the end of the filtering process input-output linearity is restored by mapping the output voltages into current form through an expansion stage. The compressing and expanding actions confer on log-domain filters a number of desirable features: small distortion levels, low noise sensitivity, large dynamic range, high-speed and wide bandwidth.

In internally-linear differential capacitively-loaded filters it is common to replace each pair of equal-value shunt capacitors connected between two output nodes and ground with a single half-sized floating capacitor placed between those nodes. However, such practice gives rise to external nonlinear behavior in internally-nonlinear circuits, such as log-domain filters [3-4].

It is generally assumed that bipolar junction transistors (BJTs) employed in log-domain filters operate in the forward-active mode at all times and that the BJT input-output behavior is unaffected by its parasitic capacitances [1-2]. However, modeling each transistor as a static exponential nonlinearity, the state equations for the dynamics of floating-capacitor log-domain circuits, designed according to the method of operational simulation of doubly-terminated LC ladders [2], are unable to explain the externally-nonlinear behavior observed in such circuits [5]. In [6] including the BJT internal capacitances in the transistor large-signal Ebers-Moll static model [7] permitted us to explain the emergence of zero-input limit-cycle oscillations in a floating-capacitor second-order LC-ladder band-pass filter.

In this paper the BJT dynamic model presented in [6] is used to explain the rich nonlinear dynamics of a floating-capacitor third-order Chebyshev LC-ladder low-pass filter, which experiences limit-cycle oscillations, period-doubling bifurcations and even chaos for zero input and special initial conditions as one of the circuit parameters is incremented in small steps. This external nonlinear behavior, observed in PSpice simulations of the circuit, was described but left unexplained in [4]. Here the theory is validated by comparing the numerical solutions to the state equations, based on the BJT dynamic model, with the PSpice simulation results from [4].

Section 2 reviews the BJT dynamic model presented in [6]. Section 3 derives the mathematical form of the state equations for the dynamics of the zero-input third-order log-domain filter, whose external nonlinear behavior was described but left unexplained in [4]. The theory is validated in Section 4. Conclusions are drawn in Section 5.

## 2. BJT dynamic model

Figs. 1a and 1b show the basic positive and negative cells employed in log-domain LC-ladder filters [2]. If, in agreement with common assumptions from log-domain circuit theory [1-2], it is assumed that each BJT acts as a static nonlinearity in which the collector current $i_C$ is exponentially related to the base-emitter voltage $v_{BE}$ according to

$$i_C = I_S \exp(v_{BE} \mathrm{V_t}^{-1}) \qquad (1)$$

and BJT finite base current and parasitic effects are neglected, from the Translinear Principle [2] the input-output behavior of each cell in Fig. 1 is found to be:

$$i_{out} = I_o \exp((v_{in} - v_{out}) \mathrm{V_t}^{-1}) \qquad (2)$$

As proved in [5], such a BJT static model is unable to explain the externally-nonlinear behavior of the zero-input third-order LC-ladder Chebyshev low-pass filter from [4].

On the other hand, the large-signal dynamic models of the positive and negative cells, depicted in Figs. 2a and 2b respectively, presented in [6] and obtained by replacing each BJT in Fig. 1 with its Ebers-Moll static model [7] and inserting equal-value parasitic capacitances in parallel with the diodes, permit us to capture the nonlinear dynamics of the log-domain circuit under study, shown in Fig. 3.

Basic principles from circuit theory [7] yield the following characteristic equations for each cell in Fig. 2:

$$\frac{dy_j'}{d\tau} = A_j F(y_j') + b_{oj} + B_j i_j$$
$$v_j = C_j^T y_j' + c_{oj} \quad (3)$$

where $A_j$, $B_j$, $C_j^T$, $b_{oj}$ and $c_{oj}$ are suitable matrices, $j = 1, \cdots n$ ($n$ is the number of cells in the circuit), $\tau = tC^{-1}$ is the normalized time variable, $y_j' = y_j V_t^{-1} \in R^{n_j}$ is the normalized state vector ($n_j$ equals 6 for a positive cell and 7 for a negative cell). Eq. (3) represents each cell as a nonlinear time-invariant system with input $i_j = (i_{in,j} \quad i_{out,j})^T$, output $v_j = (v_{in,j} \quad v_{out,j})^T$ and nonlinearity $F(y_j') \in R^{n_j}$, whose $i^{\text{th}}$ component is $f(y_j'(i)) = \exp(y_j'(i)) - 1 \ (1 \le i \le n_j)$.

Applying Kirchhoff's Voltage Law to each cell of Fig. 2, linear relationships among the corresponding state variables are established:

$$D_j^T y_j' = d_{oj} \quad (4)$$

where $d_{oj} \in R^{p_j}$ ($p_j$ is equal to 1 for a positive cell and 2 for a negative cell) and $D_j^T$ is a suitable matrix.

### 3. Mathematical form of the circuit equations

The state vector of the overall system is $y' = (y_1' \quad \cdots \quad y_n')^T \in R^N$, where $N = n_1 + \cdots + n_n$. We order so that $y_1'$, ⋯, $y_n'$ correspond to cells $P_1, \cdots P_r, N_1, \cdots, N_{n-r}$ respectively, where index $r$ denotes the number of positive cells in the circuit.

Modeling each cell in Fig. 3 according to equations (3), the dynamics of the overall system are described by:

$$\frac{dy'}{d\tau} = AF(y') + b_0 + Bi$$
$$v = C^T y' + c_o \quad (5)$$

where $i = (i_1 \quad \cdots \quad i_n)^T \in R^{2n}$ and $v = (v_1 \quad \cdots \quad v_n)^T \in R^{2n}$ represent the input and output vectors respectively, $A$, $B$, $C^T$, $b_o$ and $c_o$ are suitable matrices and $F(y') = (F(y_1') \quad \cdots \quad F(y_n'))^T \in R^N$.

From equation (4), solutions of (5) must satisfy the following $q = p_1 + \cdots + p_n$ constraints:

$$D^T y' = d_o \quad (6)$$

where $d_o \in R^q$ and $D^T$ is a suitable matrix.

Equating voltages at each node in the circuit of Fig. 3, $m_1$ linear equations in $v$ are established:

$$Kv = 0 \quad (7)$$

where $K$ is a suitable matrix.

Application of Kirchhoff's Current Law to each floating capacitor yields $m_2$ ($m_1 + 2m_2 = 2n$) linear equations in $i$:

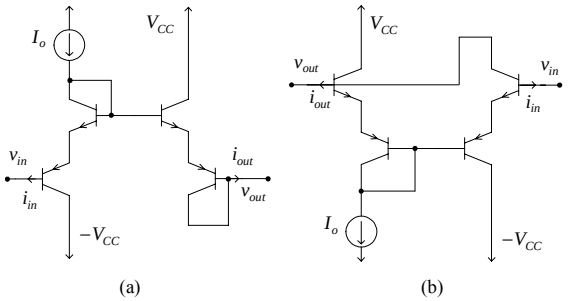


Fig. 1 (a) Positive cell. (b) Negative cell.

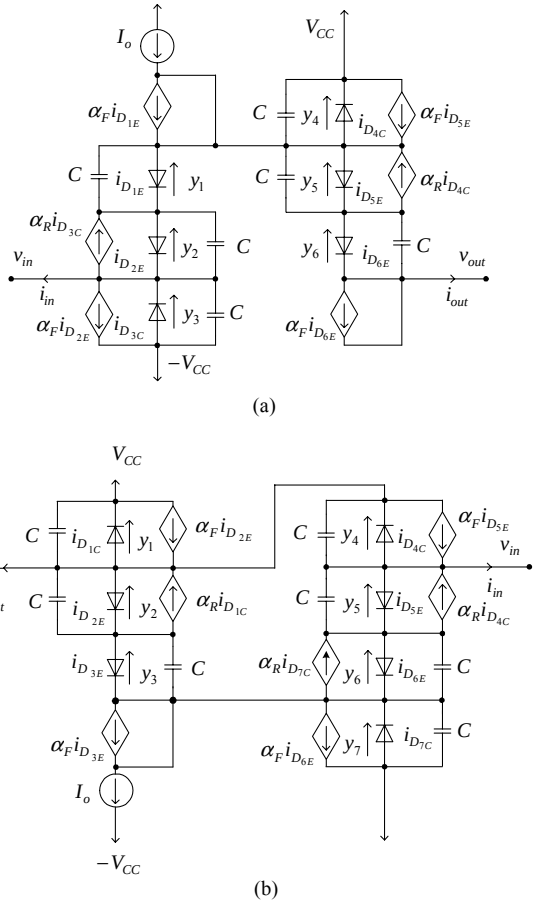





Fig. 2 Large-signal dynamic models of positive (a) and negative (b) cells.

$$\Lambda i = \rho_2 I_o \quad (8)$$

where $\Lambda$ and $\rho_2$ are suitable matrices.

The defining equations of the floating capacitors give further $m_2$ linear equations in $v$ and $i$:

$$\frac{H}{C}\frac{dv}{d\tau} + Li = \rho_3 I_o \quad (9)$$

for suitable matrices $H$, $L$ and $\rho_3$.

Equations (7)-(9) can be employed to uniquely determine $i$. Then, inserting $i$ into (5), the circuit equations are found to be:

$$\frac{dy'}{d\tau} = \tilde{M}_1 F(y') + \tilde{M}_o \quad (10)$$

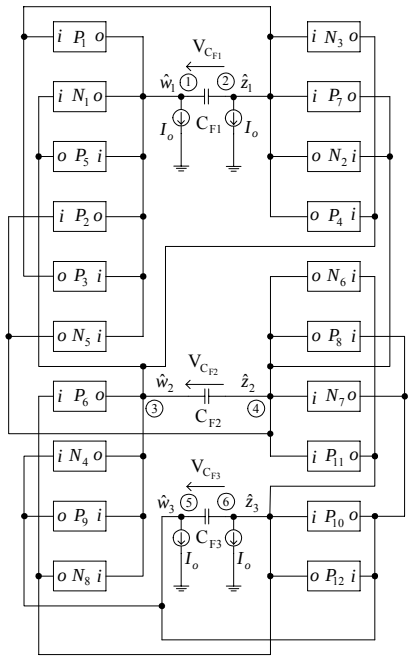


Fig. 3 Third-order log-domain filter from [4] without input and output cells. Here $n = 20$, $r = 12$, $N = 128$, $q = 28$, $m_1 = 34$, $m_2 = 3$ and $s = 62$.

for suitable matrices $\widetilde{M}_1$ and $\widetilde{M}_o$.

From equations (5) and (7):

$$KC^T y' = -Kc_o \tag{11}$$

Equations (6) and (11) yield $s = q+m_1$ linear relationships among the state variables. Accordingly, the $N$-dimensional system (10) is restricted to operate on an invariant affine hyperplane of dimension $N$-$s$. A vector z is formed with $N$-$s$ linearly independent components of $y'$. Using (6) and (11) to express the remaining $s$ components of $y'$ as a linear combination of the elements of z, (10) are rewritten as

$$\frac{dz}{d\tau} = A_1 F(z) + A_2 F(P_1 z + P_o) + A_o \tag{12}$$

for suitable matrices $A_1$, $A_2$, $P_1$, $A_o$ and $P_o$. These nonlinear differential equations qualitatively capture the dynamics under study, as confirmed next.

## 4. Theory validation

The fast dynamics due to the parasitic capacitances are responsible for the emergence of the external nonlinear behavior. Figs. 4-9 compare a number of PSpice simulation results of the circuit of Fig. 3 with the corresponding Matlab numerical solutions of (12), in which the parasitic capacitance $C$ is set to 10 pF. The nonlinear behavior of the system is studied on the $V_{CF3}$-$V_{CF2}$ plane. The low-pass filter of Fig. 3 ideally features a maximum pass-band ripple width of 1dB and a cut-off frequency of 3 MHz if the circuit parameters are chosen as follows: $C_{F1} = C_{F3} = 0.2$ nF, $C_{F2} = 0.1$ nF and $I_o = 100$ μA. However, such a circuit may lose external linearity even for zero input. In fact, a slight perturbation of the autonomous system away from its equilibrium gives rise to undesired oscillations (Fig. 4). As circuit parameter $C_{F1}$ is incremented in small steps, the circuit experiences a number of interesting dynamical behaviors. Fig. 5 presents the period-two limit-cycle observed in PSpice for $C_{F1} = 0.55$ nF and in Matlab for $C_{F1} = 0.701$ nF. Increasing the bifurcation parameter further, the period-two limit cycle becomes unstable and a period-four cycle is born as $C_{F1}$ is set to 0.58 nF in PSpice and to 0.78 nF in Matlab (Fig. 6). Finally, chaos is detected for $C_{F1} = 0.585$ nF in PSpice and for $C_{F1} = 0.797$ nF in Matlab (Fig. 7). Chaotic behavior is observed even for different values of the system parameters. For example, setting $C_{F1}$ to 1.6 nF, the system experiences chaotic behavior for $\alpha_F = 0.988$ in PSpice and for $\alpha_F = 0.984$ in Matlab (Fig. 8). In this case, Fig. 9 depicts the dynamic input-output behavior of cell $N_1$, as obtained in PSpice (left) and Matlab (right). Clearly, cell $N_1$ does not act as a simple static exponential nonlinearity, in contradiction with (2). Fig. 9 indicates that the proposed BJT dynamic model of Fig. 2 qualitatively describes the input-output behavior of a cell.

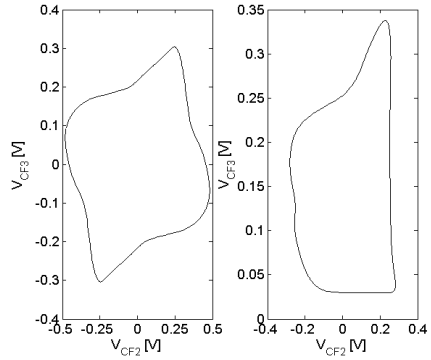


Fig. 4 Period-one limit-cycle ($C_{F1} = 0.2$ nF). Left: PSpice circuit simulation. Right: Numerical integration of (12).

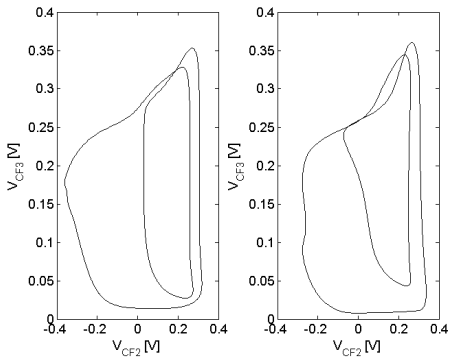


Fig. 5 Period-two limit cycle. In PSpice $C_{F1} = 0.55$ nF (left), while in Matlab $C_{F1} = 0.701$ nF (right).

## 5. Conclusions

In this paper a BJT dynamic model is used to explain the rich nonlinear dynamics recently observed in a third-order log-domain filter. The circuit equations, based upon this

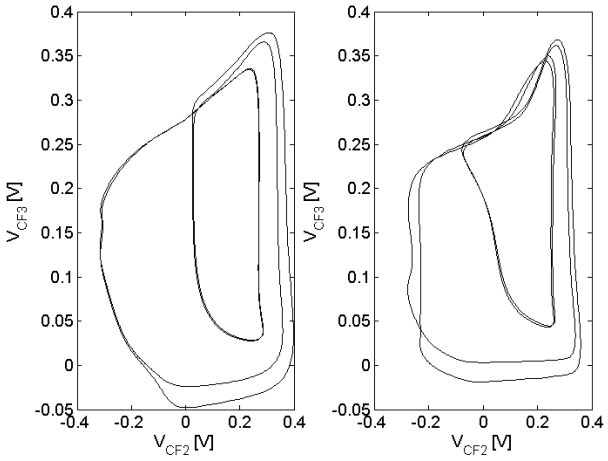


Fig. 6 Period-four behavior. Left: PSpice simulation result for $C_{F1}$ = 0.58 nF. Right: Numerical solution of (12) with $C_{F1}$ = 0.78 nF.

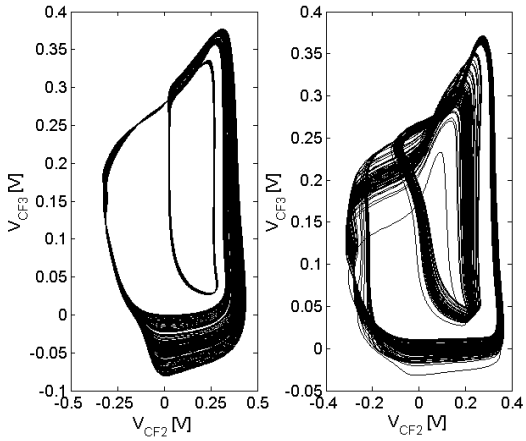


Fig. 7 Chaotic attractor. Left: PSpice simulation result for $C_{F1}$ = 0.585 nF. Right: Numerical integration of (12) with $C_{F1}$ = 0.797 nF.

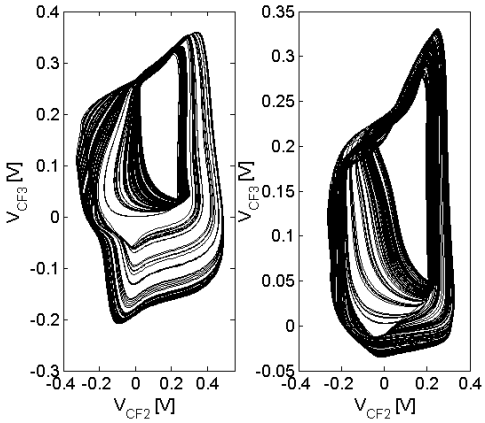


Fig. 8 Chaotic attractor of the autonomous system for $C_{F1}$ = 1.6 nF. Left: PSpice simulation result for $\alpha_F$ = 0.988. Right: Matlab numerical solution to (12) for $\alpha_F$ = 0.984.

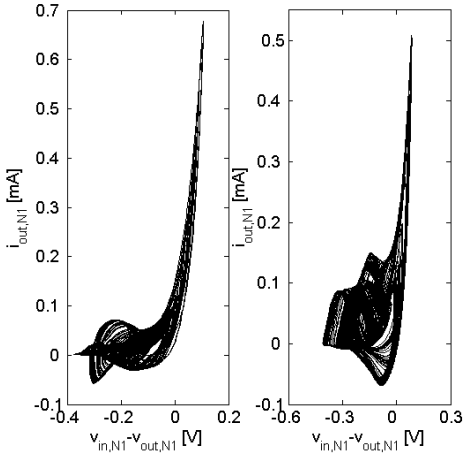


Fig. 9 Dynamic nonlinearity introduced by $N_1$ in the circuit of Fig. 3 for $C_{F1}$ = 1.6 nF. PSpice (left, $\alpha_F$ = 0.988) and Matlab (right, $\alpha_F$ = 0.984) simulations.

model, are numerically integrated and the corresponding solutions are compared with PSpice circuit simulations to validate the theory. It is important to note that the circuit equations, based upon any plausible static BJT model, are unable to explain any dynamic behavior [5]. The reason for the failure of the BJT static model is due to the important role played by BJT parasitic capacitances, which strongly affect the dynamics of the system.

## References


[1] D.R. Frey: "Log-domain filtering: an approach to current-mode filtering", *IEE Proc.-G*, vol. 140, no.6, pp.406-416, Dec. 1993

[2] G. W. Roberts and V. W. Leung: "Design and analysis of integrator-based log-domain filter circuits", Kluwer Academic Publishers, Norwell, Massachusetts, 2000

[3] E. Ferrer and R.M. Fox: "Limit-cycle oscillations in a log-domain-based filter", *IEEE Trans. on Circuits and Systems-II*, vol. 46, no. 6, pp.832-836, 1999

[4] A. Ascoli, O. Feely and P. Curran: "Chaotic third-order log-domain filter", *Proc. of the Workshop on Nonlinear Dynamics of Electronic Systems* (NDES), pp. 75-78, 2004

[5] A. Ascoli, P. Curran and O. Feely: "On the Modeling of Log-domain LC-ladder Circuits", *Proc. of the IEEE Int. Symp. on Nonlinear Theory and its Applications* (NOLTA), pp. 243-246, 2004

[6] A. Ascoli, P. Curran and O. Feely: "A Slow-fast Dynamics Model of a Second-order Log-domain Floating-capacitor LC-ladder Circuit", to be published in the *Proc. of the IEEE Eur. Conf. On Circuit Theory and Design* (ECCTD), 2005

[7] A.S. Sedra and K.C. Smith: "Microelectronic circuits", 4th edition, Oxford University Press, New York, 1998