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A PWM-mode CMOS Threshold-coupled-map Circuit Robust to Device Mismatches

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Abstract—In order to develop large-scale coupled nonlinear dynamical systems using CMOS integrated circuits, we propose a threshold-coupled-map element circuit that is robust to CMOS device mismatch. We have already proposed a voltage- and a current-waveform-sampling-mode circuits which can achieve arbitrary analog nonlinear dynamics in the time domain by using pulse width/phase modulation (PWM/PPM) signals. The voltage-sampling-mode circuit is robust to device mismatches of CMOS circuit elements, while the current-sampling-mode circuit facilitates weighted summation. These advantages are important for developing a large-scale coupled array circuit. In this study, we propose a new circuit that is robust to DC offset voltage variation as well as current variation, by utilizing the advantage of both sampling-mode circuits. We show the robustness of the proposed circuit by an HSPICE circuit simulation.

1. Introduction

Large-scale coupled nonlinear dynamical models, which show various spatio-temporal patterns, have been proposed [1, 2, 3, 4]. Although these models are evaluated by a numerical simulation, there are few examples of CMOS circuit implementation. Our final goal is to design a CMOS circuit of the threshold coupled map [5] which is one of the large-scale coupled nonlinear dynamical models.

We have already proposed a CMOS element circuit using a pulse modulation approach that can achieve arbitrary analog nonlinear transformation in the time domain by using pulse width/phase modulation (PWM/PPM) signals [6, 7]. However, the characteristics of an element circuit are not generally equal with those of the other element circuits. This problem is caused by CMOS device mismatches including parasitic capacitance and wiring resistance.

In this paper, we propose a CMOS element circuit that is robust to DC voltage offset and current variation to overcome these problems. An HSPICE circuit simulation shows that the proposed element circuit can achieve an accurate analog nonlinear transformation even if DC voltage offset and current variations exist.

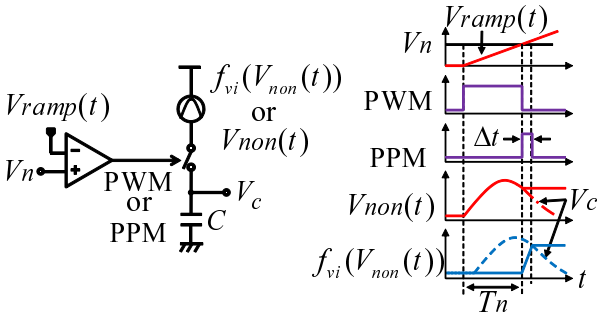

Figure 1: Circuit principle of nonlinear transformation in a voltage/current sampling waveform mode.

2. Nonlinear dynamical model with threshold coupled map

The threshold coupled map [5] performs a nonlinear transformation:

$$x_{n+1}(i) = f(x_n(i)), \tag{1}$$

where x_n is the state variable on a certain lattice site at time step n, $f(\cdot)$ is a nonlinear transformation function such as a logistic map, and i is the site index in the lattice. Then, an excess δ_i $(= x_{n+1}(i) - x_{th})$ is transported to the neighboring lattice site(s), if $x_{n+1}(i)$ is larger than threshold value x_{th}. This is given by

$$\begin{aligned} &x_{n+1}(i) \to x_{th}, \\ &x_{n+1}(i+1) \to x_{n+1}(i+1) + \delta_i. \end{aligned} \tag{2}$$

This model has several updating schemes. By changing them, we can obtain various spatio-temporal patterns.

3. Voltage/current waveform sampling approach

Figure 1 shows a principle of a voltage- and a current-sampling-mode nonlinear transformation using PWM signals. In the voltage sampling mode, state voltage V_n $(\propto x_n)$ at time step n is transformed into a PWM signal having pulse width T_n $(\propto V_n)$. This transformation can be achieved by comparing V_n with ramped reference voltage $V_{ramp}(t)$ as

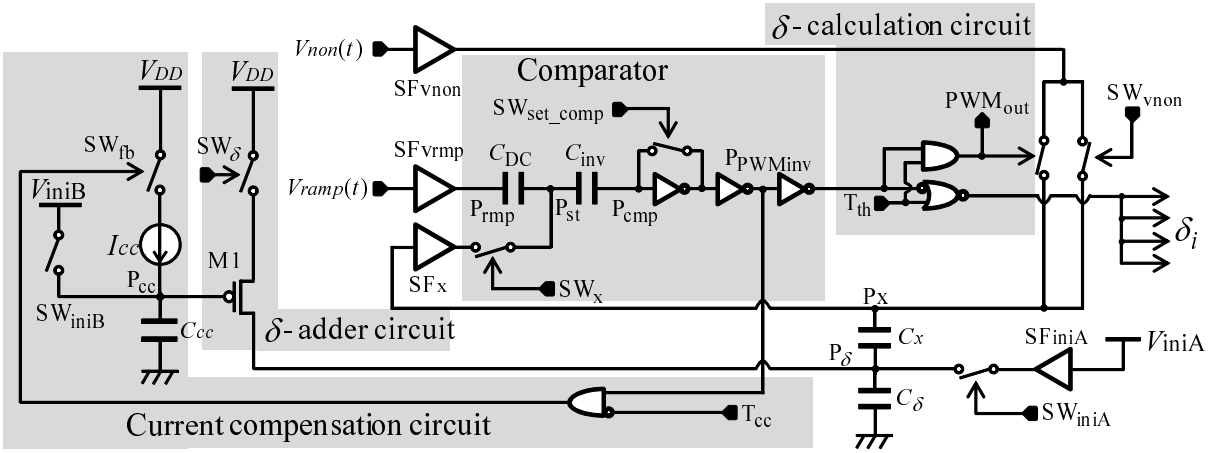

Figure 2: Proposed element circuit.

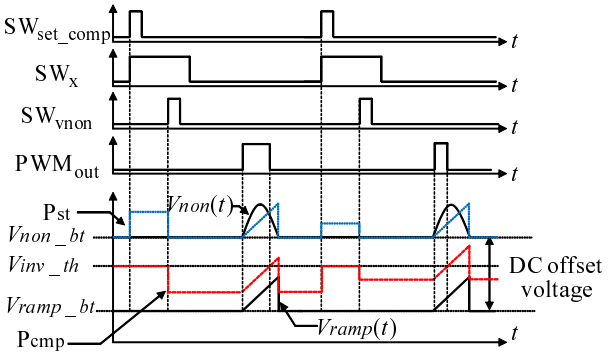

Figure 3: Timing diagram of the control signals and node voltages for nonlinear transformation with DC offset cancellation.

shown in Fig. 1. Nonlinear voltage waveform $V_{non}(t)$ is sampled with this PWM signal. This is given by

$$V_c = V_{non}(T_n), \tag{3}$$

where V_c is a voltage that is sampled to a capacitor. Arbitrary discrete-time analog nonlinear dynamics can be achieved by considering V_c as V_{n+1} at the next time step $(n + 1)$. Base voltage difference between $V_{ramp}(t)$ and $V_{non}(t)$ (DC offset voltage) is transformed into the offset time width of the PWM signal. This DC offset voltage is caused by the voltage shift variation of analog buffers, wiring resistance, and so on.

In the current sampling mode, a nonlinear current waveform is generated by converting a nonlinear voltage waveform $V_{non}(t)$ to current $f_{vi}(V_{non}(t))$, where $f_{vi}(\cdot)$ is the voltage-current conversion function in an MOSFET. As with the voltage sampling mode, V_n ($\propto x_n$) is transformed into the PWM signal having pulse width T_n. A PPM signal having a certain small width Δt is generated at the trailing edge of the PWM signal. A current source is switched by the PPM signal during period $[T_n, T_n + \Delta t]$, and charges up capacitor C. The capacitor voltage is given by

$$V_c \approx \frac{\Delta t}{C} f_{vi}(V_{non}(T_n)), \tag{4}$$

where the initial voltage of the capacitor C is assumed as zero. Unlike the voltage sampling mode, parameter variations of C, Δt, and $f_{vi}(\cdot)$ influence a nonlinear transformation result in the current sampling mode as shown in Eq. (4).

4. Proposed Circuit

We employ the voltage sampling mode robust to device mismatches for nonlinear transformation, and the current sampling mode, easily realizing addition and subtraction for calculating the connection states. The element circuit can be designed to be robust to a DC offset voltage and a current variation, which are the problems in respective sampling mode.

The proposed element circuit is shown in Fig. 2. The circuit is consisted of source-follower analog buffers SF_{vnon}, SF_{vrmp}, SF_x, and SF_{iniA}, a comparator robust to DC offset voltage variation, a capacitor C_x that is used in voltage sampling with PWM signals, a δ-calculation circuit, a δ-adder circuit, and a current compensation circuit. This circuit achieves nonlinear transformation robust to DC offset voltage between the base voltages: $V_{non\_bt}(t)$ of $V_{non}(t)$ and $V_{ramp\_bt}(t)$ of $V_{ramp}(t)$ that are generated from the analog buffers SF_{vnon}, SF_{ramp}, SF_x, and wiring resistance by holding at C_{DC} in the comparator. The current compensation circuit adjusts gate voltage V_p at a node P_{cc} in order that the comparator outputs a PWM signal with target pulse width T_{tgt} when SW_δ is turned on during time span T_δ.

4.1. Operation of nonlinear transformation circuit robust to DC offset voltage variation

Figure 3 shows a timing diagram of control signals and node voltages for nonlinear transformation in the proposed

element circuit. It is assumed that the signals SW_{iniA} is closed and T_{th} is fixed at "High", and the δ-adder circuit does not operate. Here, in the initial condition the output voltage of SF_x is defined as V_{X0}.

1) When SW_{set_comp} and SW_x is turned on, nodes P_{st} and P_{cmp} are set at V_{X0} and threshold voltage V_{inv_th} of the inverter in the comparator, respectively.

2) After SW_{set_comp} is turned off, SW_{vnon} is turned on, then node P_{st} is varied from V_{X0} to V_{non_bt}. At the same time, node P_{cmp} is varied from V_{inv_th} to $(V_{inv\_th}-V_{X0})$. Capacitor C_{DC} holds the voltage difference, $(V_{ramp\_bt}-V_{non\_bt})$, in this step.

3) After SW_{vnon} is turned off, SW_x is turned off. The voltage difference $(V_{inv\_th}-V_{X0})$ at node P_{cmp} is transformed into a PWM signal. This transformation can be achieved by comparing $(V_{inv\_th}-V_{X0})$ with ramped reference voltage $V_{ramp}(t)$. Nonlinear voltage waveform $V_{non}(t)$ is sampled to C_x by PWM_{out}. (see PWM_{out} as shown in Fig. 3).

4.2. Operation of current compensation circuit

Figure 4 shows a timing diagram of control signals and node voltages for current compensation operation. Gate voltage of the M1, V_p, shown in Fig. 2 is adjusted in order to minimize the difference of the time width between target pulse width T_{tgt} and T_{PWM_δ}, where T_{PWM_δ} is defined as the time width of the PWM signal output from the comparator, which corresponds to the voltage V_δ. The voltage V_δ is a shift voltage at a node P_δ when SW_δ is turned on during T_δ. The δ-calculation circuit does not operate during current compensation operation, and $V_{non}(t)$ is fixed at the base voltage $V_{non\_bt}(t)$. The current compensation operation is as follows:

1) In order to initialize nodes P_x, P_δ, P_{st}, and P_{cmp}, SW_{set_comp}, SW_x, SW_{iniA}, and SW_{vnon} are turned on.

2) After SW_{set_comp}, SW_{iniA}, and SW_{vnon} are turned off, SW_δ is turned on during pulse width T_δ. Nodes P_δ, P_x, P_{st}, and P_{cmp} are shifted up by V_δ.

3) After SW_x is turned off, $V_{ramp}(t)$ is decreased linearly. The comparator generates an inverted PWM signal during time width T_{PWM_δ} corresponding to V_δ. The node P_{cc} is charged up during the difference of the time width $(T_{PWM\_\delta}-T_{tgt})$.

4) Repeat 1) to 3) until $(T_{PWM\_\delta}-T_{tgt})$ is minimized.

This current compensation circuit has only the current source for charging up V_p. Therefore, the initial voltage of V_p has to be set sufficiently low.

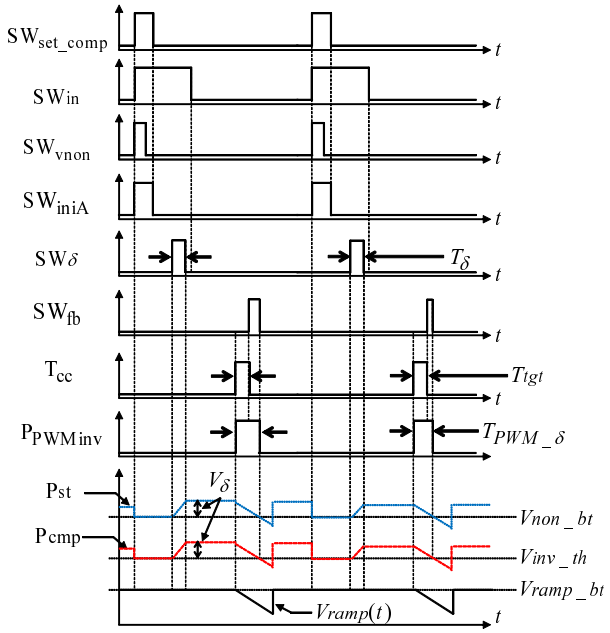

Figure 4: Timing diagram of control signals and node voltages for current compensation.

5. Circuit simulation results in HSPICE

5.1. Nonlinear transformation circuit

We conducted a circuit simulation of the proposed element circuit for evaluating robustness to DC offset voltage variation using the TSMC 0.25 μm CMOS process parameters. The capacitance values were set as follows: $C_{DC} = C_{inv} = 0.225$ pF, $C_x = 0.1$ pF, $C_\delta = 2.0$ pF, and $C_{cc} = 0.5$ pF. Logistic map $(x_{n+1} = \alpha x_n(1-x_n))$ was used as a nonlinear transformation, where $\alpha = 4$ in the simulation. The time width of the PWM signal expressing the maximum state value was set to 2,600 ns. In order to evaluate the precision of nonlinear transformation, the bit precision was calculated by using the mean squared error between a fitting function and a return map obtained from the simulation results. A logistic map was used as a fitting function. The amplitude of $V_{ramp}(t)$ and V_{ramp_bt0} that is the base voltage before inputting into SF_{vrmp} at the input stage were fixed at 1.3 V and 1.6 V, respectively. The amplitude of $V_{non}(t)$ was fixed to 1 V. In order to show the robustness to DC offset voltage variation, V_{non_bt0} that is the base voltage before inputting into SF_{vnon} was varied as follows: $V_{non\_bt0} = 1.6, 1.7, 1.8$ V, which means that the ratios of the DC offset voltage to the amplitude of $V_{non}(t)$ are 0%, 10%, and 20%, respectively.

Figure 5 shows simulation results in HSPICE. The obtained return map was nearly unchanged when the DC offset voltage changed, although the ratio of the DC offset voltage to the maximum amplitude was 20 % (see the case of $V_{non\_bt0} = 1.8$ V). In all cases, the bit precision were more than 8 bits.

Table 1: The voltage V_p at the node P_{cc}, and the pulse width T_{PWM_δ}.

V_p(V)	$n = 0$	0.4	0.5	0.6	0.7	0.8
	$n = 17$	1.022	1.022	1.023	1.023	1.023
T_{PWM_δ} (ns)		398.6	398.5	398.6	398.6	398.5
ϵ (ns)		1.4	1.5	1.4	1.4	1.5

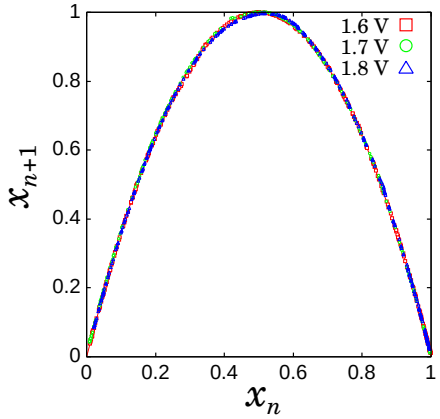

Figure 5: Circuit simulation results of return maps for different DC offset voltages between V_{non_bt0} and V_{ramp_bt0}.

5.2. Current compensation circuit

We conducted a circuit simulation of the current compensation circuit for $T_{tgt} = T_\delta = 400$ ns, where the update step of V_p is defined as time step n.

Figure 6 shows time-series of T_{PWM_δ}, which starts from different initial voltages. As shown in Fig. 6, T_{PWM_δ} were converged to T_{tgt} at $n = 5$.

Table 1 shows node voltages V_p, T_{PWM_δ} and difference ϵ ($= T_{tgt} - T_{PWM\_\delta}$), which start from different initial voltages. In all cases, the differences of ϵ were smaller than 1.5 ns. This means that the compensation precision was more than 10 bits for the maximum time span (2,600 ns) of the state variable.

6. Conclusions

We proposed a nonlinear transformation circuit robust to DC voltage variation, and a current compensation circuit. The element circuit was designed including these circuits for realizing coupled array CMOS chaos circuits. The HSPICE circuit simulation results showed that the designed circuit operates at a bit precision of more than 8 bits, and the compensation precision of the current compensation circuit is more than 10 bits even if DC voltage offset and current variation exist.

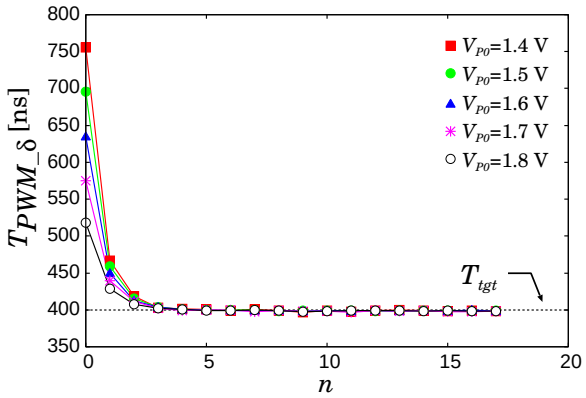

Figure 6: Time-series T_{PWM_δ} obtained from HSPICE circuit simulation.

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