

# Design, Simulation and Measurement of a 120GHz On-Chip Antenna in 45nm CMOS for High-Speed Short-Range Wireless Connectors

Noël Deferm and Patrick Reynaert

KU Leuven ESAT/MICAS, Kasteelpark Arenberg 10, 3001 Leuven, Belgium

**Abstract**—In this paper an on-chip antenna solution for high-speed millimeter wave wireless integrated transceivers in CMOS is presented. Accurate design and analysis of the complete 3D antenna structure has lead to an efficiency as high as 69% and an input bandwidth of 48GHz. A peak antenna gain of 4.4dBi is also achieved. The bondwire dipole is fabricated on a 45nm CMOS chip as part of a fully integrated 120GHz wireless communication front end. Measurements of the E-plane and H-plane radiation pattern are in good agreement with the simulation results.

**Index Terms**—Millimeter-wave, on-chip antenna, CMOS.

## I. INTRODUCTION

Recent developments in the CMOS process technology enable the design of fully integrated mm-wave data transmitters for short range communication. The scaling of the CMOS transistors has lead to an increase of the devices  $f_t$  and  $f_{max}$ , which allows the implementation of integrated mm-wave systems. These high frequencies enable the use of a high available bandwidth.

One of the most important building blocks in integrated wireless transceivers is the antenna as it provides the interface to the transmission channel. The performance of the antenna can have a large impact on the bandwidth and SNR of the transceiver. Therefore, accurate antenna design and analysis is essential in the development of a mm-wave wireless transceiver.

As the wavelength of the transmitted carrier is scaled down to the order of millimeters, antennae dimensions become comparable to chip dimensions. This leads to the possibility of integrating antennas in the same package, or even on the same die as the integrated circuits. Of course, integration of an antenna in a standard CMOS technology imposes restrictions on the geometrical properties of the antenna, making the design challenging.

Fully integrated planar antennas were already presented in the past [1]. Despite their high factor of integration, their performance suffers from the geometrical and physical technology limitations. Due to the large difference in permittivity between the air and the silicon substrate, the largest part of the radiated power gets trapped in the silicon chip in the form of surface waves. Due to the lossy substrate, part of the surface wave power is dissipated in the silicon. The finite dimensions of the chip result in radiation of the remaining surface wave power at the edges of the chip, which disturbs the radiation pattern of the antenna. To deal with the problem of surface waves, several techniques are already discussed in literature. One technique is to apply back etching of the silicon chip to prevent the generation of surface waves (figure 1(a)) [2]. Unfortunately, this technique results in a reduction of the mechanical stability of the chip, which is undesirable. Moreover, post processing steps are required to create the back cavity in the substrate.

This has to be avoided for a high volume target application. Another technique, which does not incorporate post processing of the silicon chip itself, is to add a silicon lens at the backside of the chip to convert the surface wave power to useful radiated power (figure 1(b)) [3]. The problem with this technique is the assembly of the complicated structure with the dielectric lens on which the chip has to be mounted. Several materials have to be assembled and aligned accurately, which is a time consuming and costly post processing step.

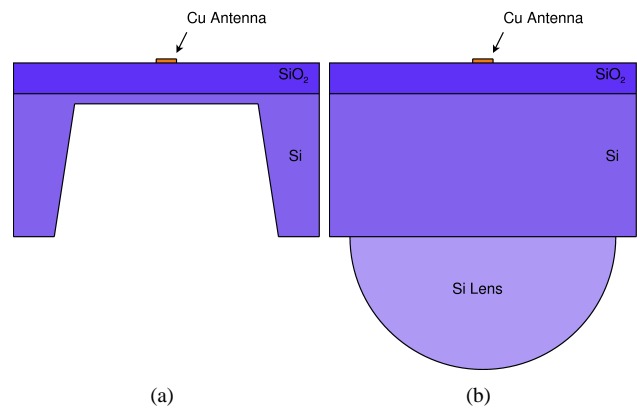


Fig. 1: Integrated antenna with silicon backetching (a) and silicon lens (b).

The solution discussed in this paper, places a reflector between the antenna and the substrate, rather than underneath the substrate. This prevents the entrapment of the radiated power in the substrate as surface waves. The only way to accomplish this when the radiating element is designed in the top metal layers, is to design the reflector shield in the lower metals of the CMOS metalstack. Due to the geometrical limitations of a standard CMOS technology, the distance between the antenna and the reflector is greatly reduced to a couple of micrometers. The small antenna-reflector spacing results in a vast reduction of the radiation resistance. The overall antenna resistance will therefore be dominated by the ohmic losses in the copper structure, resulting in an even lower radiation efficiency [3].

An elegant technique to increase the antenna-reflector spacing is to implement a full three dimensional structure by means of bond wires [4]. In this way, both the antenna efficiency and directivity can be increased. Although this solution is not a completely integrated solution, the antenna can still be included in the same package without any additional processing steps. Also, the impact of the variation on the antenna dimensions and position are rather limited, making this a very attractive solution for integrated mm-wave wireless communication systems and mm-wave laboratory chip measurement setups.

## II. ANTENNA DESIGN AND ANALYSIS

In this section, the design and analysis of the presented 120GHz bondwire dipole is discussed. It is a complete 3D structure as part of the radiating elements are lifted 500 $\mu\text{m}$  with respect to the substrate and reflector. Figure 2 shows the 3D view of the bondwire dipole.

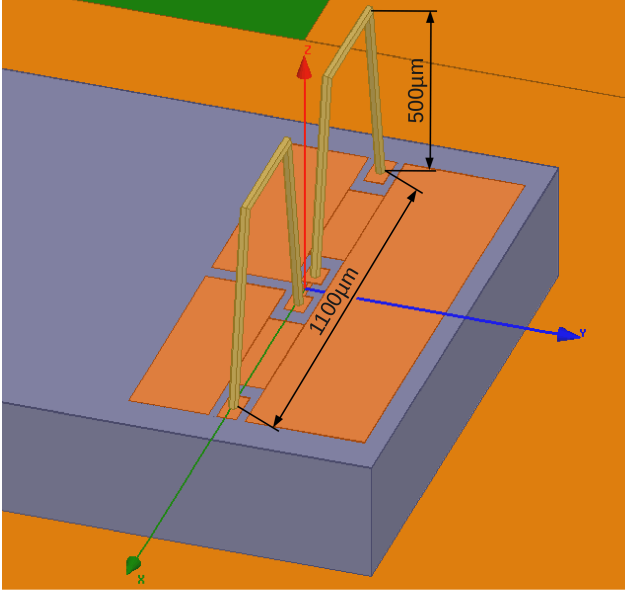


Fig. 2: 3D view of the bondwire dipole.

The bondwire antenna is mounted on a 45nm CMOS silicon chip. The chip itself will be mounted on an FR4 carrier. The dimensions of the chip and the interaction with the FR4 carrier will have a large impact on the antenna performance, so they have to be taken into account in the simulation of the antenna. To make a fair comparison between different antenna types, typical dimensions were chosen for the chip on which a complete CMOS transceiver is integrated. The dimensions of the FR4 carrier were chosen as large as possible while maintaining an acceptable simulation time. The complete structure together with the antenna is simulated in Ansoft HFSS. In figures 3 and 4 the front and top view of the silicon chip mounted on the FR4 carrier with copper ground plane are respectively shown. Intuitively one can see that this ground plane will behave as a reflector for electromagnetic waves with a wavelength significantly smaller than the ground plane dimensions. This will result in a shift of the main lobe of the radiation pattern along the z-axis.

Figure 5 shows the 3D radiation pattern of the bondwire dipole. The peak gain of 4.4dBi is pointing in the positive z-direction. There are also 2 large side lobes pointing in the x-direction under an angle of 70° compared to the z-axis. Peak gain of the side lobes is around 3.4dBi. The high directivity of the antenna results in a narrow main lobe. The radiation efficiency of this bondwire dipole is 69%.

The antenna is resonant at 30GHz with an input impedance of approximately 50 $\Omega$ . The input impedance at 120GHz is 69-22j $\Omega$ . Figure 6 shows the input impedance over frequency. Input bandwidth under conjugate match at 120GHz ranges from 107GHz up to 155GHz. Apart from the input bandwidth of the

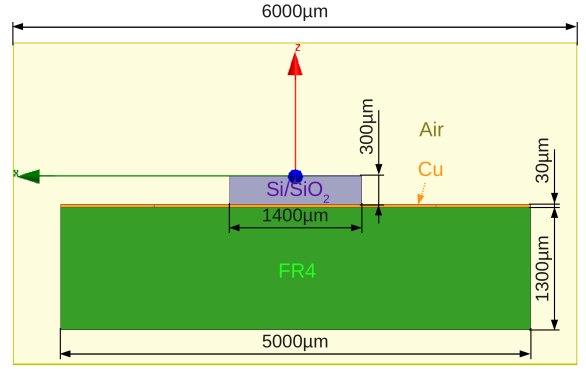


Fig. 3: Front view of the silicon chip on PCB carrier with reflector.

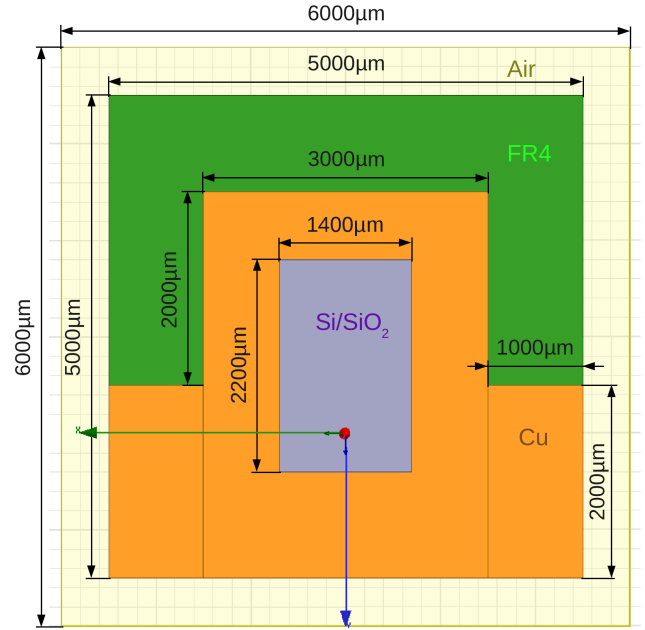


Fig. 4: Top view of the silicon chip on PCB carrier with reflector.

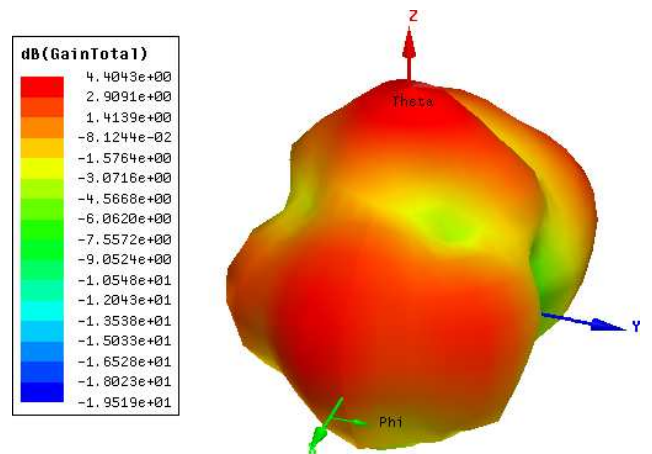


Fig. 5: 3D radiation pattern of the bondwire dipole.

antenna, the 3dB antenna gain bandwidth also plays an important role when the target application is data communication. The 3dB gain bandwidth of the antenna is depicted in figure 7 and is ranging from 107 up to 140GHz. The large antenna

gain bandwidth leads to very reliable operation when integrated together with the power amplifier. Ideally, the center frequency of the PA should be located near the center of the antenna gain bandwidth. Uncertainties in the fabrication of the antenna can lead to a shift of the bandwidth. Thanks to the large gain bandwidth, variations of the antenna center frequency and PA center frequency due to variations in the fabrication process can be tolerated.

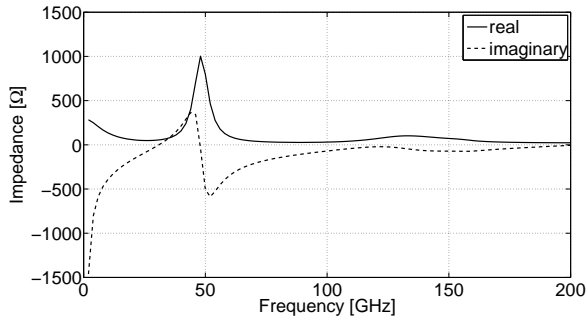


Fig. 6: Antenna input impedance as a function of frequency.

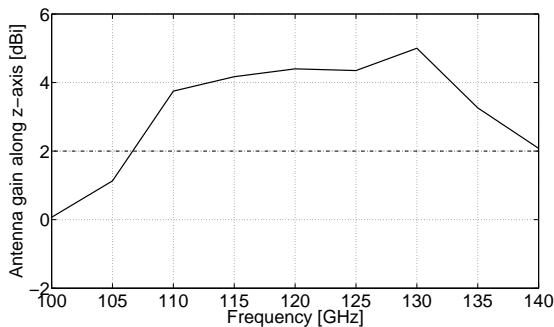


Fig. 7: Antenna gain as a function of frequency.

The main antenna characteristics are highly depending on the shape and dimensions of the antenna. Therefore, changes in the shape or dimensions as a result of variations in the fabrication process will have an impact on the electromagnetic properties of the antenna. Manufacturing the bondwire dipole antenna is a semi-automatic process of which the bondwire positions in the XY-plane can be controlled with an accuracy of one to several micrometers. The height of the bondwire however, cannot be controlled with the same accuracy. To have an idea of the sensitivity of the antenna to height variations, simulations were performed in which the height of the bondwire antenna was swept. When a height variation of 100 $\mu\text{m}$  around the optimal value of 500 $\mu\text{m}$  is considered, the antenna gain in the z-direction only varies between 3.7 and 4.4dBi. For the same height variation, the radiation efficiency varies between 60% and 69%. In figure 8 the variation of the antenna gain in the z-direction and the radiation efficiency are shown for a height sweep from 200 $\mu\text{m}$  up to 950 $\mu\text{m}$ .

The antenna behaves like a double wave dipole of which the frequency of first resonance is approximately 30GHz. When a height variation from 400 $\mu\text{m}$  to 600 $\mu\text{m}$  is considered, the resonance frequency varies between 29GHz and 34GHz. The

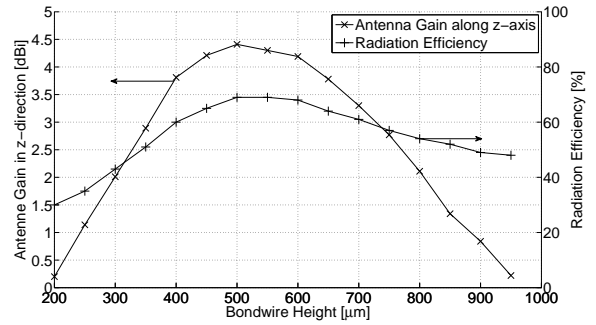


Fig. 8: Simulated variation of the antenna gain and efficiency with respect to the bondwire height.

frequency variation over the complete height sweep is shown in figure 9. Thanks to its large bandwidth, frequency shifts resulting from fabrication process variations can be tolerated up to a value of 20GHz.

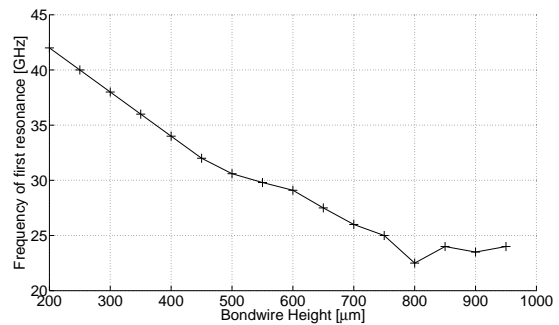


Fig. 9: Simulated variation of the antenna resonance frequency with respect to the bondwire height.

### III. MEASUREMENTS

The bondwire dipole antenna is part of a complete 120GHz transmitter with an on-chip 120GHz LO generator (figure 10) [5]. By integrating the mm-wave signal generation circuits on the same chip as the antenna, the use of probes can be omitted. Without the on-chip signal generator, a large probe (typically in the order of a couple of cm) is needed to drive the antenna. The presence of this probe would have a severe impact on the antenna radiation pattern and efficiency, which impedes the characterization of the stand-alone antenna. To measure the antenna, a continuous wave signal is generated on-chip and applied to the input of the antenna. Measurements show that optimal performance of the transmitter is achieved for a carrier frequency of 114.3GHz, so the analysis of the measured antenna radiation pattern will be carried out at this frequency.

To measure the antenna properties, the on-chip generated and radiated 114.3GHz signal has to be captured and converted down. Figure 11 shows the measurement setup to characterize the bondwire antenna. An F-band SGH antenna is used to receive the transmitted 114.3GHz signal. A wideband mixer, driven by a 59.65GHz external signal, is used to convert the received signal down to an IF of 5GHz. This IF signal is subsequently analyzed with a spectrum analyzer.

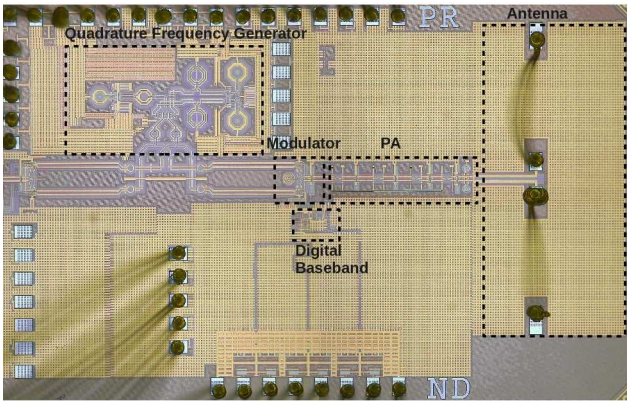


Fig. 10: Chip photograph of the 45nm CMOS 120GHz transmitter with bondwire antenna.

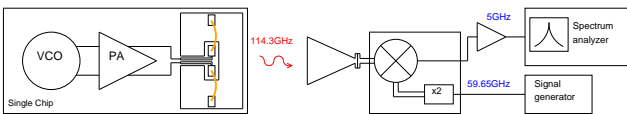


Fig. 11: Block diagram of the radiation pattern measurement setup.

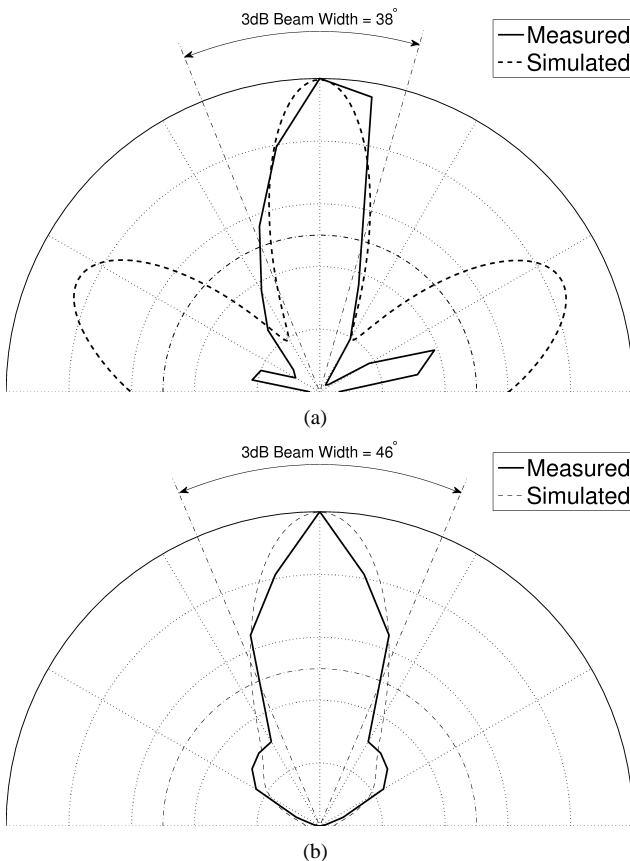


Fig. 12: Measured and simulated normalized E-plane (a) and H-plane (b) radiation pattern of the bondwire dipole at 114.3GHz.

To measure the E-plane and H-plane radiation pattern of the antenna, the chip is respectively rotated around the y-axis and x-axis according to figure 2. Figures 12(a) and 12(b) respectively show the E-plane and H-plane radiation patterns of the antenna. To compare the measured and simulated patterns, normalized

values are plotted on the graphs. Good agreement is achieved for both main lobes. Measurements show an electrical field main lobe beam width of  $38^\circ$  and a magnetic field main lobe beam width of  $46^\circ$ . In figure 13 a picture is shown of the golden bondwire dipole, manufactured on a 45nm standard CMOS silicon substrate.

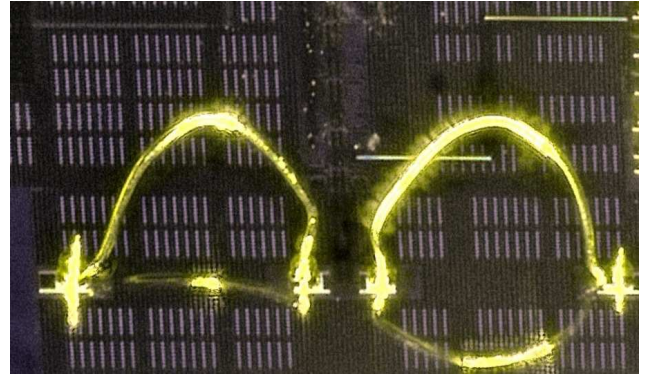


Fig. 13: Photograph of the bondwire dipole.

#### IV. CONCLUSION

In this paper, an on-chip antenna solution was presented for high-speed integrated mm-wave CMOS transceivers. The bondwire dipole was designed as part of a 120GHz integrated transmitter, fabricated in a 45nm low power CMOS technology. Accurate design and analysis of the 120GHz 3D antenna structure and carrier in Ansoft HFSS was carried out. The antenna occupies an area of  $1100\mu\text{m}$  by  $600\mu\text{m}$ . The radiating elements are lifted  $500\mu\text{m}$  with respect to the silicon substrate and reflector which has lead to a radiation efficiency of 69% and an antenna gain of 4.4dBi. Also, an input bandwidth of 48GHz was achieved.

#### ACKNOWLEDGMENT

This research is partly supported by the ERC Advanced Grant 227680, the CHIPS K.U.Leuven Program Financing (Circuit design for smart and high-performance electronic systems). Furthermore, the authors would like to thank NXP research Eindhoven to support this work. The authors also thank the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT Vlaanderen).

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