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Brain-like Synaptic Oxide Thin-Film Transistors Gated by Solid Electrolytic Gate Insulators

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Abstract– Synaptic oxide thin-film transistors (TFTs) using two types of solid electrolytic gate insulators were fabricated and characterized for realizing the brain-like synaptic operations. The channel conductance of synaptic TFTs was gradually modulated upon applied input pulses with variations in pulse width, pulse amplitude and number of pulses by the movement of ions in electrolytic gate insulators. The synaptic operations including short-term memory and decay behavior were well emulated for both synaptic TFTs. The synaptic TFTs employing an oxide channel and electrolytic gate insulator could be expected to be promising synapse devices for large-area electronics.

1. Introduction

As the advent of big data era, new computer system technology is quite demanding. According to the international technology roadmap for semiconductors, brain-like computing systems are picked up as one of the ultimate advanced systems. In conventional computing systems, data processing is sequentially performed and hence, von Neumann bottleneck is inevitable when the huge data are to be processed. On the other hand, a human brain has powerful abilities of a simple data storage and a highly-functional information processor equipped with adaptive learning, fault tolerance, and parallel data processing. Especially, it is very impressive that a human brain can be fully working even with only a few energy. Thus, parallel information processing can be performed in a brain with lower power consumption. Such advantages are highly expected to be mimicked in electronic devices, with which we can implement artificial neuromorphic systems for future information-oriented society.

In 2014, IBM released CMOS-based neuromorphic chip, called 'True North', which is composed of 5.4 billion transistors corresponding to a million neurons. In other words, several transistors are required to act as one neuron.[1)] However, one synapse device is absolutely required to be prepared by one electronic device to realize small chip size and low power consumption. Various operation mechanisms have been examined for the one-device-type synaptic elements, such as resistive change,[2)] phase change,[3)] and electrolytic ion movements[4-5)]. Among them, synapse devices with thin-film transistor configurations using electrolytic gate insulator (GI) can be promising candidates.

In this report, we propose brain-like synaptic TFTs using two polymer electrolytes of Li incorporated poly(propylene carbonate) (Li:PPC) and poly(4-vinylphenol)-sodium beta-alumina (PVP-SBA) as GIs. In preliminary studies, the Li:PPC and PVP-SBA thin films were verified to be readily formed with spin-coating process and patterned by conventional photo-lithography and etching processes. It was also found that the obtained their physical and electrical properties are appropriate for the uses as GIs for the proposed synaptic TFTs. In-Ga-Zn-O (IGZO) was selected as an active channel layer due to such advantages as high field-effect mobility and on/off ratio even at a low process temperature.

This paper includes three parts; the first section explains the simple mechanism of the synaptic TFTs employing electrolytic GIs. Then, the synaptic operations of the Li:PPC synaptic TFTs are evaluated and characterized. The last part describes the PVP-SBA synaptic TFTs in a detailed way. The proposed synaptic TFTs using Li:PPC and PVP-SBA electrolytic GIs exhibited excellent brain-like operations such as paired-pulse facilitation (PPF), short-term memory (STM), long-term memory (LTM), and decay characteristics.

2. Experimental section

For the preparation of Li:PPC solution, PPC and $LiClO_4$ was dissolved in a propylene carbonate (PC) solvent with 10 and 0.5 wt%, respectively. The prepared Li:PPC solution was spin-coated at 4000 rpm for 30 s. They were baked at 75 ^oC for removing the PC solvent. The PVP solution was prepared by dissolving PVP in propylene glycol monomethyl ether acetate (PGMEA) solvent with 6.25 wt%. The SBA solution was also prepared by using solutes of bisulfate and aluminum nitrate hexahydrate and solvent of 2-methoxyethanol. Two solutions were blended in a volumetric ratio of 70/30 for PVP-SBA precursor. The spin-coating conditions were set as 2000 rpm for 30 s. Two steps of baking for removing the solvent and cross-linking the PVP were successively carried out at 100 ^oC and 200 ^oC, respectively.

Top- and bottom-gate synaptic TFTs using Li:PPC or PVP-SBA electrolytic GIs were fabricated with following procedures, respectively. ITO-coated glass substrates were

used as source/drain (S/D) and gate electrodes for the Li:PPC and PVP-SBA synaptic TFTs, respectively. The 20-nm-thick IGZO and 9-nm-thick atomic-layer-deposited Al_2O_3 thin films were formed as active and protection layers before and after the formation of electrolytic GIs for the Li:PPC and PVP-SBA synaptic TFTs, respectively. The 150 nm-thick ITO layers were deposited and patterned as gate and S/D electrodes for the Li:PPC and PVP-SBA synaptic TFTs, respectively. Figures 1(a) and 1(b) shows the device schematics of fabricated synaptic TFTs using Li:PPC and PVP-SBA electrolytic GIs.

Device characterizations for the fabricated Li:PPC and PVP-SBA synaptic TFTs were evaluated by using a semiconductor parameter analyzer (Keithley 4200SCS), pulse generator (HP 8110 A), and digital oscilloscope (Tektronix, MSO 4104) in an air ambient at room temperature.

3. Results and discussions

3.1 Operation principle of synaptic TFTs using electrolytic gate insulators

In a biological system, a synapse is a signal passage between two neurons which is a basic cell of neural system. The degree of connection between neurons changes with the application of external stimuli as the neuro-transmitters are released from pre-synapse to post-synapse. Here, the degree of connection is called 'synaptic weight'. In an artificial neuromorphic system, synaptic device emulates the functions of a biological synapse. Thus, the synaptic weight can be modulated as variations in channel conductance. Gate voltage pulses are applied to the gate terminal (pre-synapse) as input signals corresponding to external stimuli and drain currents are measured at the drain terminal (post-synapse) as output signals corresponding to response. As results, the output drain current of the synaptic device can be modulated by designed variations of input pulses.

For the synaptic TFTs using electrolytic GIs, positively-charged mobile ions drift to the channel/GI interface when the positive input pulses are applied to the gate terminal. Then, the conduction electrons within the IGZO channel can be coupled with drifted ions and a larger number of carriers can be accumulated in the IGZO channel with the evolution of input pulse applications. The drain currents gradually increase as the increase in the total amounts of drifted ions. At the end of the input pulse trains, electrostatic coupling effect vanishes and the ions gradually return to initial positions. The output drain currents also inversely decrease to initial values. Consequently, the values of output drain currents of the synaptic TFTs can be gradually modulated by controlling the amounts of drifted ions with various pulse conditions.

The synaptic weights adjusted in biological synapses changes upon external signal spikes. When stronger, longer, larger number of spikes are applied to the synapse, the synaptic weights can be expected to more quickly change their values. To evaluate the device operations of the proposed synaptic TFTs, we designed variables such as pulse voltage, pulse width, and the number of pulses to emulate the real conditions of external stimuli and investigated the effects of these variables on the synaptic operations.

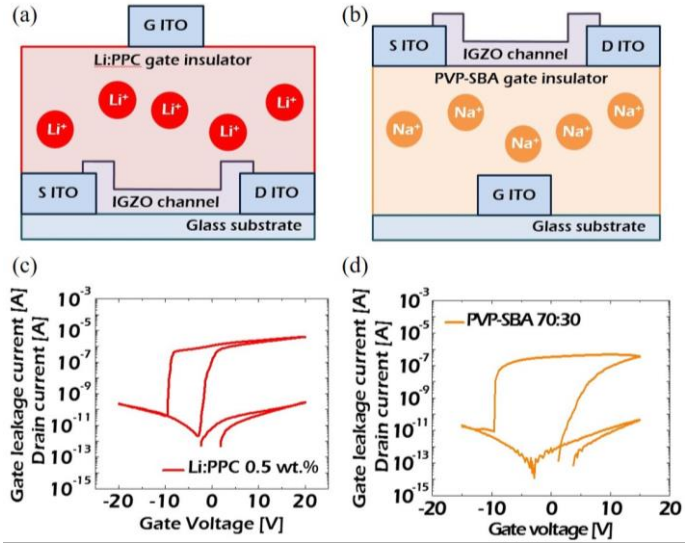

Fig. 1. Cross-sectional schematics and I_{DS}-V_{GS} transfer characteristics of the synaptic TFTs using (a, c) Li:PPC and (b, d) PVP-SBA electrolytic GIs.

3.2 Li:PPC synaptic TFTs

First, the proposed synaptic TFTs were implemented by using Li-incorporated PPC electrolytic GI and a-IGZO channel layer. Fig. 1(c) shows the typical I_{DS}-V_{GS} transfer characteristic. The transfer curve showed counter-clockwise hysteresis owing to the movements of Li ions within the PPC. Figs. 2(a) and 2(b) shows the variations in the output drain currents with the evolution of input pulse trains when the input pulse width was varied to 100 and 500 ms, respectively, in which the pulse amplitude was 10 V. After the application of 5-times input pulse trains with a pulse width of 100 ms, the increased output drain currents completely disappeared during 1 s. On the other hand, the time to decay was extended to 8 s when the pulse width was 500 ms. In this operation, the pulse width and time-dependent decrease in output drain current in a synaptic TFT correspond to the learning time at a single event and loss of memory in a bio-synapse. Fig. 2(c) shows the estimated decay times for the output drain current as a function of total pulse time which is a summation in width of 5-times pulse trains. As can be seen in a figure, the learning effect remains for longer duration when the learning events are performed for longer time. Thus, the Li:PPC synaptic TFTs exhibited the pulse-width dependence of applied pulse signals on the decay time characteristics of the output drain currents, which suggests the learning-time effect on memory persistence.

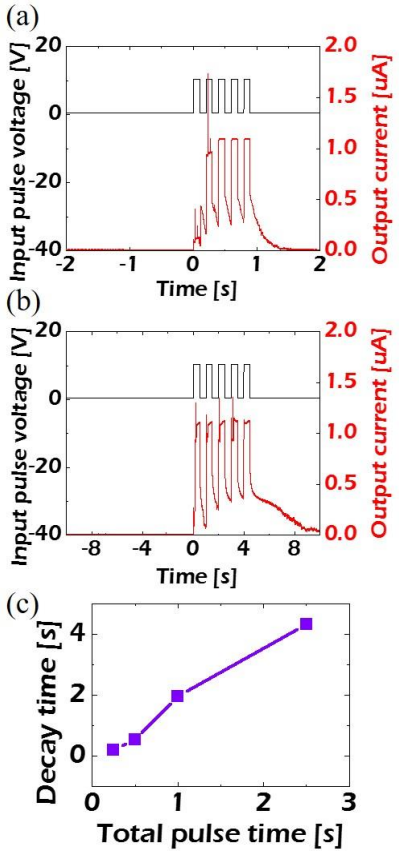

Fig. 2. Variations in output drain current as progress of 5-times input pulse trains with a pulse width of (a) 100 and (b) 500 ms. (c) Estimated decay times as a function of total pulse time.

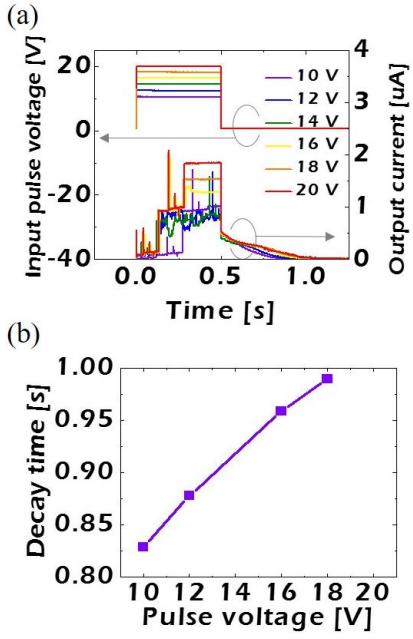

Fig. 3. (a) Waveforms of output pulse signals at an application of single input pulse with various amplitudes from 10 to 20 V. (b) Estimated decay times as a function of input pulse amplitude.

Pulse amplitude modulation effects were also investigated. Fig. 3(a) shows the waveforms of output drain currents obtained when the amplitude of a single input pulse was varied from 10 to 20 V. At an application of input pulse with a higher pulse amplitude, the number of drifted Li ions increases, and hence larger output drain current and longer decay time were obtained, as shown in Fig. 3(b). These behaviors well demonstrate the learning effect for the Li:PPC synaptic TFTs according to the degree of intensity in external stimuli.

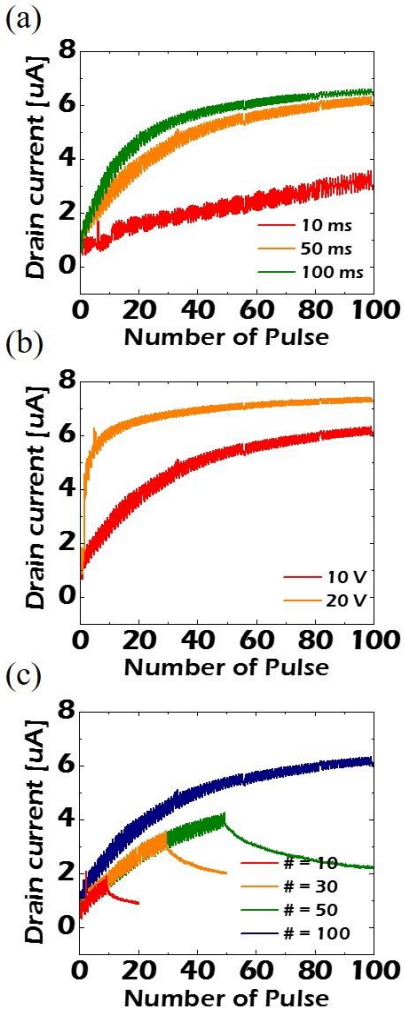

Fig. 4. Variations in output drain currents upon modulating the input pulse conditions of (a) pulse width, (b) pulse amplitude, and (c) number of pulses.

3.3 PVP-SBA synaptic TFTs

The synaptic IGZO-TFTs using PVP-SBA electrolytic GI were also fabricated with bottom-gate bottom-contact structures, as shown in Fig. 1(b), in which counterclockwise hysteresis in transfer curves were obtained owing to the movements of mobile sodium ions, as shown in Fig. 1(d).

The synaptic operations of the fabricated synaptic TFTs were investigated with the variations in width, amplitude and number of input pulses. Fig. 4(a) showed the variations in the output drain currents when the pulse width was varied from 10 to 100 ms with a fixed pulse voltage of 10 V. With increasing the pulse width, larger number of ions quickly drifted and output drain currents were saturated at higher current levels even with the same number of pulses. Furthermore, the output drain currents were observed to more sharply increase with increasing the number of pulses when the input pulse amplitude was varied from 10 to 20 V with a fixed width of 50 ms, as shown in Fig. 4(b). These operations well emulate the functions of bio-synapses that a larger quantity of information can be finally available after longer learning time and for stronger learning event. Interestingly, we can also memorize much more information when we are more frequently learning. To mimic this synaptic behavior, the number of input pulses was varied from 10 to 100 with the same width (50 ms) and amplitude (10 V) conditions, as shown in Fig. 4(c). The output drain currents increased to higher current levels for larger number of applied pulses.

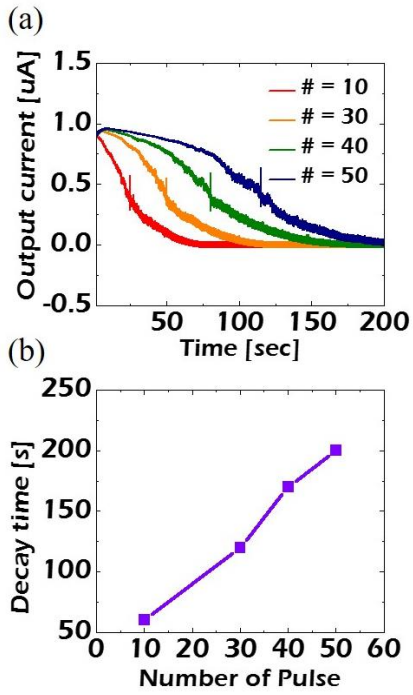

Fig. 5. (a) Decay characteristics of the output drain currents with time evolution and (b) estimated decay times as a function of number of applied input pulses.

It is interesting to investigate the decay time characteristics after learning events. Fig. 5(a) describes the decay characteristics for the saturated output drain currents. The estimated decay time increased from 60 to 200 s with increasing the number of pulses from 10 to 50, as summarized in Fig. 5(b). The fabricated synaptic TFTs emulated the memory decay functions of human brain. In other words, larger quantity of information can be memorized for longer time when the learning events are more frequently performed, even though the memory is naturally decayed with a lapse of time.

The above-mentioned learning behaviors correspond to short-term memory (STM) operations in the sense that the memory can be stored only for a short period and eventually be forgotten. However, for the proposed device, a long-term memory operation can also be available by means of electrochemical doping effect of sodium ions, as if we have unforgettable memories. The LTM behaviors will be discussed in detail at presentation.[6)]

4. Conclusions

Synaptic TFTs using electrolytic GI and a-IGZO active channel were proposed and fabricated. The Li incorporated PPC and PVP-SBA were chosen as electrolytic GIs for exploiting the free drifts of mobile Li^+ and Na^+ ions, respectively. First, the device feasibility of Li:PPC synaptic TFT was verified as the modulations in output drain currents with varying the width and amplitude of input pulse trains. Then, the suitable choice of PVP-SBA as electrolytic GI markedly improved the device characteristics of the proposed synaptic TFTs. As results, the synaptic behaviors such as short-term memory operations and decay time characteristics could be clearly obtained for the PVP-SBA synaptic TFTs. Consequently, we can conclude that the proposed synaptic TFTs using electrolytic GIs have great potentials to applications in ultra-low power flexible artificial neuromorphic systems.

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