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Arithmetic and Piecewise Linear Circuits for Sigma-Delta Domain Multi-Level Signal Processing

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Abstract—This paper presents arithmetic and piecewise linear circuits operating directly on first-order multi-level sigma-delta modulated signals. The circuits can operate slower than sigma-delta domain binary circuits and can be more compact than Nyquist rate multi-bit circuits to obtain the same precision of processing. Thus, the proposed circuit technique will provide well-balanced signal processing systems both in operation speed and in circuit scale.

1. Introduction

Linear and nonlinear circuit modules operating directly on binary quantized sigma-delta (SD) modulated signals have been developed [1][2][3]. We call signal processors built of these modules the binary SD domain processors. They are smaller in circuit scale than multi-bit Nyquist rate signal processors because the modules themselves consist of small numbers of logic gates and decimators transforming outputs from SD based analog-to-digital (A/D) converters to multi-bit signals are not necessary. The bit-stream rate of SD modulated signals is OSR(: oversampling ratio) times higher than the data stream rate of Nyquist signals. Accordingly, the binary SD domain processors must operate OSR times faster than Nyquist rate processors. This makes it difficult for the binary SD domain processors to process wideband signals.

Now we consider to process multi-level SD modulated signals directly. Multi-level SD modulators operate at lower OSR than binary modulators because they generate less quantization noise [4]. Thus, processors for the signals will be lower(/higher) in operation speed, but larger(/smaller) in circuit scale than the binary processors(/Nyquist rate processors). Then, we expect that the multi-level SD domain processing technique will offer well-balanced circuits in speed and size. Moreover, the circuits will be practical since A/D and D/A converters based on multi-level SD modulation are commercially available [5].

In this paper we consider to build arithmetic and piecewise linear (PWL) circuits operating on multi-level SD modulated signals. We then discuss their operation speed and circuit scale.

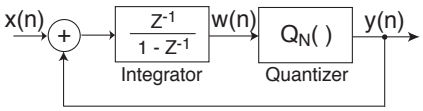

Figure 1: First-order sigma-delta modulator.

2. First-Order Multi-Level Sigma-Delta Modulation

Figure 1 shows a first-order discrete-time multi-level SD modulator. Suppose that its input range is $-1 \le x(n) \le 1$. It consists of an N(: even integer)-level quantizer $Q_N(\cdot)$, an integrator and an adder. The modulator is described by

$$\begin{aligned} y(n+1) &= Q_N(w(n+1)) \\ w(n+1) &= w(n) + x(n) - y(n) \end{aligned} \tag{1}$$

When quantization step is $\Delta Q_N = 2/(N-1)$, output $y(n)$ takes an element of a set S_N^o,

$$\begin{aligned} y(n) \in S_N^o = \{ & k_0/(N-1) \mid \\ & -(N-1) \le k_0 = 2k+1 \le N-1, k\text{: integer}\} \end{aligned} \tag{2}$$

We can decompose N-level SD modulated signals $y(n)$ into $N-1$ binary components as follows:

$$\begin{aligned} y(n) &= \tfrac{1}{N-1} \textstyle\sum_{Th \in S_N^e} sgn(y(n) - Th) \\ Th \in S_N^e = \{ & k_T/(N-1) \mid \\ & -(N-2) \le k_T = 2k \le N-2, k\text{: integer}\} \end{aligned} \tag{3}$$

The modulator responds to constant input $x(n) = x_c$ in the following way:

Property 1 *Suppose that $k_0 = k_T + 1$. When $k_T/(N-1) \le x_c \le k_0/(N-1)$, output $y(n)$ takes $(k_0-2)/(N-1)$ and $k_0/(N-1)$. However, it does not consecutively take $(k_0-2)/(N-1)$.*

Similarly when $(k_0-2)/(N-1) \le x_c \le k_T/(N-1)$, the output takes $(k_0-2)/(N-1)$ and $k_0/(N-1)$ but does not consecutively take $k_0/(N-1)$.

Reference [3] gives a proof of this property for $N=2$. Extending the proof, we can easily prove the property for any integer N.

Hereafter, we consider the N-level SD modulated signals as $(\log_2 N)$-bit SD modulated signals. Then, arithmetic and PWL circuits to be shown in the following sections can be built of digital logic gates.

3. SD Domain Arithmetic Circuits

3.1. Adders

We consider an SD domain adder whose output $z(n)$ is equal to a half of the sum of two inputs $x(n)$, $y(n) \in S_N^o$ in local average around time n, that is,

$$\overline{z(n)} = \frac{1}{2}\overline{(x(n) + y(n))} \tag{4}$$

The addition should be equivalent to N-level SD modulation of $(x(n) + y(n))/2$. Then,

$$z(n+1) = Q_N(e(n) + (x(n) + y(n))/2) \tag{5}$$

where we assumed that the adder possesses an N-level quantizer $Q_N(\cdot)$ which makes quantization error $e(n)$. Assume further that $e(n)$ is given by

$$e(n) \in \{-\Delta Q_N/4, \Delta Q_N/4\} \tag{6}$$

Then, the adder can be realized as a sequential logic circuit operating according to Tab. 1. In this table, $\delta(n)$ denotes difference between the sum of the two inputs and its quantized value,

$$\begin{array}{l} \delta(n) = Q_N((x(n) + y(n))/2) \\ -(x(n) + y(n))/2 \in \{-\Delta Q_N/2,\ 0,\ \Delta Q_N/2\} \end{array} \tag{7}$$

Next we consider a three-input SD domain adder whose output $z(n)$ is given by

$$\overline{z(n)} = \frac{1}{3}\overline{(u(n) + x(n) + y(n))}, \quad u(n), x(n), y(n) \in S_N^o \tag{8}$$

The addition should be equivalent to N-level SD modulation of $(u(n) + x(n) + y(n))/3$. Then,

$$z(n+1) = Q_N(e(n) + (u(n) + x(n) + y(n))/3) \tag{9}$$

Let the quantization error $e(n)$ be given by

$$e(n) \in \{-\Delta Q_N/3 + \epsilon, \epsilon, \Delta Q_N/3 + \epsilon\}, 0 < \epsilon < \Delta Q_N/6 \tag{10}$$

Then, the three-input adder can be realized as a sequential circuit operating according to Tab. 2. In this table $\delta(n)$ denotes difference between the sum of the three inputs and its quantized value,

$$\begin{array}{l} \delta(n) = Q_N((u(n) + x(n) + y(n))/3) \\ -(u(n) + x(n) + y(n))/3 \in \{-\Delta Q_N/3,\ 0,\ \Delta Q_N/3\} \end{array} \tag{11}$$

Figure 2 shows a schematic diagram of SD domain adder circuits. We need 80 and 130 logic gates to build the two and three-input (N=)four-level adders.

Table 1: State transition of the two-input adder.

$\lvert\delta(n)\rvert$	z(n+1)	e(n+1)
ΔQ/2	sum + 2e(n)	− e(n)
0	sum	e(n)

sum = (x(n) + y(n))/2

Table 2: State transition of the three-input adder.

δ(n) \ e(n)	−ΔQ/3 + ε	ε	ΔQ/3 + ε
ΔQ/3	z(n+1) = sum − ΔQ/3 e(n+1) = ε	z(n+1) = sum − ΔQ/3 e(n+1) = ΔQ/3 + ε	z(n+1) = sum + 2ΔQ/3 e(n+1) = −ΔQ/3 + ε
0	z(n+1) = sum e(n+1) = e(n)		
−ΔQ/3	z(n+1) = sum − 2ΔQ/3 e(n+1) = ΔQ/3 + ε	z(n+1) = sum + ΔQ/3 e(n+1) = −ΔQ/3 + ε	z(n+1) = sum + ΔQ/3 e(n+1) = ε

sum = (u(n) + x(n) + y(n))/3 0 < ε < ΔQ/6

Figure 3 shows waveforms obtained by averaging 20 consecutive input and output samples of the two and three-input 4-level adders. The outputs contain quantization noise. The power of the noise components in signal band [DC, $f_s/(2\ \mathrm{OSR})$], f_s(=1): sampling frequency, is shown in Fig. 4. The noise power of two-input SD domain binary adder is also shown in the figure for comparison.

3.2. Multipliers

In the SD domain, a product of two signals $x(n)$, $y(n) \in S_N^o$ is not obtained precisely by multiplying $x(n)$ to $y(n)$ simply. For example, let $x(n)$, $y(n)$ be given by

$$x(n) = y(n) = \begin{cases} \frac{1}{N-1}, & n\text{: even} \\ -\frac{1}{N-1}, & n\text{: odd} \end{cases}$$

Then, $\overline{x(n)}$=$\overline{y(n)}$=0. However, simple product $z(n)$ = $x(n)y(n)$ is not zero. Thus, we have to consider a multiplier whose output satisfies

$$\overline{z(n)} = \overline{x(n)} \times \overline{y(n)} \tag{12}$$

We expand above equation to

$$\overline{z(n)} = \tag{13}$$

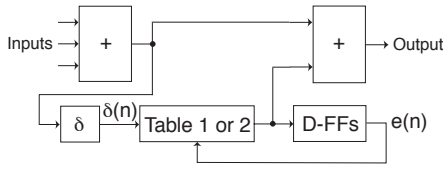

Figure 2: Schematic diagram of SD domain adders.

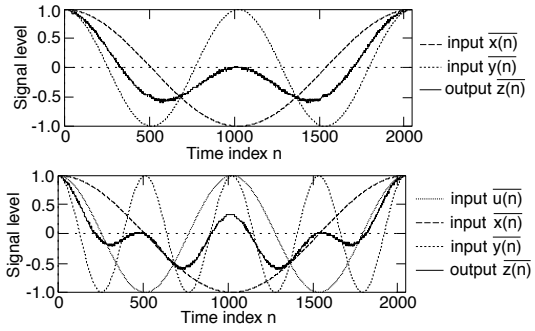

Figure 3: Averaged input and output waveforms of the adders.

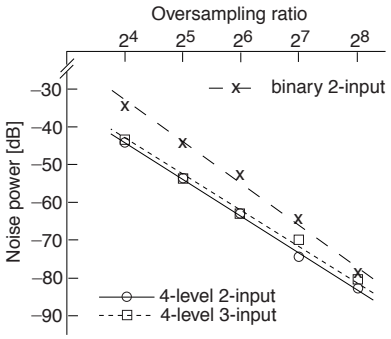

Figure 4: Output noise power of the adders.

$$= (\frac{1}{M_1}\sum_{m_1=n-M_1+1}^{n} x(m_1))(\frac{1}{M_2}\sum_{m_2=n-M_2+1}^{n} y(m_2))$$

$$= \frac{1}{M_1M_2}\sum_{m_1=n-M_1+1}^{n}\sum_{m_2=n-M_2+1}^{n} x(m_1)y(m_2)$$

We decompose one signal $y(n)$ as we have shown in Eq.(3),

$$y(m_2) = \frac{1}{N-1}\sum_{Th\in S_N^e} sgn(y(m_2) - Th) \qquad (14)$$

Then, we obtain partial product $x(m_1)\times y(m_2)$ by a circuit which consists of comparators, a 2's complement circuit, multiplexers and an $(N-1)$-input SD domain adder as shown in Fig. 5. We also use SD domain adders for the summation (13) of the partial products. When M_1=M_2=3, a (N=)four-level SD domain multiplier is built of about 2000 logic gates.

Figure 6 shows locally averaged inputs and outputs of 4-level SD domain multiplier when M_1=M_2=8. Figure 7 shows output noise power of the multiplier and a binary SD domain multiplier when M_1=M_2=3 and 8. The figure shows that SD domain multipliers do not always reduce output noise even if their scale $M_1\times M_2$ is larger.

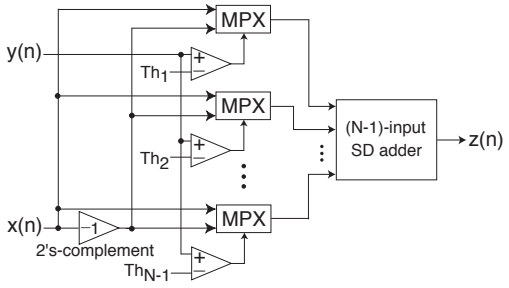

Figure 5: Schematic diagram of the circuit computing partial products.

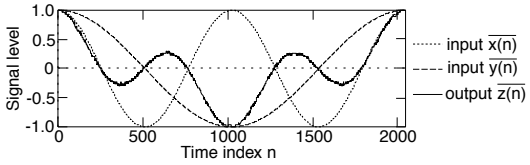

Figure 6: Averaged input and output waveforms of the multiplier.

4. SD Domain Piecewise Linear Circuits

Let k_T=0 in Property 1 in Sect. 2. Then, the property says that first-order SD modulated signals $\{\cdots, y(n), y(n+1), \cdots\}$ does not contain consecutive negative(positive) values if $x_c \geq 0 (<0)$. The signal $y(n)$ would hold the property even if local average of input $\overline{x(n)}$ varies slowly. Exploiting this property we build an absolute circuit as Fig. 8 shows. A part consisting of two AND gates, a D-latch, and an SR-FF judges polarity of the local average of input $x(n)\in S_N^o$. If two consecutive values of $x(n)$ are negative, the output of SR-FF becomes low and the 2's complement circuit reverses the polarity of $x(n)$. Then, we obtain $\overline{y(n)}=|\overline{x(n)}|$. We need 42 logic gates to build a (N=)four-level SD domain absolute circuit.

Minimum and maximum functions are expressed by

$$Max(\overline{x(n)}, \overline{y(n)}) = \overline{c(n)} + |\overline{d(n)}| \qquad (15)$$

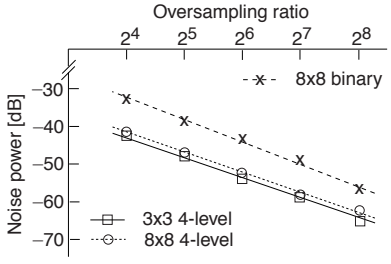

Figure 7: Output noise power of the multiplier.

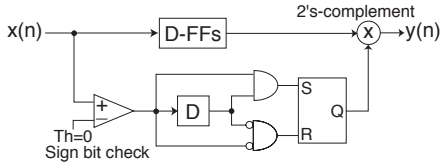

Figure 8: Schematic diagram of the absolute circuit.

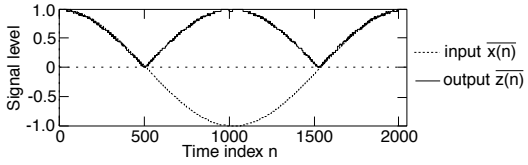

Figure 9: Averaged input and output waveforms of the absolute circuit.

$$
\begin{aligned}
Min(\overline{x(n)}, \overline{y(n)}) &= \overline{c(n)} - |\overline{d(n)}| \qquad (16)\\
c(n) &= (x(n) + y(n))/2\\
d(n) &= (x(n) - y(n))/2\\
x(n), y(n) &\in S_N^o
\end{aligned}
$$

Using above absolute circuit we can build Min/Max circuit as shown in Fig. 10. We need 386 logic gates to build a (N=)four-level Min/Max circuit.

Figures 9 and 11 show averaged inputs and outputs of the absolute and Min/Max circuits operating on 4-level SD modulated signals.

5. Discussion and Concluding Remarks

As we have shown in Figs. 4 and 7, the power of quantization noise contained in outputs from the multi-level SD domain arithmetic circuits is smaller than that of binary SD domain circuits. Although we have not shown in this paper, we found that the power of quantization noise in the outputs from the multi-level PWL circuits tends to decrease in signal band as OSR is set higher. We also found that their output noise power is about 7dB lower than that of binary SD domain PWL circuits. Thus, the low speed multi-level circuits process signals with the same precision as high speed binary circuits process.

The presented SD domain circuits process signals

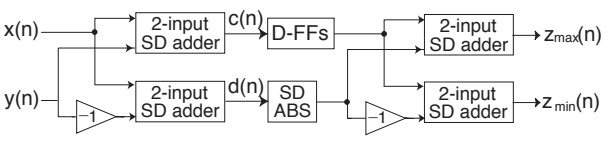

Figure 10: Schematic diagram of the Min/Max circuit.

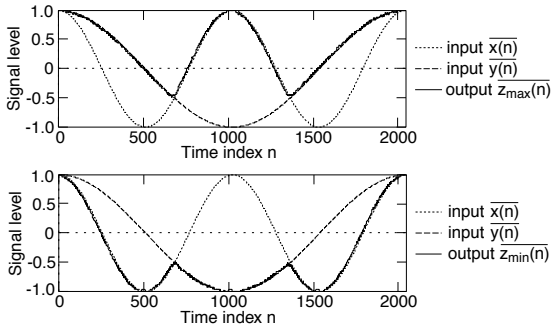

Figure 11: Averaged input and output waveforms of the Min/Max circuit.

from SD modulators directly without decimators between them. Moreover, the SD domain adder, absolute and Min/Max circuits can be built of small number of logic gates as we mentioned in Sects. 3 and 4. Therefore, it is obvious that these small scale circuits can process signals with the same precision as larger scale Nyquist rate circuits process when the small scale circuits are driven by high speed clocks. Lastly, we consider the multiplier. As we mentioned, in order to build a 3×3 four-level SD domain multiplier we need about 2000 logic gates, which is almost as same as the number of gates required for a 12-bit parallel multiplier. Nyquist rate signals with 12-bit length have quantization noise of -72dB. Output noise level of the SD domain multiplier can be reduced to the same level when it operates at OSR=2^{10}.

From above investigations we conclude that the proposed hardware technique for multi-level SD domain processing offers well-balanced circuits in both circuit scale and operation speed.

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