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Adaptive-Learning Functions of Ferroelectric Field-Effect Transistors for Synaptic Device Applications

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Abstract– Synaptic devices and neuron circuits employing ferroelectric thin films are technically reviewed. Ferroelectric field-effect transistor and thin-film transistor can provide interesting synaptic behaviors including an adaptive-learning function by exploiting partial switching events for the ferroelectric polarization.

1. Introduction

Artificial neuromorphic systems executing a distributed parallel information processing and an adaptive learning functions have recently been energetically developed for the 4th-industrial-revolution-driven information-oriented society. In these systems, neurons accept many weighted input signals and generate output pulses when total values of input signals exceeds a threshold value. The weighting to input signal is operated by synapses attached to neurons. Therefore, the synapse and neuron can be implemented by suitably designing the nonvolatile memory device and processor in artificial neural networks. Conventional hardware-based neuron chips needed too many transistors and external memories to exploit the synaptic functions. However, considering that lower-power consumption and smaller device size are absolutely required for realizing electrically-modifiable synapse array, the synapse device should be prepared with one electronic device. Various physical mechanisms such as resistive-change, phase-change, electrolytic ion movement, and ferroelectric partial switching, have been employed for mimicking the biological synapses.

Among them, a metal-ferroelectric-semiconductor field-effect transistor (MFSFET) [1] and ferroelectric thin-film transistor (Ferro-TFT) [2] implemented on Si and various substrates can be promising candidates by utilizing their nonvolatile analog-like memory operations. In establishing novel synaptic connections using an array of MFSFETs, two specified features of 'adaptive-learning' and 'electrically-modifiable function' in synaptic values, can be preferentially exploited. The adaptive-learning means that the electrical characteristics of the devices are partially or totally changed by applying given numbers of usual input signals to the devices. Furthermore, the different values of synaptic weights can be programmed and modified by designed pulse signal trains. In this presentation, we overview the historical developments and demonstrate the synaptic functions of the proposed ferroelectric neuron circuit using the MFSFET as a synapse device. Recent advancements and remaining technical issues of ferroelectric synapse devices are also discussed.

2. Operation Principles of Adaptive-Learning Neuron Circuits Using Ferroelectric FETs

2.1. Pulse frequency modulation-type ferroelectric synaptic device operations

Basic ferroelectric neuron circuit can be implemented to be pulse frequency modulation (PFM)-type, in which the adaptive-learning function can be obtained by controlling the amounts of ferroelectric polarization in the gate insulator of MFSFET. The channel conductance of the MFSFET can be gradually modulated with partially switching the polarization states of ferroelectric gate insulator. As results, the synaptic values stored in MFSFETs can be gradually changed by applying an adequate number of input signals. Thus, the duration of input pulses should be shorter than the switching time for the polarization reversal of the employed ferroelectric thin films. In PFM neuron circuit, since the output pulse interval is determined to be proportional to the product of the capacitance of embedded capacitor and channel resistance of MFSFET, the output pulse frequency can be gradually modulated during the application of input pulses. This function well emulates the information processing in human brain [3].

2.2. Multiple-input neuron circuit and electrically-modifiable synapse array

In practical neural networks, each neuron has many synapses connected to the neurons in previous layer. If the outputs of m neurons are fully connected to n neurons in the next layer, $m \times n$ synapses are required in this neuron circuit. This synapse array can be implemented by parallel connection of the MFSFETs, in which, each MFSFET is differently programmed and accepts pulse signals from neighboring neurons. Therefore, the total drain currents

summed up for all the MFSFETs in array determines the output behaviors of the ferroelectric neuron circuit. A series of this operation corresponds to the 'weighted-sum operation' of synaptic values.

2.3. Low-power large-area electronics applications

Even though the neuromorphic applications have been mainly developed in Si-based major electronic industries, the highly-functional novel large-area electronics are also important application fields for ultra-low-power neuromorphic systems. Conventional Si-based electronic technology is not compatible with large-area electronic devices fabricated on glass or flexible substrates. The thermal budget of fabrication process is also limited to glass transition temperatures of the employed substrates. In these applications, organic ferroelectric copolymer and oxide semiconductor thin film can be good choices as gate insulator and active channel materials, respectively, for the synapse devices with TFT configuration. Generally, the switching kinetics of the organic ferroelectric thin film, such as poly(vinylidene fluoride-trifluoroethylene) [P(DVF-TrFE)], are sensitively dependent on the applied electric field and the microcrystalline structure of the film. Thus, in order to realize the adaptive-learning synaptic operations for the ferro-TFT, the ferroelectric gate insulator and gate-stack structure should be carefully designed.

3. Adaptive-Learning Functions of Ferroelectric Neuron Circuits Using SBT Thin Films

3.1. Device fabrication

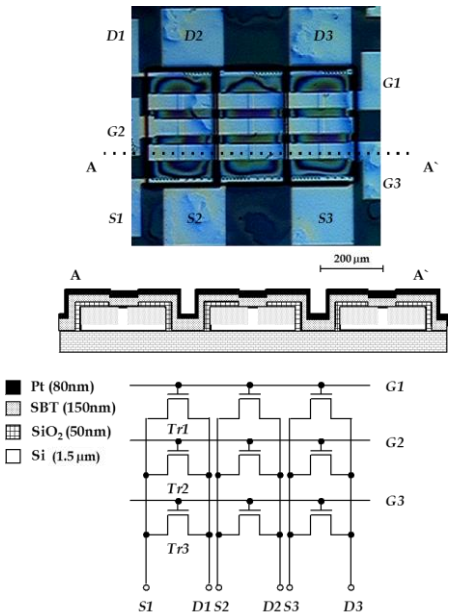

Figure 1. (a) Microscopic photo image, (b) schematic cross-section, and (c) equivalent circuit diagram of the MFSFET synapse array fabricated on SOI structure.

To demonstrate the adaptive-learning functions of ferroelectric synapse TFTs and neuron circuit, $SrBi_2Ta_2O_9$ (SBT) thin film was selected as ferroelectric gate insulator. First, the device regions were separated into islands of rectangular shapes using plasma etching system. The ion implantation processes were processed to form the active and source/drain regions of the devices. SBT films were deposited by liquid-source misted chemical deposition (LSMCD) method to secure the conformality of the deposited film. Crystallization temperature and thickness conditions were 750 ^oC and 150 nm, respectively. After the formation of Pt gate electrode, the SBT film was patterned by the selective etchant NH_4F:HCl solution. Finally, Al interconnection and electrode pads were formed by lift-off process.

3.2. Electrically-modifiable MFSFET synapse array

The prototype synaptic connection was designed to be 3×3 MFSFET array structure, which was implemented on silicon-on-insulator (SOI) substrate to individually give different synaptic weights to the devices connected along a common gate stripe. Figure 1 demonstrates a microscopic photo image, schematic cross-sectional view, and an equivalent circuit diagram of the fabricated MFSFET array. The Si islands are connected to the source terminals of FETs through the body contacts [4].

Figure 2(a) shows the drain current – gate voltage (I_{DS}-V_{GS}) characteristics of three transistors prepared on the same Si island. The MFSFETs with array structure was confirmed to be well fabricated on an SOI substrate without marked fluctuations in their electrical characteristics. The 'weighted-sum' operation could be carried out using the synapse FET array. The value of I_{DS} was almost doubled when two FETs are turned-on and was roughly three-times larger than that of one FET when three FETs are turned-on, as shown in Fig. 2(b). This results suggest that the data stored in MFSFET array can be summed-up with non-volatility. Furthermore, the different values of synaptic weight were stored by applying input pulses as program signals. The I_{DS} values in read-out operations were varied with an approximate ratio of 1:2:4 when the program pulse amplitude was adjusted to 2, 3, and 6 V for each synapse FET, as shown Fig. 3(a), which correspond to the configuration of varied initial synaptic weights. In order to sum up these values,

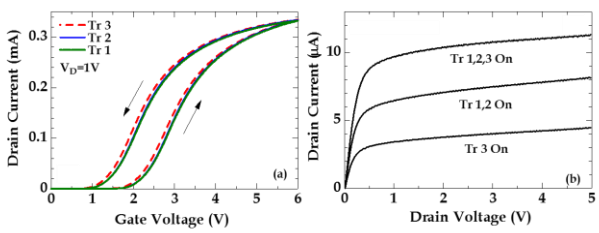

Figure 2. (a) I_{DS} – V_{GS} characteristics of three MFSFETs fabricated with array structure. (b) Sum operation of stored data in drain currents for the MFSFET array structure.

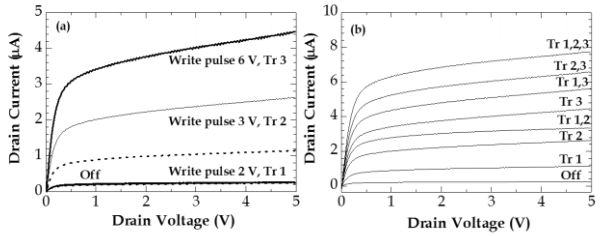

Figure 3. (a) Configuration of initial synaptic values into the MFSFETs in the array structure by applying different amplitude voltage pulses to Tr1, Tr2, and Tr3. (b) Demonstration of weighted-sum operation in MFSFET array structure.

total I_{DS}'s were evaluated for 3-bit input pulse signals, as shown in Fig. 3(b). A 3-bit analog-to-digital conversion was successfully examined as an example of the 'weighted-sum' operation. This is an interesting demonstration on the feasibility for high-density synaptic connections composed of electrically modifiable MFSFET synapse array.

3.3. Adaptive-learning ferroelectric neuron circuit

In a proposed adaptive-learning ferroelectric neuron circuit, CMOS Schmitt-trigger oscillator was proposed as a switching component, as shown in Fig. 4(a). The PFM-type oscillation operation can be available for the CMOS Schmitt-trigger, enclosed by dotted line, owing to its hysteretic behavior in input-output transfer characteristic. To minimize the process damages to the ferroelectric film, the CMOS processes were performed prior to the deposition of the SBT film. Full fabrication process was designed with 12 sheets of photo-masks. Figure 4(b) shows the microscopic image of the fabricated ferroelectric neuron circuit composed of synapse MFSFET and CMOS Schmitt-trigger oscillator [5].

Figure 5 shows typical output pulse waveforms for the ferroelectric neuron circuit after one and sixty pulses were

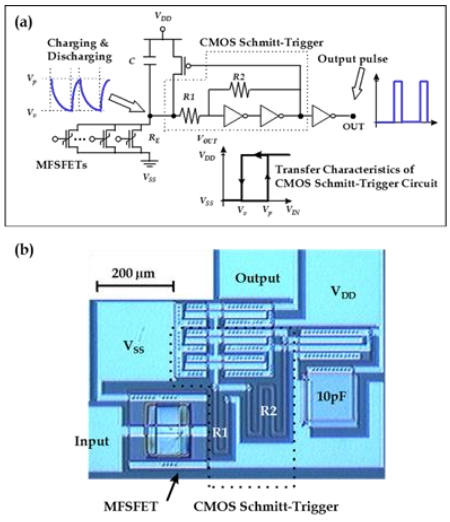

Figure 4. (a) Circuit diagram and (b) microscopic photo image of the ferroelectric neuron circuit composed of an MFSFET and a CMOS Schmitt-trigger oscillator.

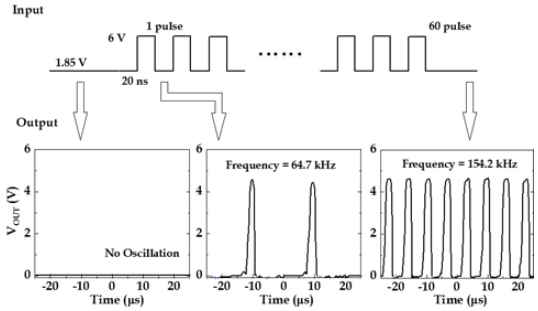

Figure 5. Output pulse waveforms of the integrated ferroelectric neuron circuit when one and sixty pulses with 6 V and 20 ns were applied as input signals.

applied to the input terminals. The circuit started to oscillate at an application of a single pulse and the oscillation frequency increased with increasing the number of applied pulses. This operation clearly demonstrates the adaptive-learning function of the proposed ferroelectric neuron circuit. It was suggested that the fabricated neuron circuit gradually changes its output characteristics (responses) by the past experience caused by the input pulses (stimulus). Furthermore, the output pulses generated from the CMOS Schmitt-trigger oscillator can be expected to be used as input signals for next-stage neurons.

4. Ferroelectric Synaptic TFTs Using P(VDF-TrFE) Thin Films for Large-Area Electronics

4.1. Device fabrication

To control the device characteristics of the proposed ferroelectric synapse TFTs, P(VDF-TrFE) were blended with various amounts of poly(methyl methacrylate) (PMMA) for solution coating process. Top-gate synapse TFTs with the gate-stack structure of Al/P(VDF-TrFE)-PMMA/Al_2O_3/In-Ga-Zn-O (IGZO) were fabricated. 20-nm-thick IGZO active channel was prepared by rf magnetron sputtering and a 9-nm-thick Al_2O_3 layer was successively deposited by ALD as a protection layer to protect the active region during the patterning process. An optical microscopic image and a schematic cross-sectional view of the fabricated synapse TFT are shown in Figs. 6(a) and 6(b), respectively [6].

4.2. Switching Behaviors of Organic Ferroelectric Co-Polymers

For the synapse TFT applications, the effects of the PMMA blended into the P(VDF-TrFE) on the ferroelectric switching characteristics were carefully examined. The ferroelectric switching time and the degree of partial switching of polarization are critical parameters to control the synaptic behaviors of the proposed devices. Based on the Kolmogorov-Avrami-Ishibashi (KAI) model, the switching kinetics for the P(VDF-TrFE)-PMMA blended films were systematically characterized. Important findings could be deduced from the obtained results (not

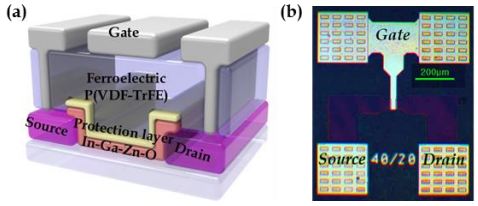

Figure 6. (a) Schematic cross-sectional diagram and (b) microscopic photo image of the fabricated synapse TFTs using PMMA-blended P(VDF-TrFE) GIs.

shown here) as follows; (1) longer switching time (t_s) and larger minimum electric field (E_a) required for minimizing t_s for the blended film with higher amounts of PMMA can be desirable for more gradual learning capability of the ferroelectric synapse TFTs. Thus, the control of volumetric amounts of ferroelectric phase in the blended film is a good solution to effectively control the switching kinetic parameters in the ferroelectric gate insulator of the synapse TFT and to minutely provide the synaptic weights to the device; (2) excessively blended amounts of PMMA was not so good to obtain sound ferroelectric natures. Thus, the amounts of PMMA blended into P(VDF-TrFE) should be carefully designed in consideration with the value of t_s and its electric field dependence.

4.3. Device Characterization of Ferroelectric Synapse TFTs

The gradual increase in I_{DS} for the fabricated synapse ferro-TFT was confirmed when the positive voltage pulses were repeatedly applied, which suggest that the synaptic weights could be controlled by the number of applied pulses. Figures 7(a) and 7(b) show the calculated modulation ratios of the synapse TFT using the P(VDF-TrFE) and P(VDF-TrFE)-PMMA gate insulators when the applied pulse amplitude was 20 V. To quantitatively evaluate the degree of synaptic weight variations for the ferroelectric synapse TFTs, the modulation ratio in synaptic weight was defined as the proportion of the I_{DS} obtained with given numbers of applied pulses to the I_{DS} obtained with 100-times pulses. The gradual variations in I_{DS} for each ferroelectric synapse TFT as the increase in number of pulses can be compared by the increasing trend of the modulation ratios. However, the marked dependence of the blended PMMA amounts on the synaptic weight variation was not reflected on the device characteristics. Consequently, the switching events observed in the synapse ferro-TFTs employing the IGZO active channel and organic ferroelectric copolymer insulator were found to be complicated to be accurately designed. This observation was supposed to originate from the formation of depletion capacitance within the IGZO channel layer.

5. Remaining Issues and Future Perspectives

We successfully demonstrated the adaptive-learning capability of the ferroelectric neuron circuit using

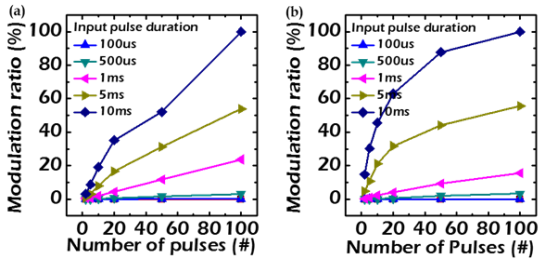

Figure 7. Variations in calculated modulation ratios in synaptic weights of the synapse TFTs using (a) P(VDF-TrFE) and (b) PMMA-blended P(VDF-TrFE) GIs.

MFSFET synapse devices. Furthermore, these synaptic operations could also be well verified for the ferro-TFT fabricated on glass substrate. It can be concluded from the obtained results that the proposed ferroelectric neuron circuit with an adaptive-learning function is very promising for next-generation large-scale neural networks in Si industries and for ultra-low power neuromorphic systems in large-area electronics. To enhance the device and system performance, several technical issues and appropriate solutions should be carefully examined as future works. In ferroelectric material viewpoints, it is necessary to improve the linearity for the ferroelectric polarization reversal and to accurately control the switching kinetics of ferroelectric gate insulators.

Acknowledgments

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