

## Brain-like Integrated System using Thin-Film Devices

Mutsumi Kimura<sup>†,‡</sup>, Tomoya Kameda<sup>†</sup>, and Yasuhiko Nakashima<sup>†</sup>

<sup>†</sup>Graduate School of Information Science, Nara Institute of Science and Technology  
Takayama, Ikoma 630-0192, Japan

<sup>‡</sup>Department of Electronics and Informatics, Ryukoku University  
Seta, Otsu 520-2194, Japan  
Email: mutsu@rins.ryukoku.ac.jp

**Abstract**– We are investigating "brain-type integrated system", namely, neural network built only by hardware, which can be compact, low power, robust, and integrated on everything. Until now, we have succeeded in hardware simplification and are trying to utilize thin-film devices for the neuromorphic application because they can be fabricated using low cost fabrication. In this study, we made a sandwiched structure of Ti/a-IGZO/Ti and found that the conductance decreases as the time goes by, which is available to modified Hebbian rule, a learning rule we proposed for our network. We modeled the conductance degradation of the a-IGZO thin film, developed a simulator, and obtained the learning results. We would like to develop brain-type integrated system with three-dimensional structure utilizing the thin-film devices in future.

### 1. Introduction

Artificial intelligences are biomimetic thinking machines that imitate biological neural networks in living brains. They are promising as key technologies in future societies with many advantages, such as self-organization, self-teaching, parallel distributed computing, fault tolerance, etc [1-4]. These advantages are obtained by connecting a large number of neurons with a much larger number of synapses to imitate human brains strictly, where more than  $10^{11}$  neurons and  $10^{15}$  synapses exist.

However, because the conventional artificial intelligences are complicated software executed on high-spec hardware, the machine size is very bulky and power consumption is unbelievably huge. Therefore, we are investigating "brain-type integrated system", namely, neural network built only by hardware, which can be compact, low power, robust, and integrated on everything in future [5-11]. In order to realize such system, simplification of the processing elements, such as neuron elements and synapse elements, three-dimensional structure, and low cost fabrication are required.

Until now, we have succeeded in that simplification and are trying to utilize thin-film devices for the neuromorphic application because they can be fabricated using low cost fabrication. In this study, we made a sandwiched structure of Ti/a-IGZO/Ti and found that the conductance decreases as the time goes by, which is available to modified Hebbian rule, a learning rule we proposed for our network. We modeled the conductance degradation of the a-IGZO

thin film, developed a simulator, and obtained the learning results [12,13]. We would like to develop brain-type integrated system with three-dimensional structure utilizing the thin-film devices in future.

### 2. Hardware Simplification [9]

#### 2.1. Neuron Element

We re-considered the operation of the neuron element and arrived at an idea that the necessary least functions are (1) generation of a binary state and (2) alternation of the binary state according to the input signal. We propose three-type neuron circuit: 2-inverter 2-switch, 2-inverter 1-switch, and 2-inverter circuits, as shown in Fig.1.

The 2-inverter 2-switch circuit is a circuit where the two inverters and two switches are circularly connected. The inverters generate a binary state, which is maintained when the switches are on, whereas it is alternated when the switches are off and some input signal is received. The two terminals are bi-directional, namely, work as both input and output terminals. One is for positive logic, whereas the other is for negative logic.

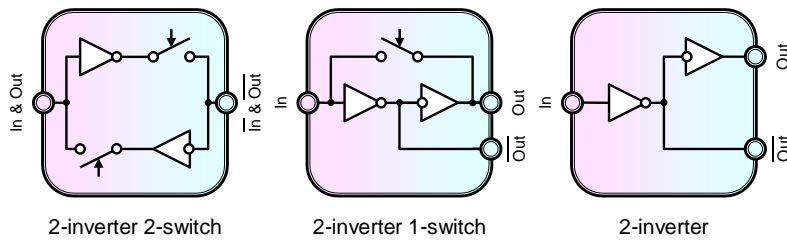
The 2-inverter 1-switch circuit is a circuit where the two inverters and one switch are circularly connected. In contrast to the 2-inverter 2-switch circuit, the three terminals are uni-directional, namely, work as either input or output terminal. One is an input terminal, another is an output terminal for positive logic, whereas the other is an output terminal for negative logic.

The 2-inverter circuit is a circuit where the two inverters are connected in series. The inverters generate a binary state, which is alternated whenever some input signal is received. The three terminals are uni-directional.

It should be noted that these neuron elements are extremely simple. Therefore, it is possible to compose them using thin-film devices including oxide semiconductors.

#### 2.2. Synapse Element

We re-considered the operation of the synapse element and arrived at an idea that the necessary least functions are (1) send of the signal from a neuron element to the neighboring one, (2) merge of the signals from the multiple neuron elements, and (3) controlling the synaptic connection strength. We propose a synapse element, variable register, as shown in Fig. 2.



	Number			Synapse per connected neuron	Switching noise
	Inverter	Switch	Transistor		
2-inverter 2-switch	2	2	8	2	Some
2-inverter 1-switch	2	1	6	4	Some
2-inverter	2	0	4	4	No

Fig 1. Simplification of the neuron element

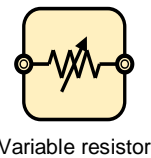


Fig 2. Simplification of the synapse element

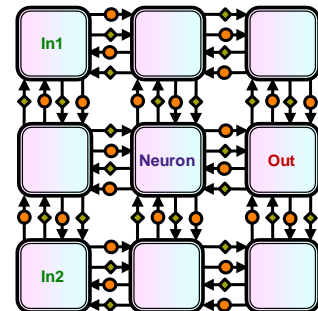
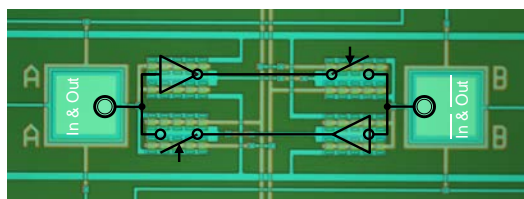
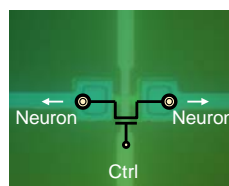


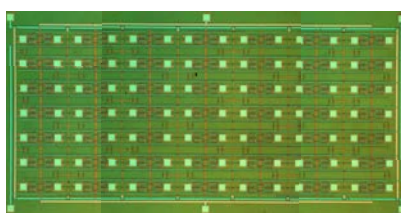
Fig 3. Architecture of the cellular network



(a) Neuron element

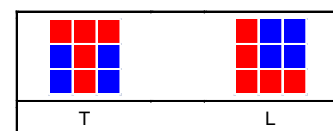


(b) Synapse element

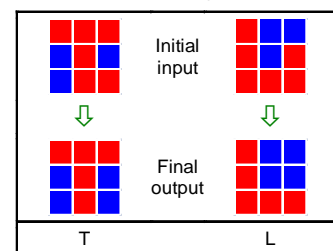


(c) Cellular Neural network

Fig 4. Actual hardware of the cellular neural network



Learning



Recalling

Fig 5. Confirmation of the letter recognition

The variable resistor sends the signal as an electric current, where the conductance corresponds to the synaptic connection strength. The electric currents are added by bundling them in parallel, which corresponds to merging the signals.

It should be noted again that this synapse element is extremely simple. Therefore, it is possible to compose them using thin-film devices including oxide semiconductors.

### 2.3. Network Architecture

The cellular neural networks are neural networks where a neuron is connected to only neighboring neurons. Figure 3 shows the neural networks, network structure. We propose two-type synapse connections, concordant connection and discordant connection. The concordant connection connects the same logics of the two neurons, namely, positive and positive logics or negative and negative logics, and tends to make the states of the two neurons the same. On the other hand, the discordant connection connects the different logics of the two

neurons, namely, positive and negative logics, and tends to make the states of the two neurons different. The reason why we prepare two-type synapse connections is to obtain the same effect that the synaptic connection strength becomes both stronger and weaker even if the actual strength becomes either one.

### 2.4. Behavior Confirmation

We compose the processing elements of thin-film transistors, which are promising for giant microelectronics applications, and form a cellular neural network by the processing elements, as shown in Fig. 4. Thin-film devices, including TFTs, are expected to be key technologies for giant microelectronics, because micro-size electron devices can be fabricated on large and inexpensive substrates. In this development, the thin-film devices are fabricated on a glass substrate, but they can also be fabricated on plastic films, which can be folded down to a compact size similar to a human brain. Therefore, we believe that thin-film devices are the most promising electron devices for cellular neural networks.

We verified that the cellular neural network can simultaneously recognize multiple simple alphabet letters. The experimental results of the letter recognition is shown in Fig. 5. Only the states in the 3×3 I/O neurons are shown, although hidden neurons exist between them. First, letter patterns of "T" and "L" are repeatedly inputted to the I/O neurons for several minutes. Finally, letter patterns with slightly different parts from "T" and "L" are initially inputted to the I/O neurons and immediately released, and output patterns are automatically outputted from the I/O neurons. It is confirmed that the output patterns are exactly the same as the letter pattern of "T" and "L" inputted first. This means that the cellular neural network can simultaneously recognize multiple simple alphabet letters of "T" and "L". Once the output patterns are exactly the same as the letter pattern inputted first, it is easy to classify the letters by a logical operation, namely, direct comparison of the letter patterns.

### 3. Oxide Semiconductor

#### 3.1. Device Characteristic

Figure 6 shows the characteristic of the In-Ga-Zn-O thin film [14]. First, a Ti electrode is deposited using vacuum evaporation. Next, an IGZO thin film is deposited using RF magnetron sputtering. The thickness of the IGZO thin film is 70 nm. After that, a Ti electrode is again deposited using vacuum evaporation. As a result, we get a sandwiched structure of Ti / a-IGZO / Ti. The size of the Ti electrodes is 150x150 μm. Finally, a voltage is applied and the current is measured. The applied voltage is 3.3 V.

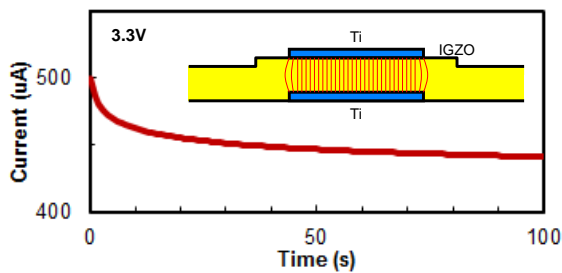
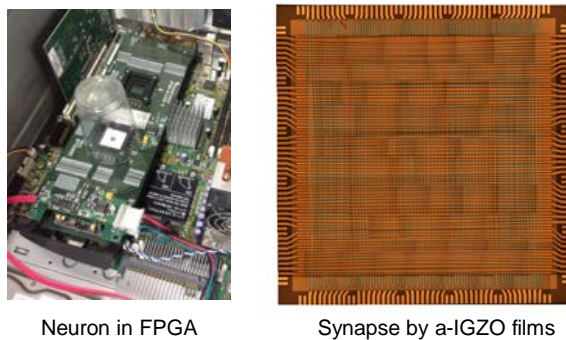


Fig 6. Device characteristic of the a-IGZO thin film.



Neuron in FPGA Synapse by a-IGZO films

Fig 7. Actual system of the neural network..

It is found that the conductance decreases as the time goes by. We believe that this is because of either the generation of trap states in the a-IGZO thin film or degradation of the metal interfaces. In any case, this characteristic is available to modified Hebbian rule, a learning rule we proposed for our network, which is explained in detail elsewhere [6].

#### 3.2. Behavior Confirmation

Figure 7 shows the actual system of the neural network. Here, we formed the neuron elements in an FPGA and the synapse elements by the a-IGZO thin film. Although the neuron elements can be potentially composed using thin-film devices, they are here formed in an FPGA just for primitive evaluation. We we tried to make this network learn number letters.

Figure 8 shows the learning principle of the neural network. Here, as for an example, number letter "0" is inputted as an input pattern. Firing states are assigned to

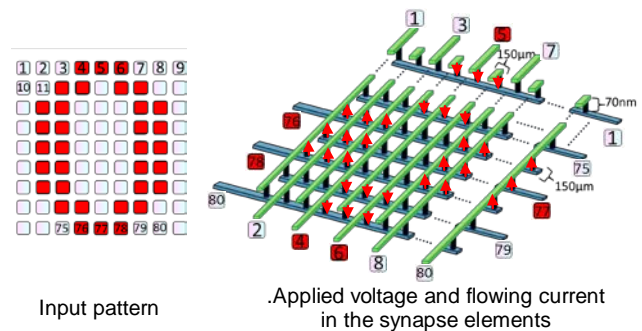


Fig 8. Learning principle of the neural network..

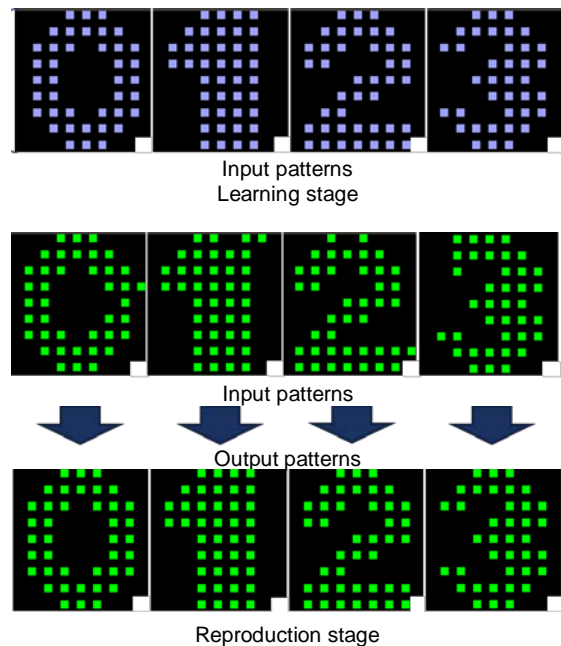


Fig 9. Learning results of number letters.

the neuron elements corresponding to the red squares, whereas stable states are assigned those to the white squares. High voltage of 3.3 V is applied to the vertical and horizontal lines corresponding to the neuron states in firing states, and ground voltage is applied to those in stable states. As a result, at the cross points where the high voltage is applied to one electrode and the ground voltage is applied to another electrode, the voltage difference occurs and the electric current flows, as shown by the red arrows in Fig. 8. The electric current causes the degradation in the conductance of the a-IGZO thin films, and the conductance decreases. By this degradation map, "0" is learned in the neural network. By repeating this procedure for other number letter, multiple number letters are overlapped and learned in the neural network.

It is regrettable that we have not yet succeeded in teaching multiple in the neural network. Instead, we modeled the conductance degradation of the a-IGZO thin film and developed a simulator [15]. Figure 9 shows the learning results of number letters obtained using the simulator. In the learning stage, number letters "0", "1", "2", and "3" are inputted as input patterns and the conductance degradation of a-IGZO thin films are induced, as explained above. In the reproduction stage, even if slightly distorted number letters are inputted as input patterns, the neural network outputs the correct number letters as output patterns. This behavior is a letter reproduction, which is a part of letter recognition.

### Acknowledgments

We would like to thank Prof. Mamoru Furuta of Kochi University of Technology, Prof. Toshio Kamiya of Tokyo Institute of Technology, KAKENHI 16K06733, Laboratory for Materials and Structures of Tokyo Institute of Technology, ROHM Semiconductor, Yazaki Memorial Foundation for Science and Technology, Support Center for Advanced Telecommunications Technology Research Foundation, and KOA Corporation.

### References

- [1] J. E. Dayhoff, *Neural Network Architectures, An Introduction*, Van Nostrand Reinhold, New York, 1990.
- [2] R. Hecht-Nielsen, *Neurocomputing*, Addison-Wesley Reading, MA, 1990.
- [3] S. Becker and G. E. Hinton, "Self-organizing neural network that discovers surfaces in random-dot stereograms," *Nature*, vol. 355, pp. 161-163, 1992.
- [4] J. V. Stone, N. M. Hunkin, and A. Hornby, "Neural-network models: Predicting spontaneous recovery of memory," *Nature*, vol. 414, pp. 167-168, 2001.
- [5] T. Kasakawa, H. Tabata, R. Onodera, H. Kojima, M. Kimura, H. Hara, and S. Inoue, "An artificial neural network at device level using simplified architecture and thin-film transistors," *IEEE Trans. Electron Devices*, vol. 57, pp. 2744-2750, 2010.
- [6] M. Kimura, T. Miyatani, Y. Fujita, and T. Kasakawa, "Apoptotic self-organized electronic device using thin-film transistors for artificial neural networks with unsupervised learning functions," *Jpn. J. Appl. Phys.*, vol. 54, 03CB02, 2015.
- [7] M. Kimura, Y. Fujita, T. Kasakawa, and T. Matsuda, "Novel architecture for cellular neural network suitable for high-density integration of electron devices - learning of multiple logics -," *ICONIP 2015*, pp. 12-20, 2015.
- [8] M. Kimura, R. Morita, Y. Koga, H. Nakanishi, N. Nakamura, and T. Matsuda, "Simplified architecture for cellular neural network suitable for high-density integration of electron devices," *NOLTA 2015*, pp. 499-502, 2015.
- [9] M. Kimura, N. Nakamura, T. Yokoyama, T. Matsuda, T. Kameda, and Y. Nakashima, "Simplification of processing elements in cellular neural networks - working confirmation using circuit simulation -," *ICONIP 2016*, pp. 309-317, 2016.
- [10] M. Kimura, R. Morita, S. Sugisaki, T. Matsuda, T. Kameda, and Y. Nakashima, "Letter reproduction using a cellular neural network consisting of simplified neurons and synapses fabricated by thin-film transistors," *NOLTA 2016*, pp. 36-39, 2016.
- [11] M. Kimura, R. Morita, S. Sugisaki, T. Matsuda, T. Kameda, and Y. Nakashima, "Cellular neural network formed by simplified processing elements composed of thin-film transistors," *Neurocomputing*, vol. 248, pp. 112-119, 2017.
- [12] T. Kameda, M. Kimura, and Y. Nakashima, "Neuromorphic hardware using simplified elements and thin-film semiconductor devices as synapse elements - simulation of Hopfield and cellular neural network -," *ICONIP 2017*, to be presented.
- [13] M. Kimura and T. Matsuda, "Neuromorphic application of oxide semiconductors," *2017 ULSIC vs. TFT Conference*, 2017.
- [14] M. Kimura, Y. Koga, T. Matsuda, and Y. Nakashima, "Characteristic analysis of IGZO thin films using planar and stacked devices - evaluation of electrical resistivity and current density," *IDW '16*, pp. 398-399, 2016.
- [15] T. Kameda, Master's Thesis, NAIST, NAIST-IS-MT1551036 (2017).