NOVEL ANTENNA FOR PACKAGED INTEGRATED RF FRONT ENDS

C.T.P. Song[(1)], P.S. Hall[(1)], H. Ghafouri-Shiraz[(2)], and D. Wake[(3)]
[(1)]School of Electrical and Electronic Engineering
University of Birmingham
Edgbaston, Birmingham B15 2TT, U. K.
Email: songp@eee-fs7.bham.ac.uk
[(2)]School of Electrical & Electronic Engineering (South Spine Block S1)
Nanyang Technological University , Nanyang Avenue, Singapore 639798
[(3)]B.T. Advanced Communications Technology Centre,
Adastral Park, Martlesham Heath, Ipswich, Suffolk, IP5 3RE, U. K.

1. Introduction

In recent years packaging for digital system technology has received widespread attention and has not only led to considerable miniaturisation of electronic components and subsystems but now also offers the prospect of complete systems on a single chip, as seen in recent conferences and symposiums. This technological approach gives increases in circuit performance and reliability. It is to be expected that by applying the same methodology to radio frequency integrated circuits (RFIC) a fully integrated transceiver module is now feasible with the same benefits of size and reliability. Such integrated modules would not only consist of various RF components such as low noise amplifiers (LNA), mixers, oscillators, phase shifters, and passive tuning components, but would also contain low power integrated circuits for signal processing. Increasing demand in the wireless communication market has generated the need for compact and fully integrated RF front end products, providing robustness, portability and ease of integration. An additional challenge in the development these transceiver chips is to fully integrate the antenna on the same piece of semiconductor material.

Antenna research is currently actively engaged in the development of such integrated packages and prompted the study of planar antennas on semiconductor substrates such as gallium arsenide (GaAs) and indium phosphide (InP) utilising standard processes [1]. However, when implemented at lower frequencies, this approach for antenna integration suffers from several problems. Fundamentally, these designs are limited by their size and hence operating frequency. Integrating an electrically small radiating element also results in small effective aperture, poor efficiency, high Q and therefore narrow bandwidth. Our work is aimed at these fundamental problems, especially in the restoration of the efficiency of the antenna, providing a solution to a truly compact, robust and efficient transceiver chip. In principle, baseband signals and DC bias are the only connection necessary to the chip. With the appropriate modification of the leadframe and chip packaging process, the chip carrier provides a large enough area for a suitable antenna to be installed. Although it is anticipated that on-chip digital signal processing will be included in such a system, pin counts requirement for this is expected to be minimal. This design also enables possible multi-chip module configuration, providing high-speed compact digital signal processing circuits within a single package. In the following two sections, we will first present three packaging concepts, followed by the gain restoration mechanism, using parasitic coupling.

2. Package design

There are two important requirements of the packaging system. Firstly, it must lead to ease in handling of a fragile semiconductor chip in the fabrication process and secondly, it must provide protection of the circuits from the environmental. There are currently several encapsulations and chip carrier standards being laid out by JEDEC JC-11 committee[3]. Fig. 1 shows the assembly concepts for an on carrier parasitic patch. In this design, a reduced sized antenna is integrated with the RF transceiver on a MMIC which is bonded onto the lead frame in layer 3. It was found that by using a parasitic patch antenna suspended over an air space, the performance of the MMIC antenna can be

greatly enhanced. This will be discussed in the next section. In this configuration, a digital signal processing (DSP) chip may be assembled beneath the ground plane of the antenna. This ground will provide isolation of the digital circuitry of the DSP chip to the RF circuitry. Other novelties in the antenna design are possible, such as adding on a specific superstrate to enhance performance[3-4]. In this case, the top cover sealing the entire package may function as a radome to further improve the gain of the chip carrier antenna. Finally, the parasite may also be use as the top cover, sealing the MMIC antenna within the package. Circular polarisation is also possible by appropriate parasite design. Another advantage of using parasitic coupling in close proximity to a small MMIC antenna is that connection from the circuit to the antenna is simplified, hence cutting cost in production. The exploitations of chip carrier antenna configurations are numerous. Further examples of other on chip carrier antenna configurations and assembly concepts will be presented at the conference.

3. Parasitic coupling of small antennas

A quarter wave H-shaped reduced size patch antenna has recently been reported and is to our knowledge one of the lowest operating frequency antennas so far made on Gallium Arsenide (GaAs)[1]. Such small integrated antennas have small radiating element and therefore small effective aperture. Hence they offer poor efficiency, high Q and therefore narrow bandwidth. Numerous references have discussed the improvements made by a parasitic coupled patch on the feed antennas' performance. However, most reported work involves half-wave feed patch[5-6] and only recently has the gain enhancement of an electrically small antenna been attempted[7]. In our application we aim to characterise this parasitic coupling performance with our reduced size, electrically small quarter wave feed antenna.

The size reduction reported in[1] is achieved by dielectric loading and by reducing the dimension of the center stem of the H. Further size reduction can also be achieve by reducing the number of shorting pins. This approach for further size reduction is demonstrated in the design of the feed antenna with only 2 shorting pins, shown in Fig. 2a. The feed antenna is built on FR4 substrates (ε_r=4.5, thickness=0.508mm) with an overall length(along z-axis) and width(along x-axis) of 7.5 x 9.8*mm* at a resonance frequency of 2.466GHz. It should be noted that antennas built on semiconductor material such as GaAs would have a substrate dielectric constant of 12.9. The measured bandwidth and gain are 1.4% and -16dBi respectively. Four different parasite arrangements are shown in Fig. 2b. They are, a half wave parasite (A_1); a tuned parasite (A_2); a tuned parasite with FR4 superstrate (A_2+B); and finally, a parasite with a U-Slot cut (B+C). The performance of S_{11} and gain at optimum coupling height of 2mm was measured for these parasitic configuration, shown in Fig. 3. From the measurements, it can be seen that a half wave parasite (A_1) is not an optimum coupling size, with gain enhancement of only 10dB. By tuning the parasite (A_2), an overall gain enhancement of 21dB, bringing the overall antenna gain to 5dBi was achieved. Bandwidth of the antenna system has also increased. However, by placing a FR4 superstrate on top of the tuned parasite (A_2+B), a much larger gain bandwidth results. This superstrate cover simulates the top cover encapsulation of the final chip carrier. To reduce the size of the parasite and further enhance bandwidth, a U-Slot is introduced on the parasite (B+C). This final parasite gives a bandwidth increase to 4.3% and a gain of 5dBi. The patterns are shown in Fig. 4 with polarisation isolation close to 20dB. The relation of the position and height of the parasite were also investigated. Fig 5 shows the gain at 2.466GHz and the 3dB gain bandwidth of the antenna, with varying position of the tuned parasite (A_2) along the Z-axis. The offset position at about Z=12.8*mm* was found to be the optimum for maximum gain and gain bandwidth. As expected, when parasitic plate height increases, coupling strength of the antenna system reduces, hence the overall antenna gain also reduces. The antenna concept has been demonstrated in a 5.8GHz ISM band data transfer unit which will be shown during the conference.

4. Conclusion

A novel method of integrating an antenna and transceiver chip within a single package is presented. In this approach, the antenna size is no longer restricted by the space on the semiconductor substrate but by its encapsulating carrier material. Existing fabrication process technologies can be utilised, being

largely compatible with the structures described. However it is anticipated that as RFIC semiconductor fabrication evolves customised leadframe and packaging design will be developed to give ultimate design flexibility. Single package transceiver integrated systems will soon emerge combining advances in VLSI and MMIC technology.

5. Acknowledgment
The authors would like to thank BT Advanced Communications Technology Centre for their funding for this study and Dr. Paul Webb for the discussion of semiconductor fabrication process.

6. References

1. Singh, D., Gardner, P., and Hall, P.S.,: "Miniaturised MMIC H antenna for microwave applications", *28th European Microwave Conference*, Amsterdam, Oct 1998.
2. Jackson, K.A. Cahn, R.W., Haasen, P., Kramer, E.J., Material Science and Technology: Processing of Semiconductors, *VCH Publishers Inc.*, 1996
3. Jackson, S.R., and Alexopoulos, N.G.,: "Gain enhancement methods for printed circuit antennas," *IEEE Trans. Antennas and Propagat*., vol. 33, no. 9, pp. 976-987, 1985.
4. Huang, C.Y., and Wu, J.Y.,: "Compact Microstrip Antenna Loaded with Very high Permittivity superstrate", *IEEE AP-S International Symposium*, Atlanta Georgia, ,pp. 680-683, 1998
5. Lee, R.Q., Lee, K.F., and Bobinchak, J.,: "Characteristics of a two-layer electromagnetically coupled rectangular patch antenna," *Elect. Lett.*, Vol. 23, No. 20, pp.1070-1072, Sep. 1987.
6. James, J.R., and Hall, P.S.,: Handbook of Microstrip Antennas, London, *Peter Peregrinus Ltd.*, 1989, Chapter 3 and 6
7. Sakai, S., and Arai, H.,: "Directivity gain enhancement of small antenna by parasitic patch", *IEEE AP-S International Symposium*, Atlanta Georgia, ,pp. 320-323, 1998

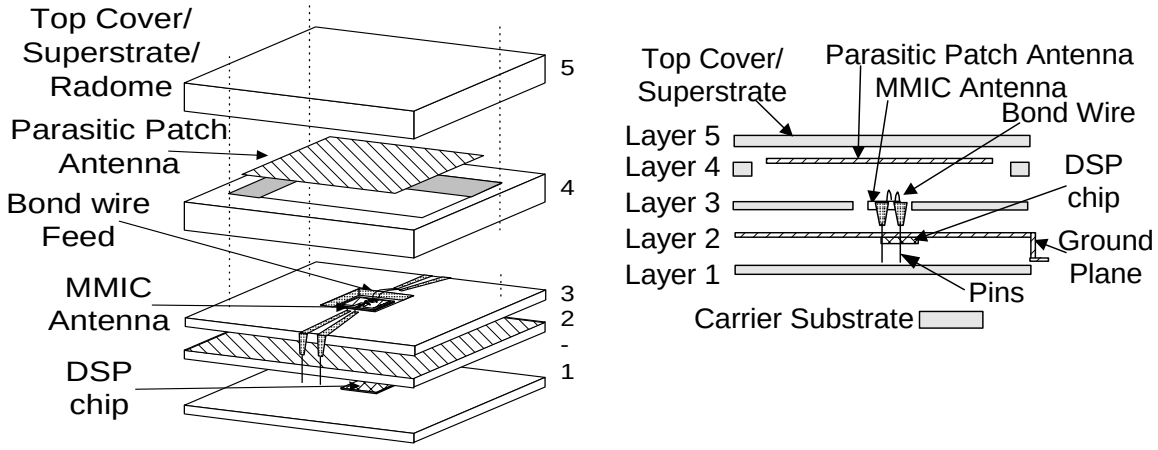
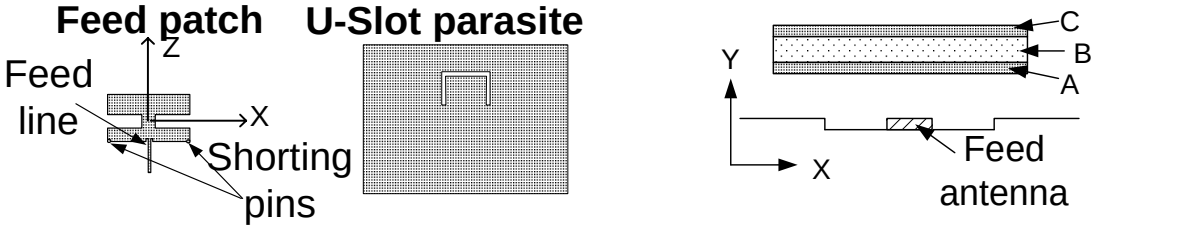


Figure 1: Assembly sequence



(a)Feed patch and parasite with U-slot (b) Electrically small feed antenna with parasites

Figure 2: Feed antenna and parasitic patch
A - First parasite: A_1 = 0.5λ at 60 x 60 *(mm)* or A_2 = Tuned at 48 x 53 *(mm)*

B - Dielectric layer (FR4, thickness 0.508mm) on first parasite
C - Parasite 43.5 x 53 *(mm)* with U-Slot printed

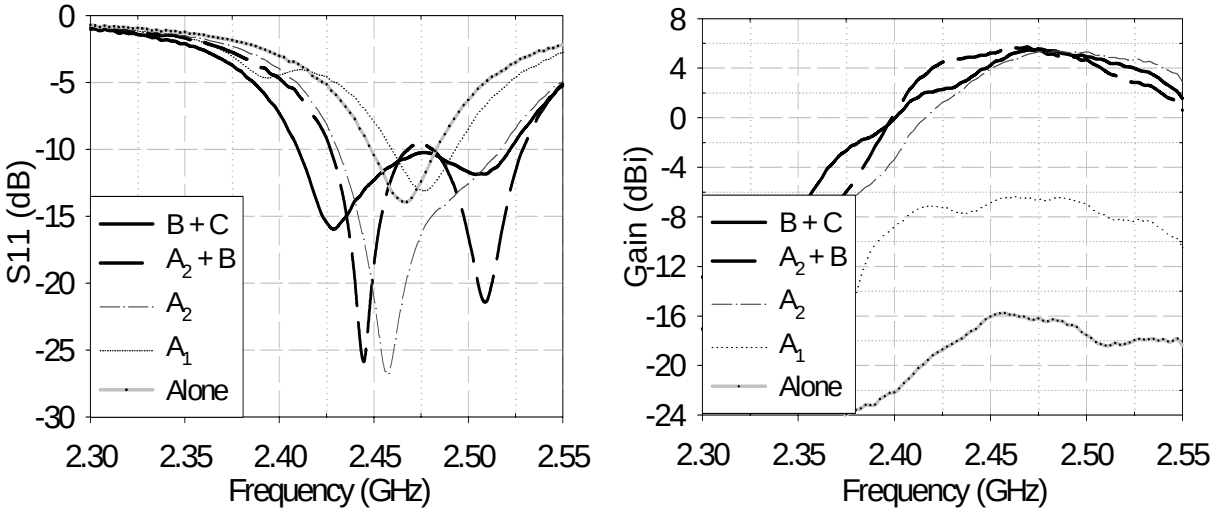


Figure 3: Performance with different parasite configuration

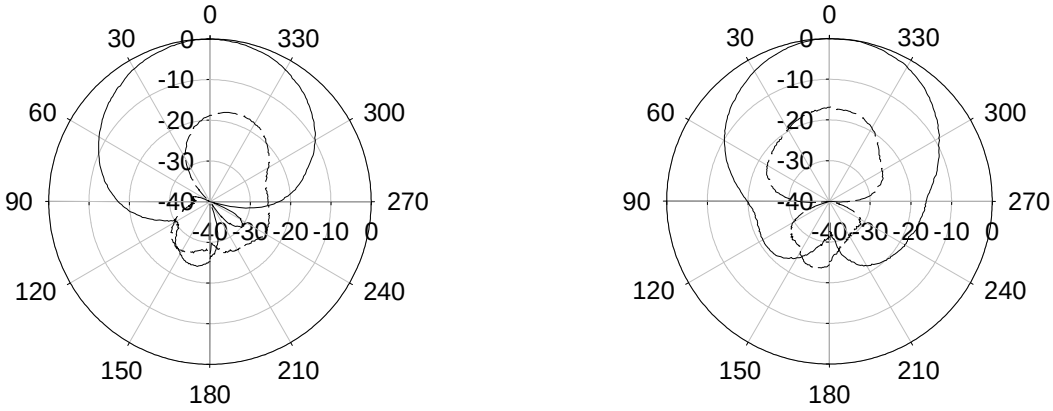


Figure 4: Measured patterns of U-Slot parasite at 2.49GHz (Configuration B+C)

(——— Co-pol. ; - - - - Cross-pol.)

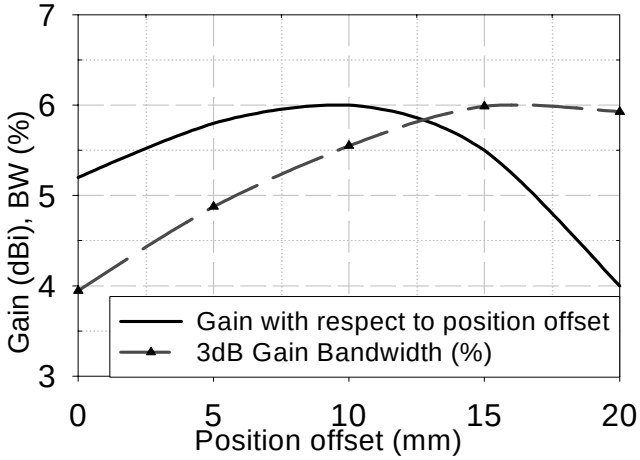


Figure 5: Position of parasite on bandwidth and gain(Configuration A_2)