

A SYSTOLIC ARRAY ARCHITECTURE FOR SCANNING SUPERRESOLUTION ARRAYS

Motoharu Ueno and Kazuaki Kawabata  
 Toshiba Research and Development Center  
 1, Komukai Toshiba-cho Saiwai-ku  
 Kawasaki 210, Japan

Introduction

Superresolution array techniques based on nonlinear spectral analysis have inherent *superresolution* capabilities in the field of signal source direction finding compared with conventional methods whose resolution capability is restricted by the Rayleigh criterion. This paper discusses two problems in a superresolution array. The first concerns hardware implementation. Recent sophisticated digital very large-scale integration (VLSI) technology has been leading to a new concept in array antennas, known as the digital beam forming (DBF) concept. While there are various configurations for the DBF processor, DBF processors having the systolic (array) architecture [1], which is regularly structured and provides resulting high-speed performances, are considered as the most suitable approach to implementing processors using VLSI technology. A new systolic architecture for the superresolution arrays will be proposed. The second problem is concerned with the scanning operation to measure the source directions in space. The superresolution array to be proposed exploits the Applebaum-Howells adaptive array. Scanning is performed by controlling the steering signal in the Applebaum-Howells adaptive array. Some limitations in the scanning performance will be discussed.

Systolic Architecture

Figure 1(a) shows a generic configuration for the superresolution array. The array consists of two blocks: an adaptive array and a (super-resolution) array output processor. The Applebaum-Howells array is used as the adaptive array; the array output is defined as [2]

$$A(u) = \frac{h(u)h^*(u)}{x^T(u)x^*(u)}, \quad (1)$$

where  $h(u)$  is the output of the adaptive array, in which  $u$  is the observation angle in the  $u$ -space, and  $x(u)$  represents the adaptive array weight vector; superscripts  $T$  and asterisk denote the vector transpose and the complex conjugate, respectively.

A systolic architecture for the superresolution array is depicted in Fig.1(b). This architecture can be derived in two steps: the procedure in the first step is to implement the Applebaum-Howells processor into a systolic configuration. The essential matter is to orthogonalize the input signals  $v(u)$  and the steering signal  $s(u)$  by using the Gram-Schmidt processor; in other words, the processing is performed in the eigen-space of the input signal. This procedure induces a systolic configuration for the Applebaum-Howells processor [3].

The array output processor is embedded into the systolic Applebaum-Howells processor at the second step. This procedure requires modifi-

$$xx_j(u) = \sum_{k=1}^j x_k(u)x_k^*(u).$$

Note that the weight norms in the original(real) and eigen space are the same. This partial sum is calculated in the boundary cells. In the bottom boundary cell, the array output is obtained by dividing the Applebaum-Howells array output by the weight norm. The internal configurations for the boundary cell and the bottom boundary cell are shown in Fig.1(d) and (e), respectively.

### Scanning Characteristics

Scanning is carried out using the steering signal  $s(u)$ [4]. An important design parameter is the scanning time  $T_{scan}$ . Figure 2 represents the scanning sequence and the design parameters; time is counted by a real number, or by an integer number in units of the sampling interval  $T_s$ . At time  $k$ , the steering signal is set at an observation angle  $u = u(k)$ . The input signals are sampled with sampling interval  $T_s$ . The steering signal is fixed at the observation angle and the input signal is sampled for  $N_{iter}$  times at each observation angle in order to converge the processors. The relation between the array *beamwidth* HPBW and the total scanning time  $T_{scan}$  necessary to observe over the space angle from zero to  $2\pi$  is, as shown in Fig.2, given by

$$T_{scan} \geq N_{iter} T_s \frac{2\pi}{HPBW}, \text{ or } \frac{T_{scan}}{T_s} \geq \frac{2\pi}{CHPBW} N_{iter} \frac{1}{\frac{HPBW}{CHPBW}}, \quad (2)$$

where CHPBW is the half-power beamwidth of a conventional array with the same aperture size. Equation(2) gives a certain limitation to the scanning time.

Figures 3(a) and (b) show the scanning characteristics of the array for a single narrow band source for those cases with variations in the scanning time  $T_{scan}(N_{iter})$  and the array beamwidth. The processor parameters, such as the loop gain and time constant, are set so as to satisfy stable operation conditions. As shown in these figures, the scanning effects on the array performances appear as degradations in the observation angle accuracy, resolution, and level. In particular, as seen from Fig.3(b), these degradations become unacceptable as the scanning time decreases.

### Conclusion

A systolic array architecture for a scanning superresolution array has been proposed. The proposed architecture has exploited a systolic architecture for the Applebaum-Howells array, and the superresolution array output processor was efficiently embedded into the systolic architecture. The scanning characteristic analysis has shown a certain relation between scanning time and resolution capability, i.e., increased resolution capability is obtained at the expense of scanning time.

### References

- [1] S.Y.Kung, VLSI Array Processor, Prentice-Hall, 1987
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- [3] M.Ueno et al., IEEE Trans. Antennas Propagat., vol.AP-38, no.8
- [4] —————, IEEE Trans. Antennas Propagat., vol.AP-32, no.3

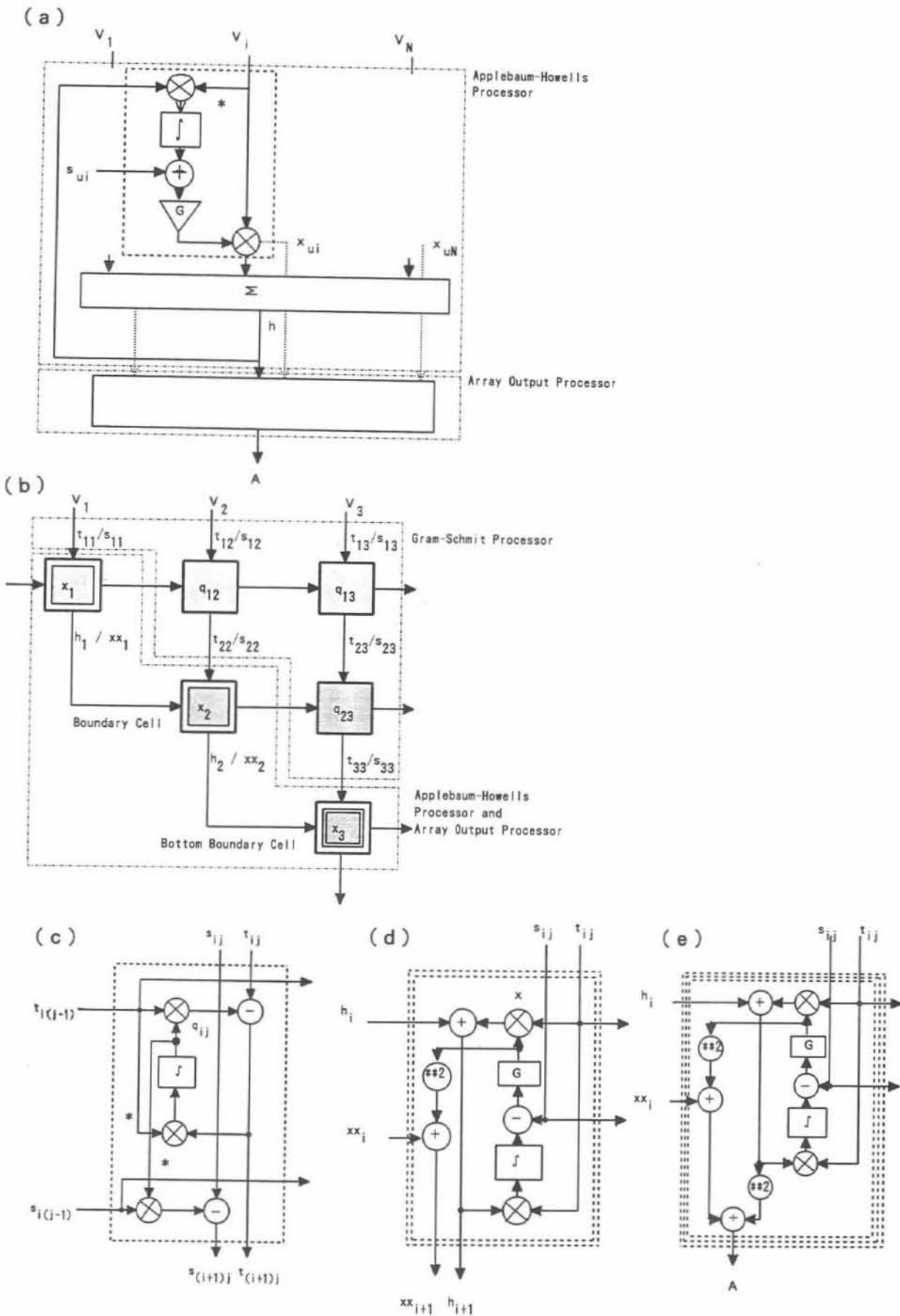


Fig.1 Generic and systolic superresolution configurations. (a)Generic configuration, (b)systolic configuration, (c)the Gram-Schmidt processor cell, (d) boundary cell, and (e) bottom boundary cell.

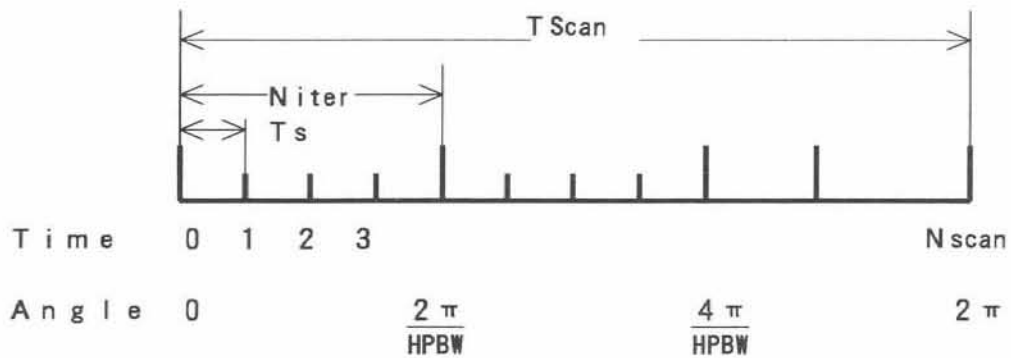


Fig.2 Scanning Sequence. Scanning is performed with observation angle interval  $2 / HPBW$ ; the input signal is sampled for  $N_{iter}$  times with sampling interval  $T_s$ , at each observation angle.

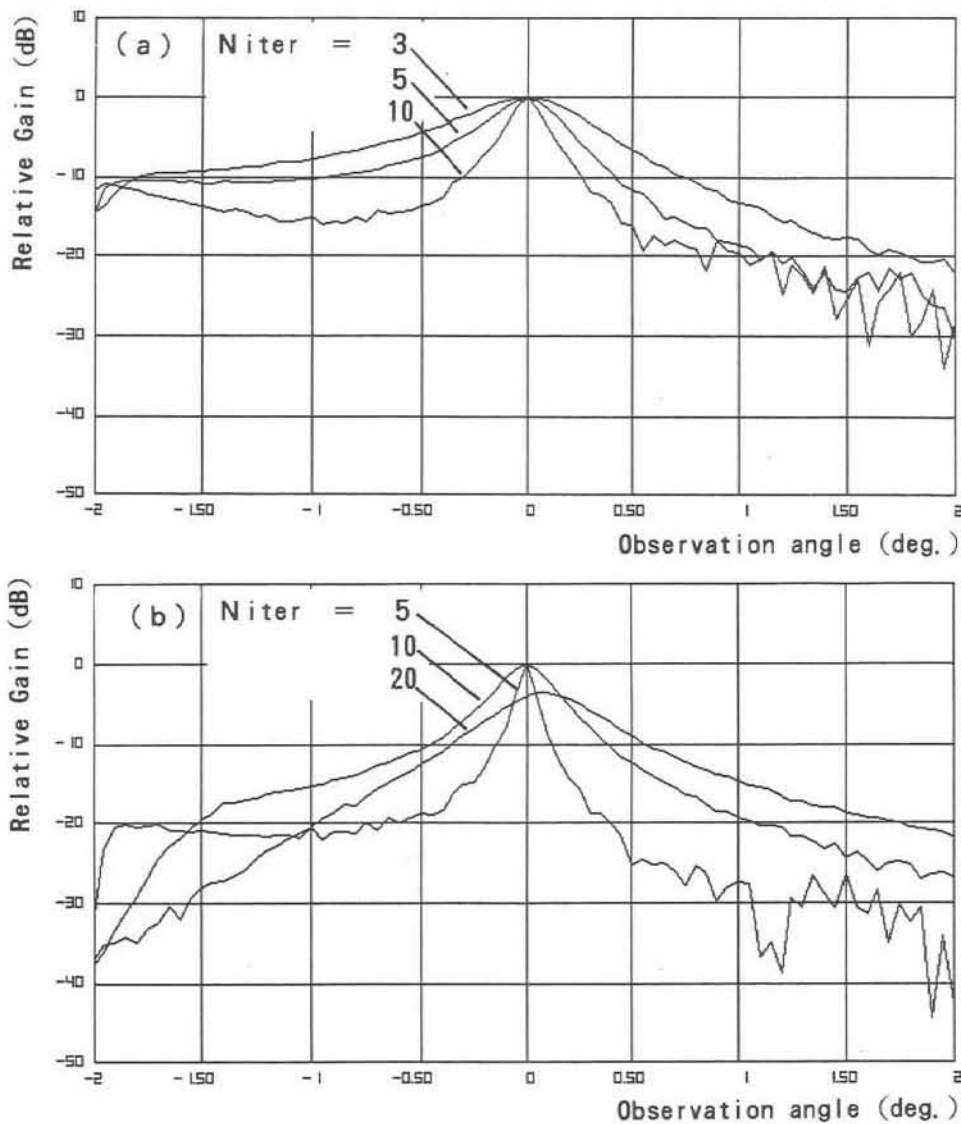


Fig.3 Scanning characteristics for those cases with variation in the scanning time  $T_{scan}$  ( $N_{iter}$ ) and the beamwidth  $HPBC$ . A single narrow band signal at levels of 40 dB relative to the thermal noise floor at the array elements, and a linear array with 17 array elements and half wavelength element spacing is assumed. (a)  $HPBC/CHPBC = 0.15$  and (b)  $HPBC/CHPBC = 0.075$ .