Design of a low power UWB CMOS LNA for UWB system

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1. Introduction

Ultra Wideband (UWB) system has become an increasingly popular technology which is a wireless technology capable of transmitting data over the wide spectrum of frequency band with very low power and high data rates [1]. For a wideband application such as UWB system, wideband input matching and sufficient gain over the entire bandwidth are important. UWB systems are under development to satisfy such demands by adopting various advanced technologies. CMOS technology is one of the key technologies not only to provide high performance but also to reduce manufacturing cost. Low noise amplifier (LNA) is one of the most critical devices in the UWB receivers since the noise figure is a dominant figure of merit in the first stage of the receiver. In addition, it should have characteristics of low power consumption, low return loss and high gain over the entire frequency band of interest. In this paper, we propose a low power current reuse CMOS LNA to increase the transconductance of the LNA without increasing the power dissipation, unlike other technologies [2-4]. To reduce the power consumption and to achieve wideband gain performance, an inverter stage with current reuse technique is stacked on the top of a common source amplifier.

2. UWB LNA design approach

To achieve the low power consumption and the sufficient voltage gain, a current reuse technique is usually adopted. By utilizing current reuse technique with inverter-type amplifier, a two-stage cascade topology shown in Figure 1 (a) can be converted to the inverter-type amplifier stage shown in Figure 1 (b). Thus, they share the same bias current.

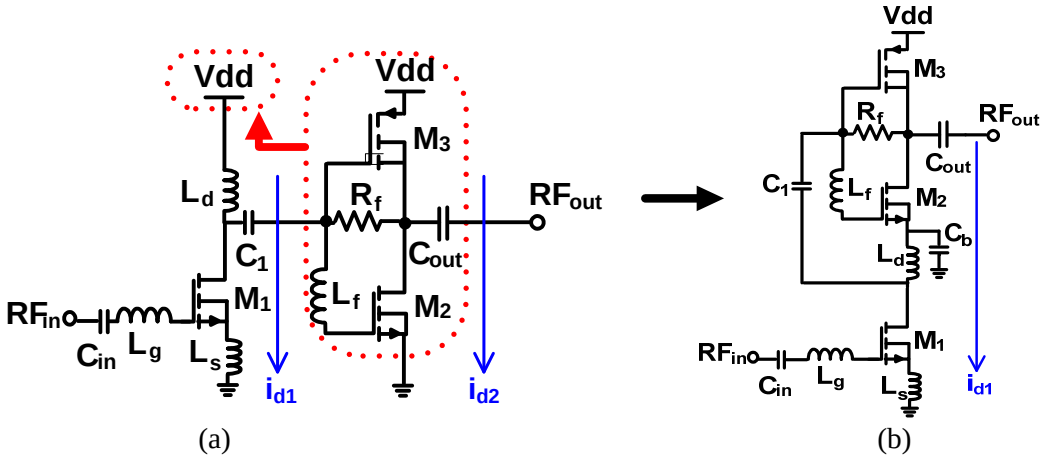


Figure 1: UWB LNA utilizing current reuse technique (a) A two- stage cascade stage (b) A full schematic of the proposed LNA

Figure 1.(b) shows a full schematic of the proposed UWB LNA. The structure is a single-stage LNA with inductive degeneration at the source. In this topology, a current reuse technique is

adopted to achieve a high transconductance with less current. M_1 operates as a common-source stage and M_2 and M_3 operate as inverter stage with splitting-load inductive peaking technique [5]. The signal amplified by M_1 is coupled to the gate of M_2 by C_1 while the source of M_2 is bypassed by C_b. Thus, the proposed topology can lower the power consumption through the reuse of the bias current and a single stage has sufficient voltage gain with minimized low power consumption. The use of source degeneration inductor has the advantage of simultaneously achieving both input and noise matching. The input impedance of M_1 is given by

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}} + R_g \qquad (1)$$

Inductors L_s and L_g form an impedance matching network with the gate capacitance C_{gs} of M_1. The matching conditions to R_s give

$$L_s = \frac{(R_s - R_g)C_{gs1}}{g_{m1}}, \qquad (2)$$

$$L_g = \frac{1}{\omega_0^2 C_{gs1}}, \qquad (3)$$

where ω_0 is the operating frequency.

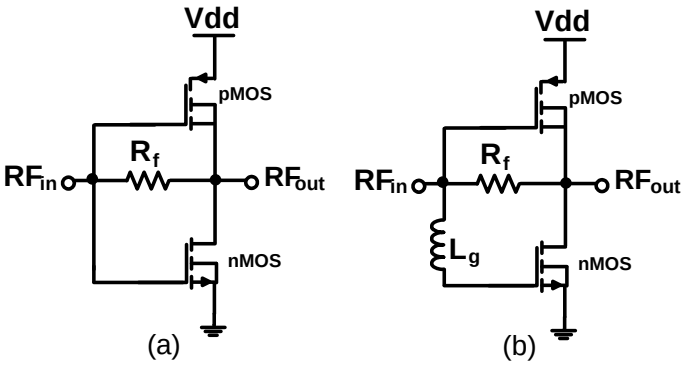


Figure 2: The resistive feedback inverter (a) Conventional one (b) Inverter with inductive peaking technique

Figure 2 shows a conventional resistive feedback inverter and inverter with splitting-load inductive peaking. As shown in Figure 2 (a), the bandwidth of a conventional feedback inverter is dominated by the time constant at the input and output node [6]. Thus, the operating bandwidth will be limited by the parasitic capacitance of the transistors. Figure 2 (b) shows the proposed inverter with a peaking inductor at the gate of NMOS device. By applying a peaking inductor asymmetrically at the gate of NMOS in the inverter, the capacitive loads from the NMOS and PMOS can be split. Thus, the 3-dB bandwidth can be further extended to a higher frequency. To achieve a flat gain of 14 dB at UWB low band (3.1 - 4.8 GHz), inverter stage with splitting-load inductive peaking technique is utilized. Figure 3 shows the simulated performances of inverter with and without splitting-load inductive peaking. Compared with the conventional resistive feedback inverter without inductive peaking, the proposed topology can effectively extend 3-dB bandwidth to a higher frequency without additional power consumption.

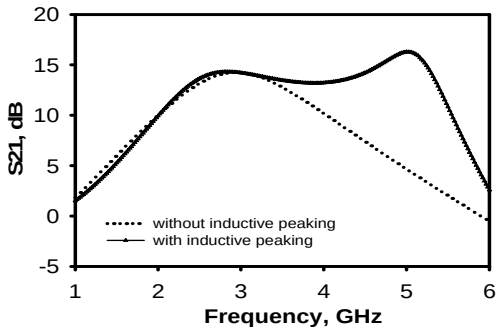


Figure 3: Comparison of the gain with and without inductive peaking

3. Simulated Results

The designed UWB LNA was simulated using Cadence SpectreRF [7] with TSMC 0.18μm RF CMOS process. As shown in Figure 4, the proposed LNA occupies a 1.0 mm x 0.93 mm die area including measurement pads.

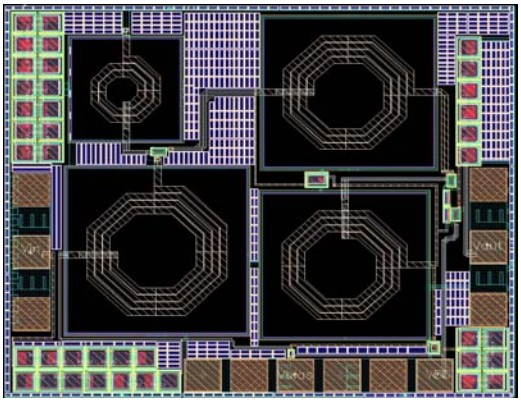
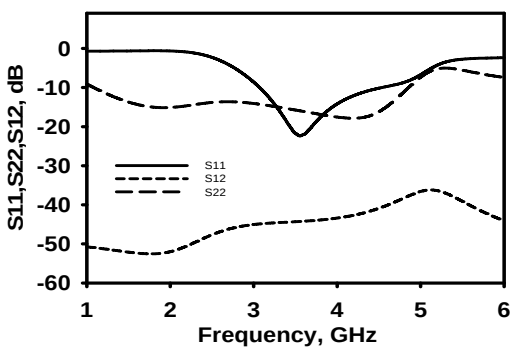


Figure 4: Layout of the LNA.

Figure 5 and Figure 6 show the simulated S-parameters and noise figure of the designed UWB LNA. The input and output matching characteristics (S_{11} and S_{22}) illustrated in Figure 4 reveal that the designed LNA has sufficient 9 dB and 10 dB I/O return losses at UWB low band, respectively. In addition, the excellent reverse isolation (S_{12}) of greater than 38 dB is obtained. As shown in Figure 6, the LNA has the maximum gain 16.3 dB with -3 dB band from 2.4 to 5.3 GHz and the noise figure of 2.9 – 3.8 dB at desired frequency. The input-referred 1-dB compression point (P1dB) is -17 dBm and input-referred third-order intermodulation point (IIP3) is -8 dBm. The proposed LNA drains 4.2 mA from a 1.6 V supply voltage.



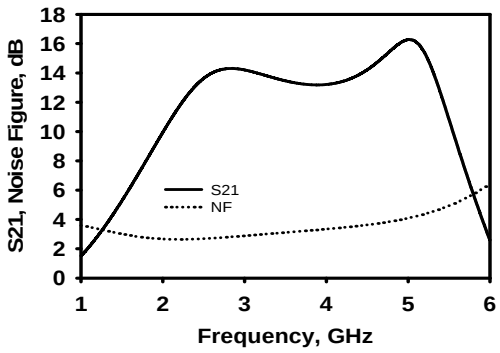


Figure 5(left): Simulated I/O return losses and reverse isolation
Figure 6(right): Simulated voltage gain and noise figure

4. Conclusions

In this paper, a low power and sufficient gain Ultra-Wideband (UWB) LNA for UWB system is proposed. In order to improve a noise performance and input matching, the common source amplifier with inductive degeneration is utilized. In addition, to provide the sufficient gain with low power consumption, an inverter stage with current reuse technique is stacked on the top of the common source amplifier. The total power consumption of the proposed LNA is 6.7 mW. The designed UWB LNA has better ratio of the gain to power consumption comparing to previous researches [2-5].

Acknowledgments

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