Safety Threshold Predictions of On-Chip Interconnects and Devices Illuminated by High-Power Electromagnetic Pulse (HP-EMPs)

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Abstract

In the presence of high-power electromagnetic pulse (HP-EMP), electrical and thermal safety thresholds of some on-chip interconnects, and passive and active devices are investigated in this paper, directly related to their possible electrical or thermal breakdowns. These safety thresholds include (a) maximum current-carrying density of bonding wires; (b) breakdown field strength of thin film capacitors; (c) peak and average power handling capabilities of conventional microstrip interconnects (MI), finite-ground thin film microstrip (FG-TF-MI) and finite-ground thin film coplanar waveguide (FG-TF-CPW) interconnects; and (d) rise in the maximum channel temperature of GaAs field effect transistors (FET). In order to capture these safety thresholds, efficient nonlinear electromagnetic-thermal coupling finite difference time domain (FDTD) and finite element methods (FEM) are implemented in the numerical computation. These safety thresholds will be useful for further taking electromagnetic protection so as to prevent on-chip device breakdown from attack by an HP-EMP.

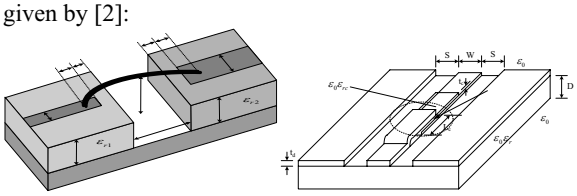
1. INTRODUCTION

In the environment of high power or high field operating environment, breakdown can be easily taken place when an applied voltage or electric field exceeds the electrical or thermal safety threshold of a dielectric or a device. In a semiconductor device, the breakdown can be physically considered as a random nonlinear transient event in which the electrical, thermal and mechanical interactions are coupled to one another. Only in recent years, researchers have realized very challenging safety problems for on-chip devices, circuits and systems illuminated by a high-power electromagnetic pulse (HP-EMP), because their sizes or geometries are minimized and power supplies are reduced significantly. Even the energy density of an ultra-wideband electromagnetic pulse (UWB-EMP) is much smaller than that of an HP-EMP, such as a high power microwave (HPM) pulse, it is still possible to cause signal jam in a circuit or system, as it is indirectly coupled to an on-chip active device through certain conductive way.

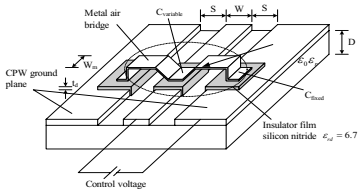
In this paper, we would like to demonstrate some effective ways for predicting electrical and thermal safety thresholds of some on-chip interconnects, passive and active devices in the presence of HP-EMPs, which include bonding wires, TF-CPW-based capacitors, conventional microstrip interconnects, FG-TF-MI and FG-TF-CPW interconnects, RF MEMS switches, and even GaAs field effect transistors. Our motivation is, based on this study, to further explore some effective ways for protecting all the on-chip devices which could be easily broken down.

2. OUTLINES OF SAFETY THREHOLDERS OF BONDING WIRES AND TF-CPW-BASED DEVICES

There are many types of interconnects and passive devices used to build various functional blocks of circuits and systems, especially including bonding wires, TF-CPW-based capacitors, spiral inductors, power dividers, and RF switches [1] *etc*. Some views of their three-dimensional structures are shown in Figs. 1(a)-1(c), respectively. The electrical or thermal safety thresholds for different devices can be described by different parameters. For a bonding wire made of aluminum in air, we can use its maximum current carrying density to describe its electrical safety threshold, and it is given by [2]:



(a) Bonding wire (b) TF-CPW-based capacitor



(c) RF MEMS switch

Fig.1. Three-dimensional views of a bonding wire, a TF-CPW-based capacitor, and a RF MEMS switch.

$$J_{\max}^2 \tau \approx 10^8 A^2 \cdot s / cm^4 \qquad (1)$$

where τ is the duration time of the input current pulse, and A denotes the wire cross section. For a TF-CPW-based capacitor, its electrical safety threshold can be characterized by a breakdown field strength E_{break} or a breakdown voltage V_{break} of the thin dielectric film. Based on the experimental date given in [3], the value of E_{break} versus relative permittivity, denoted by ε_r for most dielectric films, can be described by [3]:

$$E_{break} = 35\varepsilon_r^{-0.64} (MV / cm). \qquad (2)$$

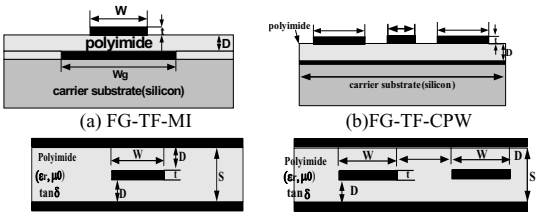
The electrical safety threshold or the pull-down voltage threshold, denoted by $V_{\max}$, is a very important indicator in the design of a TF-CPW-based RF MEMS switch, where the air-bridge region can be mechanically broken down. As defined by Katehi *et al.*, the pull-down voltage is determined by [1]

$$V_p = \sqrt{\frac{8k}{27\varepsilon_0 S} g^3} \qquad (3)$$

where k denotes the spring constant of the membrane, S stands for the contact area between the membrane and the dielectric, and g represents the gap width between the membrane and the dielectric. Hence, the value of $V_{\max}$ should be at least larger than V_p.

3. POWER HANDLING CAPABILITIES (PHC) OF MICROSTRIP AND CPW-BASED INTERCONNECTS

Figs. 2(a)-2(d) show the cross-sectional view of some typical microstrip and CPW interconnects. It should be emphasized that compared to conventional FG-MIs, FG-TF-MIs exhibit different electromagnetic characteristics, because there are significant geometrical differences between them. For example, a FG-TF-MI, as shown in Figs. 2(a), uses a thin dielectric layer of only several or ten microns in thickness deposited on top of a ground plane, and the finite ground plane is deposited onto a carrier substrate, such as GaAs, silicon, or alumina. While the substrate thickness of a conventional FG-MI substrate is usually between 100 to 500 μm, its peak or average PHC will be much larger than that of a FG-TF-MI. Therefore, in the presence of an HP-EMP, FG-TF-MI, FG-TF-CPW or FG-TF-CPW-based devices could be easily broken down, which need to be paid more attention to. Table I summarizes the predicted average PHC of a conventional 50-Ω MI interconnect on single-layer different substrate materials, respectively. Among all the materials, since the value of BeO thermal conductivity is the largest, the corresponding PHC of a MI interconnect fabricated on a BeO substrate is the highest among all substrate materials, while Teflon-based MI interconnects are only suitable for low-power applications, due to their poor thermal conductivity.



(a) FG-TF-MI (b)FG-TF-CPW

(c) FG-SL (d) FG-ECSL

Fig. 2. Cross-sectional views of some microstrip and CPW interconnects.

Table I Comparison of the P_{av} of a 50-Ω MI interconnect on single-layer different substrate materials

Substrate	ε_r	$\tan\delta$	D(μm)	W(μm)	$\Delta T(^\circ C/W)$	$P_{av}(W)$
Teflon	**2.1**	**0.0005**	**1575**	**5013**	**0.4485**	**0.2787**
Quarz	**3.8**	**0.0001**	**1575**	**3370**	**0.0639**	**1.956**
InP	**14.0**	**0.0005**	**50**	**30**	**0.0801**	**1.5605**
Sapphire	**11.7**	**0.0001**	**50**	**37**	**0.09412**	**1.3281**
AlN	**8.8**	**0.0005**	**25**	**24**	**0.02405**	**5.200**
Duroid	**2.2**	**0.0009**	**250**	**760**	**0.7771(0.8682)**	**0.1608(0.144)**
Silicon	**11.7**	**0.1540**	**100**	**75**	**0.1294(0.126)**	**0.966(0.992)**
GaAs	**12.9**	**0.0010**	**75**	**50**	**0.0788(0.0865)**	**1.586(1.445)**
Al2O3	**9.8**	**0.0002**	**250**	**235**	**0.0298(0.027)**	**4.195(4.630)**
BeO	**6.4**	**0.0003**	**250**	**352**	**0.00246(0.00237)**	**50.8(52.774)**
NOSC67	**4.1(10GHz)**	**0.0050**	**115**	**227**	**0.534**	**0.2342**
China 66	**7.7**	**0.0003**	**115**	**135**	**0.5205**	**0.2402**
NGK 73	**7.0**	**0.001**	**115**	**147**	**0.4035**	**0.3098**
IBM 68	**5.0**		**115**	**195**	**0.2331**	**0.5363**
951-AX	**7.8**	**0.0005**	**115**	**133**	**0.4462**	**0.2801**
A6M	**5.9**	**0.0002**	**115**	**170**	**0.4746**	**0.2634**

4. ELECTROMAGNETIC-THERMAL COUPLING NUMERICAL METHODS AND DISSCUSSIONS

As we have pointed out above, since a breakdown taken place in either dielectrics or semiconductors is a multiple interaction process among electromagnetic, thermal and even mechanical fields. Therefore, temperature issue must be treated appropriately if we want to capture the electrical or thermal safety threshold of a dielectric or an on-chip device numerically. Now we will focus on two methods proposed below.

(A) *Nonlinear FDTD*

To obtain the breakdown field strength (E_{break}) of a dielectric, we can use nonlinear FDTD combined with high-field conduction model of the dielectric, in which the electrical conductivity of a dielectric are functions of the electric field strength applied and operating temperature. For example, for the dielectric of polyethylene [4], its electrical conductivity can be described by

$$\sigma = \frac{\exp[a + b/T + k|E|]}{|E|} \qquad (4)$$

where a, b, and k are three coefficients depending on the dielectric type, $|E|$ is the electric field strength applied, and T is the temperature of dielectric. When an HP-EMP is obliquely incident on this substrate, as shown in Fig. 3(a), the updated equation for electric field component E_x in the 2D TE case can be written as：

$$E_{x,<p>}^{n+1}\Big|_{i+1/2,j}=\frac{2\varepsilon\Big|_{i+1/2,j}-\sigma_{<p>}^{n+1/2}\Big|_{i+1/2,j}\Delta t}{2\varepsilon\Big|_{i+1/2,j}+\sigma_{<p>}^{n+1/2}\Big|_{i+1/2,j}\Delta t}E_x^n\Big|_{i+1/2,j}+\frac{2\Delta t}{2\varepsilon\Big|_{i+1/2,j}+\sigma_{<p>}^{n+1/2}\Big|_{i+1/2,j}\Delta t}\times\left(\frac{H_z^{n+1/2}\Big|_{i+1/2,j+1/2}-H_z^{n+1/2}\Big|_{i+1/2,j-1/2}}{\Delta y}\right) \tag{5}$$

A similar equation for electric field component E_y can be also obtained. For each FDTD time step, inner iterations are needed to handle the nonlinear relationship between σ and E, as described by (4). The suffix p represents the pth iteration. In the simulation, σ is defined at half-time steps, and initialized as $\sigma_{<0>}^{n+1/2}=\sigma^n$. It is updated based on the electric field of both the pre-step and the current step. Two schemes are available to calculate the conductivity, as shown below:

$$\sigma_{<p+1>}^{n+1/2}\approx\frac{1}{2}\left(\frac{\exp\left[\left(a+b/T+k\,|\,E\,|_{<p>}^{n+1}\right)\right]}{|\,E\,|_{<p>}^{n+1}}+\frac{\exp\left[\left(a+b/T+k\,|\,E\,|^{n}\right)\right]}{|\,E\,|^{n}}\right) \tag{6a}$$

$$\sigma_{<p+1>}^{n+1/2}\approx\frac{\exp\left[\left(a+b/T+k\left(|\,E\,|_{<p>}^{n+1}+|\,E\,|^{n}\right)/2\right)\right]}{\left(|\,E\,|_{<p>}^{n+1}+|\,E\,|^{n}\right)/2}. \tag{6b}$$

It should be noted that the material properties, *i.e.* ε and σ, as well as the two current densities $\vec{J}_r$ and $\vec{J}_d$ are all defined at the centre of the spatial cell. Therefore, the material properties of two neighbouring grids should be averaged when the field components are calculated. Similarly, an average value of the surrounding field components is needed to obtain the current density at the centre point.

In Fig. 3(a), the permittivity of the dielectric layer is $\varepsilon_r=4$, and the conductivity is described by Eq. (4). The incident pulse is a Gaussian pulse, given by $g(t)=Ae^{-(t-t_0)^2/T^2}$, where $t_0=1\times10^{-13}s$ and $T=4\times10^{-13}s$. The FDTD grids are defined as $\Delta x=\Delta y=1\mu m$, and $\Delta t=dx/(2C)$. Fig. 3(b) shows the electrical conductivity in the substrate at a particular time step, with an incident angle of $\theta=45^o$. Physically, the conductive current density ($J_c=\sigma E$) generated in the conducting region, due to the applied HP-EMP, is several times of the displacement current $(J_d=\varepsilon\frac{\partial E}{\partial t})$, that is

$$|J_c(E_{break})|=n|J_d|. \tag{7}$$

So, it can be concluded that electrical breakdown takes place in the conductive region. In Fig. 3(b), the captured breakdown field strength is $E_{break}=1.6$ kV/mm when we choose n = 5, which agrees with the value reported in [4].

(B) *Nonlinear FEM*

For CPW-built active devices shown in Fig. 4, such as a GaAs effect field transistor (FET), its maximum channel temperature, denoted by $T_{c\max}$, is directly related to its thermal

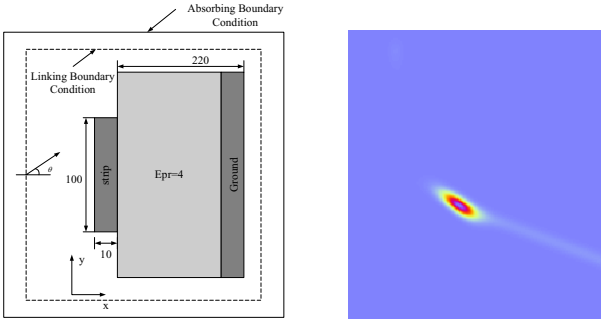


Fig. 3. (a) An HP-EMP is obliquely incident on a microstrip interconnect with $\theta=45^o$; and (b) the electrical conductivity generated in the substrate.

safety threshold. As an HP-EMP is suddenly injected into this transistor, the channel temperature will rise rapidly, and as it exceeds the value of $T_{c\max}$, the thermal breakdown will be taken place. The HP-EMP can be described by a double exponential pulse as follows:

$$\bar{E}_{in}(t)=E_0(e^{-\beta t}-e^{-\alpha t})\qquad t\geq0 \tag{8}$$

where α and β are two parameters to determine the pulse shape.To accurately characterize the thermal safety threshold of this GaAs FET under the impact of an HP-EMP, we need to sovle a non-linear transient heat conduction equation described by

$$\begin{cases}\rho c_\rho\dfrac{\partial T(x,y,z,t)}{\partial t}+\kappa_p(T)\nabla^2T(x,y,z,t)=g(t) & p=1,\ \cdots,\ \mathrm{M}\\ T\big|_{\Gamma a}=T_0\\ \dfrac{\partial T}{\partial n}\Big|_{\Gamma q}=-h(T-T_0)\end{cases} \tag{9}$$

where $T(x,y,z,t)$ represents the temperature distribution in the whole domain of interest; $\partial T/\partial n$ stands for the normal derivative of the temperature on the boundary; Γ_a is the Dirichlet boundary, Γ_q is the Neumann boundary, κ_p is the thermal conductivity, $g(t)$ is the heat generation rate of the equivalent heat source, h is the convective coefficient, and T_0 is the ambient temperature, respectively. In the above GaAs FET, most of the heat is generated at the depletion region produced by the gate. An exact description of the dynamic heating process is very complicated under the illumination of an HP-EMP. Instead, we can assume the heat is generated by a transient source with an equivalent volume source, just embedded under the metal gate. The source length is slightly larger than or equal to the gate length, which is biased towards the drain pad [5].

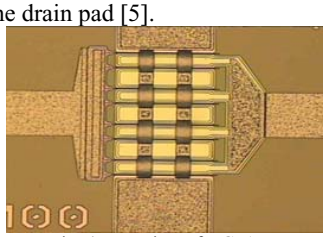


Fig. 4. Top view of a GaAs FET

According to the Ritz differentiation, the functional form of Eq. (9) can be rewritten as:

$$F(T) = \int_{\Omega} \kappa \left\| \nabla \varphi \right\|^2 d\Omega . \tag{10}$$

After introducing an FEM interpolation function, the functional form of $F(T)$ in Eq. (10) can be expressed as

$$F^{(e)}(T) \cong \frac{1}{2} \left[T^{(e)} \right]^T \left[K^{(e)} \right] \left[T^{(e)} \right], \tag{11}$$

where $T^{(e)}$ represents the element temperature vector in the FEM nodes, $\left[K^{(e)} \right]$ is the temperature-dependent element stiffness matrix, whose conformal coefficient is given by

$$K_{ij}^{(e)} = \kappa^{(e)} \int_{\Omega^{(e)}} \nabla N_i \cdot \nabla N_j d\Omega . \tag{12}$$

The stationary points of the functional $F^{(e)}(T)$ are obtained by minimizing Eq. (11) with respect to the nodal values of the potential *T*. In this procedure, a linear equation system can be obtained as

$$\left[K^{(e)} \right] \left[T^{(e)} \right] = \left[f^{(e)} \right], \tag{13}$$

where $\left[f^{(e)} \right]$ is the vector of heat load. To solve Eq.(13) numerically, the iterative scheme of a variant of Newton-Raphson iteration, which makes use of the continuity of the temporal discretion, can be adopted [6]. On the other hand, we should consider the temperature-dependent characteristics of the thermal conductivity of GaAs. Therefore, an additional Newton-Raphson iterative scheme should be adopted [7]. Based on the above formulas, a hybrid FEM code was developed so as to characterize the thermal safety thresholds of some GaAs FETs under the illumination of different HP-EMPs. The thermal boundary conditions on all the boundaries were assumed adiabatic, except that the bottom of the structure was assumed to have a constant temperature of 273*K*. Thus, the initial temperature was also assumed to be 273*K*. Fig. 5 shows the variation of the maximum channel temperature $T_{c\max}$ of a GaAs FET as a function of the pulse duration time. In Fig. 5, the GaAs FET is illuminated by a double exponential pulse (med) with the input power density P_{input} =1, 2, 3, and 4 $W/\mu m^3$, respectively. It is obvious that there is time delay between the maximum value of the $T_{c\max}$ and that of the EMP, and all the performance parameters of the GaAs FET will be reduced significantly with increasing the $T_{c\max}$. Usually, the safety temperature of a GaAs FET should not exceed 100-120 ^oC ; otherwise, the system will be broken down thermally.

CONCLUSIONS

In this paper, it has been demonstrated that under the illumination of a high-power electromagnetic pulse, (a) electromagnetic and thermal interactions are strongly coupled to each other in on-chip passive and active devices and circuits; (b) electric filed strength- and temperature-dependent conduction model of the electric conductivity of dielectrics are very important for capturing their breakdown field strengths numerically; (c) electrical and thermal safety thresholds for most on-chip functional blocks or circuits are still unknown, and there are still some more studies to be further carried out, and (d) in order to prevent on-chip devices and circuits from an intentional electromagnetic attack, the predicted electrical and thermal safety thresholds must be implemented in their design using new structures, new materials combined into advanced fabrication technology.

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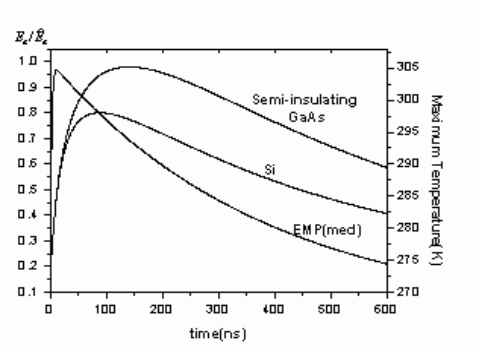

Fig. 5. The maximum channel temperature $T_{\max}^{(p)}$ versus pulse duration time.

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