FABRICATION OF A MILLIMETER WAVE HOLLOW WAVEGUIDE BY A LARGE-SCALE SILICON-PROCESS

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1. Introduction

When a waveguide slot array antenna for millimeter-wave and sub-millimeter wave bands are made by mechanical machining, fabrication errors will become a problem. The authors take silicon process into consideration as a method of making waveguide in such high frequency band. Integration with RF devices and a waveguide slot array antenna in a silicon substrate would be attractive. .

In this paper, the authors design and fabricate a 100GHz hollow waveguide by using the silicon process for semiconductor devices. The feeding structure for measuring the performance of the waveguide is also designed in its broad wall. The waveguide is made by bonding together the upper silicon substrate including the feeding parts and the bottom silicon substrate including the trench as shown in Fig.1. The upper silicon substrate has thickness of 200 ± 25μm and the dielectric constant is 11.9. The hollow trench has the depth of 200μm~300μm, width 1mm and the length 1cm.

A long slender trench in the bottom substrate oriented in the (100) plane is made by KOH anisotropic wet etching on a silicon wafer and its surface is plated with gold. The silicon wafer is able to be etched to a depth of about 300μm for about 10 hours using a SiO_2 mask formed by the thermal oxidation. We confirm that the (111)-side walls are made with an inclined angle of 55 degrees. The mode propagation in the double layer structure of silicon and air is analyzed by using a finite element method simulator Ansoft HFSS. The feeding part, also designed by HFSS, is etched on the upper substrate; it consists of coupling slots with a co-planar waveguide line for measurement by probes.

2. Structure of Silicon Processed Waveguide

Silicon wafers are used as the substrates. The method of KOH anisotropic etching is used to make a trench. The bottom substrate including the trench and the upper substrate including the feeding part are made separately and bonded together as shown in Fig.1. Posts to electrically connect with the bottom substrate are made in the upper substrate and are plated with gold on all the surfaces. The feeding part consists of a coplanar waveguide line with a radiation slot for measurement with a probe.

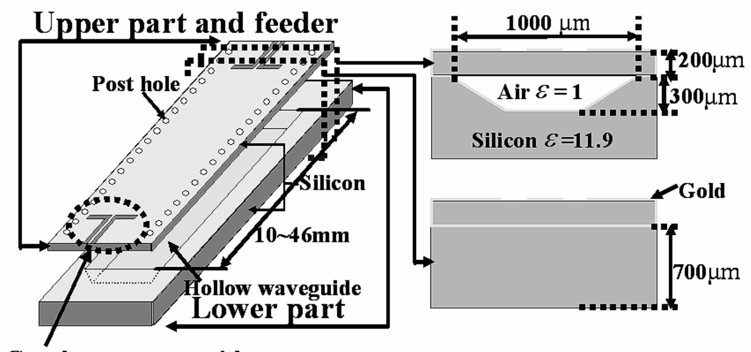

Figure 1: Structure and cross section

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3. Wide and Long Etching of (100) Surfaces with Potassium Hydroxide

To obtain a deep and wide trench structure, we use chemical anisotropic etching of a silicon wafer oriented in the (100) plane [1],[2]. The key point of the technology is the ability to etch a large (100) area to depths of hundreds of microns (200 to 300μm typically) with a good yield. High-quality etching requires straight-cut sidewalls and a flat bottom surface. The potassium hydroxide-water (KOH-water) solution is used for the silicon etching. Characteristics of this etchant are strongly dependent on both temperature and solution concentration [3], [4] and must be determined according to the specific application. The mask for silicon etching is made from silicon dioxide [5].

Thermal oxidation is the method used to form a silicon dioxide film. The etch rate of silicon dioxide is much lower than that of silicon for KOH-water solution. The thickness of the silicon dioxide film is determined from the etching depth of silicon and the selectivity of etch rate between silicon and silicon dioxide for KOH-water solution. For deep etching of silicon, a thick silicon dioxide film is needed. By experiments, we determine the following etching conditions.

The thickness of the silicon dioxide film is 1μm. The etch rate along the <100> direction, measured at 65~75 degrees C. for a solution of 30~40% (volume) KOH, is about 50μm per hour. Reproducible results with a good yield are obtained for these parameters. The scanning electron microscope (SEM) picture of an etched cross section and the picture of the whole bottom structure in silicon substrate are shown in Fig.2. The lengths of the trenches are 10mm, 20mm, 30mm, 40mm and 46mm.

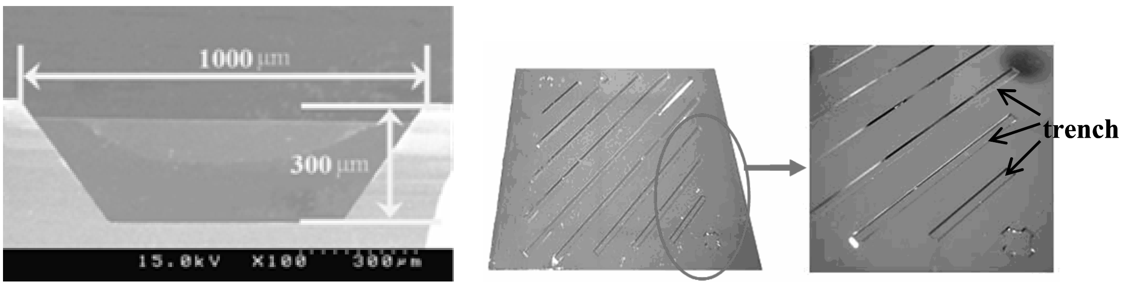

Figure 2 : Photo of the bottom substrate

4. Design and Simulation results

The design frequency of waveguide is 100GHz. The feeding part is designed by using a co-planar waveguide line with a slot. The structure is designed with Ansoft HFSS. In the first place, a waveguide dimension for single mode propagation is obtained. The waveguide shape is not simply a rectangular but is a trapezoid.

It consists of a silicon substrate of 200 ± 25μm thickness and a hollow waveguide of a depth around 200μm~300μm made by chemical etching. Due to the etching of the (100)-oriented silicon, the waveguide has a trapezoidal cross section with side walls angled at 55 degrees. This is considered in the designs of the waveguide and feed. Furthermore, the thickness of the upper silicon substrate needs to be included in the simulation. The suitable width for which only a single mode propagates is calculated using the structure shown in Fig.3 (a) by changing the size of the rectangular waveguide width W. For W from 0.87mm to 1.72mm, only a single mode propagates in a waveguide with a thickness of 200μm~300μm. The simulation result for the rectangular waveguide is given in Table 1.

Then, a value for W (Fig.3 (b)) between 0.93mm and 1.85mm is assumed and modes are analyzed for the trapezoidal waveguide. It is confirmed that only a single mode propagates for this range of the width.

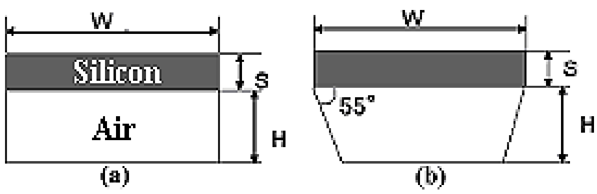

Figure 3 : Analysis model of Cross section

S (μm)	H (mm)	W (mm)
200 ± 25	0.2	0.97~1.93
	0.3	0.93~1.85

Table 1 : W for single mode propagation

However, in order to bond the upper and bottom substrates together, a certain amount of margin in the width is needed on both sides of the upper silicon substrate as shown in Fig.4. The width of the hollow waveguide is fixed to 1.4, 1.2 and 1.0mm and the width of the upper silicon substrate SW is varied. The result is given in Table 2.

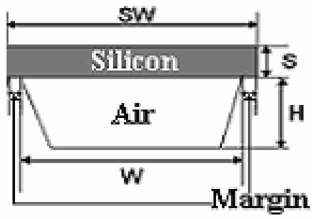

Figure 4 : Analysis model of Cross section

H(μm)	S(μm)	W(mm)	SW(mm)
200~400	200 ± 25	1.4	1.4 ~ 1.48
		1.2	1.2 ~ 1.34
		1.0	1.0 ~ 1.18

Table 2 : W for single mode propagation

Based on this result, the width of the upper silicon substrate is set to 1.18mm, the width of hollow waveguide in the bottom substrate is set to 1.0mm. The feeding part is designed for the specific structure thus designed, by full model EM simulation by HFSS. We design to minimize the reflection.

As a result, the width of the signal line and the gap of the co-planar waveguide line are 32μm and 20μm, respectively. The slot length, slot width, and aperture position are 690μm, 84μm, and 880μm as shown in Fig. 5, respectively.

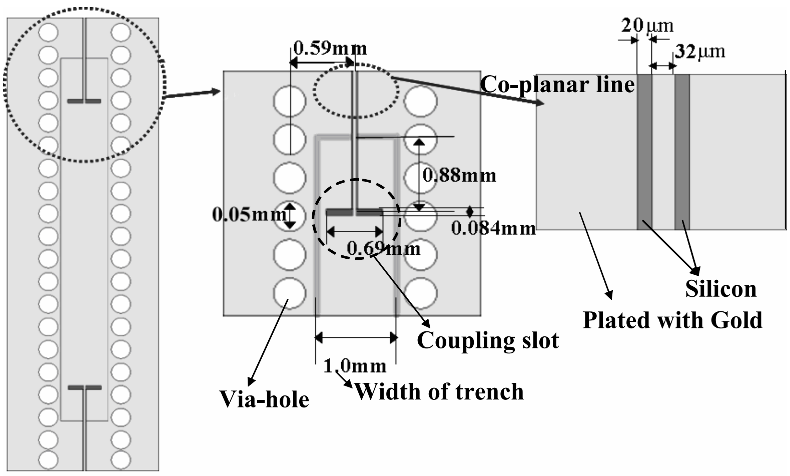

Figure 5 : Results of feeding parts

A plot of S_{11} and S_{21} versus frequency is shown in Fig. 6. As shown Fig.6, the reflection at the feed, S_{11}, is less than -40dB at the design frequency and the magnitude of transmission in the waveguide, S_{21}, is -2.3 dB. The total loss is -3.9 dB, which includes the loss of the co-planar waveguide line, propagation loss in upper silicon substrate and the radiation from the coupling slots. Fig. 7 depicts the electric field in the model from the side cross section.

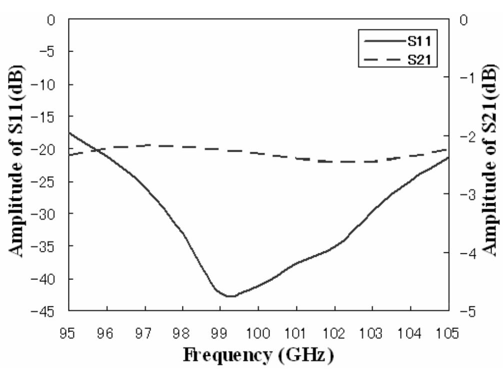

Figure 6 : S_{11} and S_{21} versus frequency

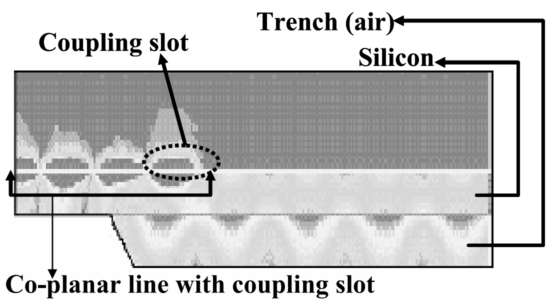

Figure 7 : Electric-field on the cross section

5. Conclusion

We have applied a silicon-process to make a hollow waveguide in the millimeter wave band at 100GHz. For the silicon-process to make the hollow waveguide, KOH anisotropic wet etch is used. Waveguides with common thickness 300μm and lengths 10, 20, 30, 40 and 46mm, respectively, are constructed. The feeding part in the upper substrate consists of a co-planar line with slots for measurement with a probe. The waveguide is designed using the finite element method simulator HFSS by varying the form and positions of the various waveguide elements so that power is efficiently supplied in the waveguide. We design the model where 59% of the power propagates in the waveguide.

We show the feasibility of fabrication of a hollow waveguide which uses silicon-process in the high frequency range. It is attractive to integrate RF circuits in a silicon based slotted waveguide array antenna. The difficulty in fabrication is positioning and bonding the upper and bottom substrates and metal-plating the surface with gold. We will fabricate the waveguide and present the measured transmission characteristics.

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