Distributed Modeling of On-chip Power Distribution Networks Using Conformal Mapping and FDTD Method

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Abstract: This paper presents the modeling and simulation of simultaneous switching noise (SSN) in on-chip power distribution networks (PDN). The circuit model of power buses over lossy silicon substrate is extracted as frequency dependent RLGC elements. The coupling between conductors on adjacent layers is represented as coupling capacitors. Accurate analytical formulae are derived to extract the RLGC transmission line parameters and crossover capacitance using conformal mapping techniques. The effect of silicon substrate and mutual capacitance upon switching noise is demonstrated through a full chip power grid simulation using the Finite Difference Time Domain (FDTD) method along with Debye approximation.

I. INTRODUCTION

While the size of semiconductor product keeps on shrinking, more digital and analog/radio-frequency (RF) functionalities are being integrated into a single chip through System-on-Chip (SOC) or through System-on-Package (SOP) technologies. A robust power distribution network is critical in ensuring the reliable operation of high performance digital and mixed-signal systems. Simultaneous switching noise caused by the switching activity of high speed CMOS circuits contributes to the malfunction of digital sub-systems as well as the performance deterioration of its neighboring analog and RF circuits.

Extensive research for on-chip PDN has been carried out for IR drop analysis and transient power supply analysis by numerous authors. This consists of single R, L, C representation for the power grid and resonance analysis [1]. Recently, the effect of substrate resistivity upon the switching noise in on-chip PDN has been quantified in [2], and the large circuit representing the full chip power grid has been simulated using FDTD method [5-6].

The equivalent circuit model developed in [2] included the coupling between the power buses on the same layer. In this paper, the circuit model is extended to include mutual capacitance between neighboring layers of the power grid. Various numerical methods have been used in the past to extract crossover capacitance formed by the orthogonal interconnects in a multi-layered structure [7]. Instead of numerical methods that are time consuming, analytical expressions of crossover capacitance has been derived in this paper, which gives accurate results and is more efficient.

The remainder of the paper is organized as follows. Section II discusses the frequency dependent RLGC parameter extraction for power grids. In section III, the fringing field distance is calculated for the overlapping interconnects. Section IV provides details on the derivation of the analytical expressions for crossover capacitance. Section V discusses the FDTD method and Debye approximation for time domain simulation. The full chip power grid with and without mutual capacitive coupling between different layers are simulated and results are compared in Section VI.

II. Coplanar Multi-conductor Parameter Extraction

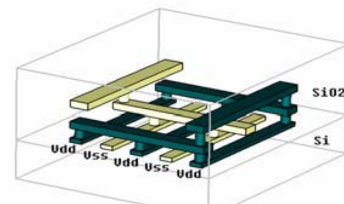

Fig. 1. Side view of on-chip power grid.

A side view of on-chip power grid is shown in Fig.1. The power (Vdd) and ground (Vss) buses are parallel in the same layer, but orthogonal to each other on neighboring layers. The 3-D power grid is embedded in SiO_2 and is present over silicon substrate.

Complex image theory [3] has been used in the past to model the coplanar waveguide (CPW) [4] over lossy

silicon substrate. To take into account the loss due to eddy currents, the substrate is approximately replaced by a conducting image plane located at a complex distance away from the metal-SiO_2 interface.

The same principle can be applied on coplanar multi-conductor (CMC) structures in on-chip PDN. After computing the effective permittivity ε_{eff}, characteristic impedance Z and propagation constant γ, RLGC parameters can be extracted [2].

III. Crossover Capacitance Calculation

In Fig. 1, two buses crossing each other with the same potential are connected by a via. However, the crossover of two interconnects of opposite potential buses results in a capacitor, which induces coupling between adjacent layers. For characterizing the crossover capacitance, two issues need to be studied: namely, 1) the effect of neighboring interconnects on the crossover capacitance and 2) the fringing distance of the electric field for calculating the capacitance.

As shown in Fig. 2, the effect of the neighboring interconnects on the crossover capacitance has been studied as a ratio of capacitances, $C_{parallel}$ over ($C_{parallel}$+$C_{crossover}$), where $C_{parallel}$ denotes the mutual capacitance between V1 and G1 and $C_{crossove}$ denotes the crossover capacitance between V1 and G2. The capacitance ratio calculated as a function of l/d is shown in Fig. 3, where l and d are the distance between V1 and G1 and the thickness of the SiO_2.

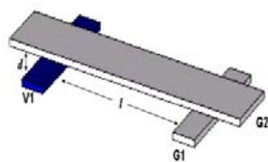

Fig. 2. Crossover structure

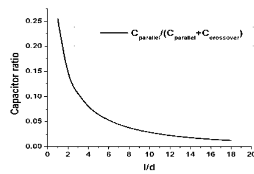

Fig. 3. Capacitance ratio

The capacitance ratio decreases fast and the value of $C_{parallel}$ is very small compared to the total capacitance. When the distance l is ten times greater than the SiO_2 thickness, the effect of the neighboring interconnects on crossover capacitance can be ignored.

In Fig. 2, the electric field is not confined within the cuboidal volume formed between two orthogonal strips. Instead, it extends beyond the volume as fringing field. To balance the accuracy and computational complexity of the problem, the two interconnects should be truncated at a finite distance away from the cuboidal volume. The distance of the fringing field or fringing distance is quantified here as a plot of the magnitude of electric field intensity versus x/d in Fig. 4, where x is the distance between the point of observation and the edge of cuboid.

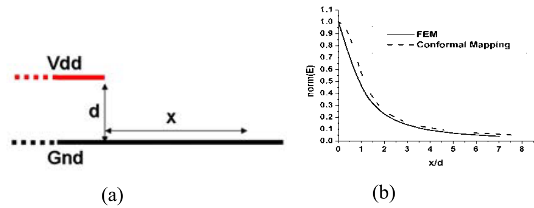

Fig. 4. Fringing filed of crossover a) Finging distance b) Magnitude of electrical field vs x/d

The fringing electric field E has been calculated in Fig. 4 using FEM as well as the conformal mapping technique, which is derived in detail in Appendix A. Its magnitude, $|E|$, normalized to the value of $|E_{x=0}|$, is plotted along the Gnd for x>=0 in Fig. 4b. It can be observed that the electric field attenuates quickly beyond the edge of the cuboid. At a distance that is four times the SiO_2 thickness away from the edge, its magnitude is less than ten percent of the original value. Since the electric energy density and corresponding capacitance is proportional to the square of $|E|$, the contribution of the field beyond the distance $4\times d$ can be neglected. Hence, two orthogonal interconnects can be truncated at a distance of four times SiO_2 thickness d away from the overlapping area, based on which further crossover capacitance calculations can be carried out.

IV. Conformal Mapping for Crossover Capacitance

After applying the fringing distance criterion and truncating the orthogonal interconnects, the crossover capacitance has the structure as shown in Fig. 5a. The coupling capacitance can be extracted using FEM [7]. However, in this section, analytical expressions for the crossover capacitance have been derived using conformal mapping, which can yield accurate capacitance and render more physical understanding.

The total crossover capacitance can be approximately divided into three major components as

shown in Fig. 5b. Capacitance $C_{overlap}$ comes from the field confined within the center cube and can be simply calculated as $C_{crossover} = \varepsilon_{siO2} * (a * b) / d$. Capacitance $C_{finging}$ denotes the contribution from the fringing field which is derived under the assumption that two conductors are infinitely thin. The effect of the conductor thickness is considered as capacitance C_{side}.

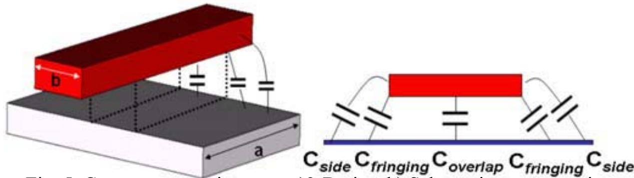

Fig. 5. Crossover capacitance. a)3-D view b) Schematic representation

As shown in Fig. 6, due to symmetry, only half of the electric field needs to be evaluated after imposing the magnetic wall along the center line. Furthermore, the capacitance per unit length of the half cross section can be approximated by the summation of two capacitances, which are related to $C_{finging}$ and C_{side} and shown in Fig. 6b and Fig. 6c, respectively.

The capacitance per-unit-length $C_{finging_PUL}$ and C_{side_PUL} are determined by going through two conformal mappings derived in (1), (2) and shown in Fig. 7 and 8, respectively. To achieve the actual value, they are doubled to account for the other half cross section and are multiplied by the width of the strip.

To validate the accuracy of the approach proposed above, results for two crossover structures obtained by the conformal mappings are compared with those computed by using FEM [7]. In the examples, two conductors are of thickness 0.3μm, which present in a homogeneous dielectric of material SiO_2 with ε_r=4. The dielectric distance between two interconnects is 1μm and the capacitances are shown in Table 1.

V. Equivalent Circuit and FDTD Solution

FDTD method is used to simulate the on-chip power distribution network, in which computation of the branch currents and node voltages are alternately calculated as time progresses. To take into account the frequency dependent RLGC parameters of each segment of the power grid, Debye approximation for N=1 [6] is used for frequency dependent power grid simulation as shown in Fig. 9.

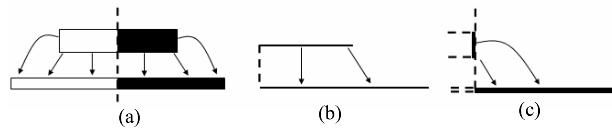

Fig. 6. Field distribution of crossover structure

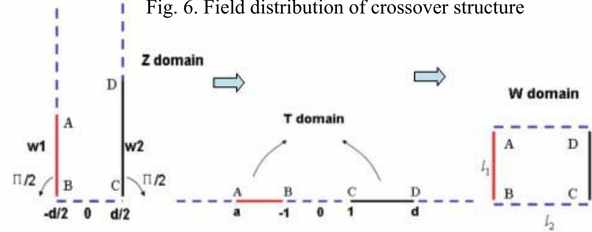

Fig. 7. Conformal mapping for $C_{fringing}$

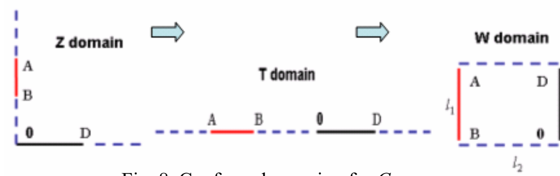

Fig. 8. Conformal mapping for C_{side}

$$T(z) = \sin(\frac{\pi}{d} z),\ W(t) = \int^{t} \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}}$$

$$l_1 = \int_{a}^{-1} \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}},\ l_2 = \int_{-1}^{1} \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}}$$

$$C_{half} = \frac{\varepsilon \cdot l_1}{l_2},\ C_{fringing_PUL} = C_{half} - \frac{\varepsilon \cdot w1}{d} \quad (1)$$

$$T(z) = z^2,\ W(t) = \int^{t} \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}}$$

$$l_1 = \int_{A}^{B} \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}},\ l_2 = \int_{B}^{0} \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}}$$

$$C_{side_PUL} = \frac{\varepsilon \cdot l_1}{l_2} \quad (2)$$

Crossover (μm)	C_{FEM} (fF)	$C_{mapping}$ (fF)	Error (%)
a=10, b=20	10.0059	9.9312	0.75
a=5, b=15	4.6594	4.5449	2.5

Table. 1 Capacitance comparison

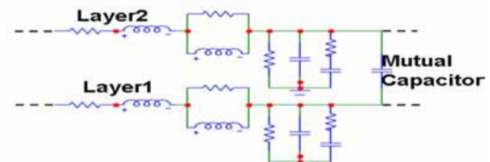

Fig.9. First order Debye approximation and mutual capacitor

VI. Full Chip Power Grid Simulation

In [2], the full on-chip power grid has been simulated as a frequency dependent network, which takes into account the effect of lossy silicon substrate.

The equivalent circuit model is extended here to include the capacitive coupling between opposite potential buses on neighboring layers. The crossover capacitance is a periodical disturbance to the RLGC model of the on-chip power grid. The mutual capacitance augments the shunt capacitance of the power grid, which changes its characteristic impedance value.

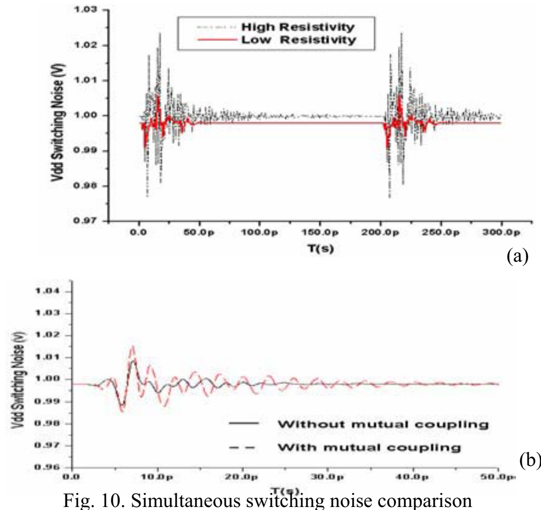

Fig. 10. Simultaneous switching noise comparison

a) between different substrates b) with and without mutual capacitance

The effect of capacitive coupling on SSN is demonstrated through a simple test vehicle used in [2], which is a 4mm×4mm chip with a three-layer power grid where the pitch of each layer are 20μm, 40μm, and 80μm, respectively. The width of the power bus is 5μm and the thickness is 1μm. Switching current is modeled as a triangular current pulse with 1ps rise time and 2ps fall time. The supply voltage is 1v and the power density at the center of the chip is 300mw/(mm^2). The voltage at a node 1mm away from the chip center at the bottom layer is recorded. In Fig. 10a, the waveforms of simulation for the chip with different substrates, namely, high resistivity with ρ =100Ω-cm and low resistivity with ρ =5Ω-cm show the effect of silicon substrate. It can be seen that lossy substrate helps attenuate the on-chip simultaneous switching noise. Another two simulations are done for the chip with the same physical setup but with and without the mutual capacitor. The waveforms of both are compared in Fig. 10b. The extra capacitance increases the propagation constant and alters the frequency response of the transmission line, which leads to more delay and different magnitude for switching noise in the time domain.

VII. Conclusion

The closed-form expression of crossover capacitance for orthogonal interconnects in on-chip power distribution network has been presented in this paper. The effect of capacitive coupling on switching noise in on-chip power distribution network has been quantified through full-chip simulation.

APPENDIX A

Maxwell's transformation $z=d/\pi(1+W+e^W)$ [4] maps the complex variable $W=u+i\cdot v$ into $z=x+i\cdot y$. The line $u=K_u=constant$, is mapped to the arc in Z domain as the electric field line at the edge of two parallel plates. Its parametric equations can be expressed as (3).

$$x=f(v)=d/\pi(1+K_u+e^{Ku}\cos(v)),\ y=g(v)=d/\pi(v+e^{Ku}\sin(v)) \quad (3)$$

Once the potential difference between two plates is set, $|E|$ is inversely proportional to the length of the arc. The formula (4) can be used to compute the length of the arc in Cartesian coordinate from the parametric equations.

$$l=\int_{\alpha}^{\beta}\sqrt{f'^2(v)+g'^2(v)}dv \quad (4)$$

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