EMC Macro-Model with I/O (LECCS-I/O) for Multi-Bit Drives

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Abstract

A LECCS-I/O model of a multi-bit drive IC was devised for reducing electromagnetic interference. An equivalent power circuit model of the IC (74LVC04) was derived from measured power impedances by measuring four test boards. Each board consisted of a single layer, a power-impedance measurement port, and two output ports from the six IC drivers. The power impedance was measured for various combinations of loading capacitances and ratios of high-impedance drivers to low-impedance drivers. The ratio of high-capacitance to low-capacitance drivers ranged from 0:6 to 6:0, and the loading capacitance varied from 1.5 pF/bit (open state) to 37 pF/bit. The power impedance of the IC can be easily modeled as that of an equivalent linear (resistance, inductance, and capacitance) circuit that combines high-impedance and low-impedance circuits. The multi-bit drive LECCS-I/O model could estimate the power impedance under high and low driver loading impedances to within an average error of 1.1 dB up to 500 MHz.

Keywords: EMI Simulation, LECCS, Impedance, PCB, Power noise, Load Depandency

1 Introduction

Electromagnetic interference (EMI) due to the switching current of ICs is still a major problem in many electric products such as digital consumer products, computers, and automotive electric units. When the switching current flows through cables and the external power bus and I/O bus on a board, they behave as antennas and radiate electromagnetic waves as unintended noise.

An EMI model for ICs is a vital tool for circuit and board designers [1, 2]. We therefore devised measurement and modeling methodology for building linear equivalent circuits for ICs [3–8], and here we report the application of this methodology to an IC with multi-bit drivers [9].

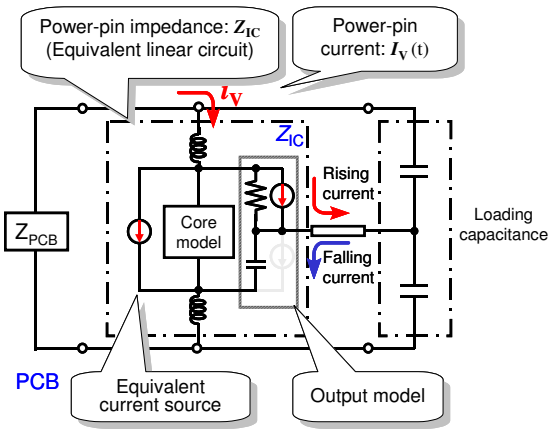

Figure 1: LECCS-core and -I/O model for power current noise.

2 LECCS Model

We previously developed a "linear equivalent circuit and current source for core" (LECCS-core) model to describe the radio-frequency (RF) power current produced by an IC [3–6]. That model can trace a wide range of power bus loading and can be described in the frequency domain. According to the LECCS-core model, the magnitude and phase of the RF power current flowing from an internal current source of an IC is determined by the impedance relation between the power bus of the board and the power circuit of the IC. The impedance of an input or output (I/O) part of an IC, however, especially the drivers of an IC, changes cyclically to and from high and low values.

We therefore expanded the one-port LECCS (core) model to a two-port model (i.e., one with a power port and an I/O port) that traces the dependency of the RF power current on the loading of the power bus and the I/O bus. We call this model the "LECCS-I/O" model (Fig. 1) [7–9].

3 Measurement and Modeling

Figure 2 is a top-view photograph of a test board, which is a single-layer board on which are mounted a small-scale IC (74LVC04) and two loading capacitors. All combinations of the high-impedance

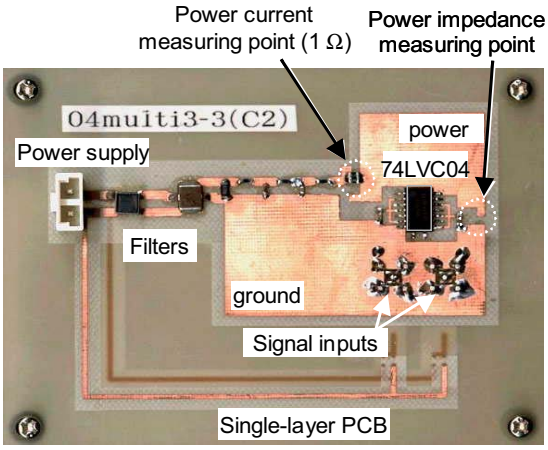

Figure 2: Test board (single layer).

and low-impedance states of the IC drivers were measured using four test boards, combination the ratio of the drivers were 6:0, 5:1, 4:2 and 3:3 of the high vs. low of outputs. The boards corresponding to the driver ratio of 2:4, 1:5 and 0:6 were used the 4:2, 5:1 and 6:0 boards with invert input.

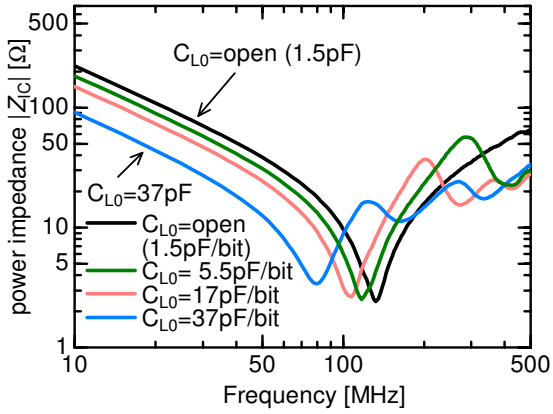

Figure 3: Measured power impedance of IC with three high-impedance drivers and three low-impedance drivers.

The power impedance measured when the ratio of the drivers was three-to-three is plotted against frequency in Fig. 3 for various values of loading capacitance ranging from 1.5 pF/bit (open state) to 37 pF/bit, and the power impedance measured at 17 pF/bit and driver ratios from 0:6 to 6:0 is similarly shown in Fig. 4.

To delive a linear equivalent circuit from as many circuits as possible, we assumed the circuit topology shown in Fig. 5. This topology is considered to be similar to the physical structure of the IC. The IC has common package inductors L_{p} at the power pin and L_{n} at the ground pin. The package was a 14-pin small outline package (SOP), and the inductance of each pin was differ-

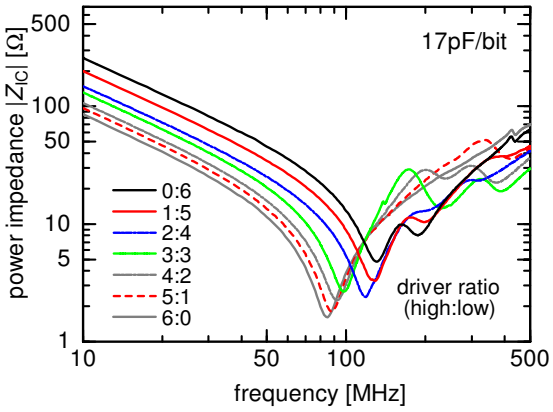

Figure 4: Measured power impedance of ICs with various ratios of high-impedance drivers to low-impedance drivers.

ent because the length of each pin was different. We assumed, however, that the inductance (L_{o}) of each driver pin was the same.

Since the power impedance of the model should depend on the combination of the states of the output impedances and the loading capacitances (C_{L1} and C_{L2}), the model includes two parts: an output high-state circuit with impedance $Z_{\mathrm{H}i}$ and an output low-state circuit with impedance $Z_{\mathrm{L}j}$. Here, "i" and "j" mean the number of driver circuits connected in parallel to output 1 and output 2. The "i" high-output driver circuit ($Z_{\mathrm{H}i}$) consists of linear circuit elements (R_{p}, R_{n}, C_{n}, R_{o}, and L_{o}). To calculate the power impedance of the circuit in Fig. 5, we introduced admittance $Y_{\mathrm{H}i}$ and $Y_{\mathrm{L}j}$ of $Z_{\mathrm{H}i}$ and $Z_{\mathrm{L}j}$.

$$Y_{\mathrm{H}i} = (Z_{\mathrm{H}i})^{-1} = i \cdot \frac{Y_{\mathrm{H}n}}{n} \quad (1)$$

$$Y_{\mathrm{L}j} = (Z_{\mathrm{L}j})^{-1} = j \cdot \frac{Y_{\mathrm{L}n}}{n} \quad (2)$$

The admittance ($Y_{\mathrm{H}i}$) of an "i−bit" parallel circuit is calculated as

$$i + j = n \ (= 6). \quad (3)$$

Here, "n" means the number of the drivers in the IC.

The power admittance of the combination an "i" high and "j" low circuit (Y_{ij}) is calculated as below.

$$Y_{ij} = Y_{\mathrm{H}i} + Y_{\mathrm{L}j} \quad (4)$$

Accordingly, a power impedance of the combination an "i" high and "j" low circuit (Z_{ij}) is represented the following equation:

$$Z_{ij} = (Y_{ij})^{-1} = \frac{n}{i/Z_{\mathrm{H}n} + j/Z_{\mathrm{L}n}} \quad (5)$$

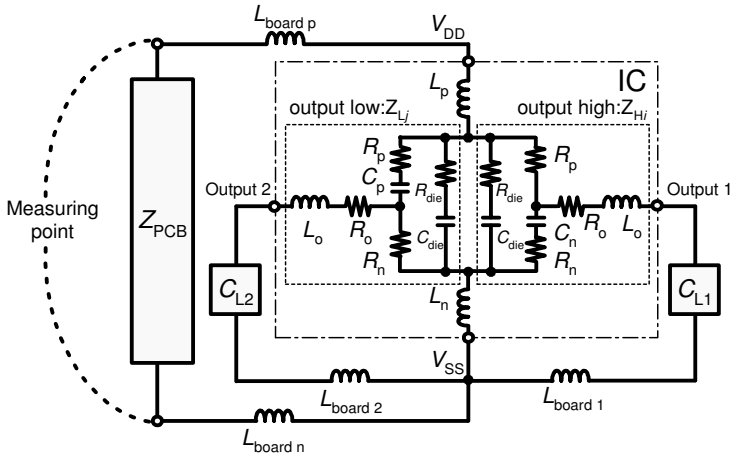

Figure 5: Equivalent circuit of multi-bit LECCS-I/O model.

The loading capacitors (C_{L1}, C_{L2}) are calculated as below.

$$C_{L1} = i \cdot C_{L0} \quad (6)$$
$$C_{L2} = j \cdot C_{L0} \quad (7)$$

Here, C_{L0} is the loading capacitance of each driver. The optimal values of parameters Z_{Hn} and Z_{Ln}

Table 1: Optimal model parameters of power impedance (Z_{IC})

IC	parameters	Z_{Hn}	Z_{Ln}
p-MOS side	L_p	5.2 nH	←
	R_p	3.4 Ω	2.0 Ω
	C_p	-	8.8 pF
n-MOS side	L_n	4.4 nH	←
	R_n	2.0 Ω	3.0 Ω
	C_n	4.7 pF	-
output	L_o	0.34 nH	←
	R_o	7.8 mΩ	←
Board parameters		C_{VG} ‡	1.5 pF
L_{board_p}	3.9 nH	L_{board_n}	7.5 nH
L_{board1}	4.56 nH	L_{board2}	←

(‡Parastic capacitance of the test board)

are listed in Table 1. The package inductances of the power and ground pin (L_p, L_n) are fixed for all driver state ratios between 0 and 6. The inductance (L_o) of the signal pins, however, depends on the ratio of the driver states because the current of each signal does not flow in the same direction and the magnetic flux generated by the current changes with the ratio of drivers.

Using the parameters listed in Table 1, we compared, from $i = 0$ to $i = 6$, the power impedance (Z_{IC}) calculated from Eq. 5 with the measured impedance. Figure 6 shows the measured and simulated impedance profiles for high-to-low ratios of

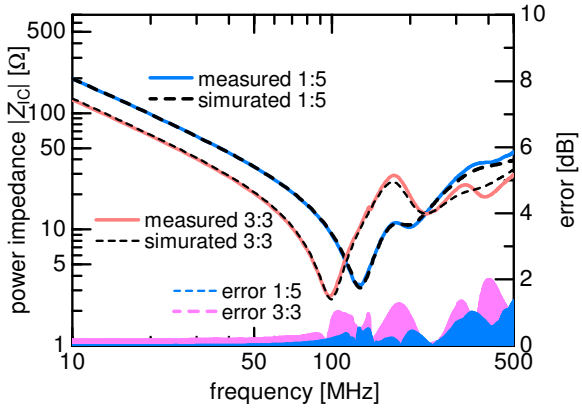

Figure 6: Power impedances and errors of multi-bit drive IC (each $C_{L0} = 16$ pF). (Dark grey hatching and pale one are error of 1:5 and 3:3 ratio, respectively.)

1:5 and 3:3 at C_{L0}=16 pF/bit. The difference errors in decibels are also hatched as a dark and a pale grey respectively, which are well fitted at errors within 2 dB up to 500 MHz.

The frequency errors of the first valley of the measured and simulated impedance profiles are plotted in Fig. 7, which shows that the frequency errors are small (within 6.25 MHz). Since the first valley is due to the resonance of the package inductor and the loading capacitor of the circuit, this figure shows that the impedance of the multi-bit LECCS-I/O model (Fig. 5) is able to provide the dependency on the loading capacitor and the combination of the driver states.

The averaging error between the measured and simulated power impedances, for frequencies up to 500 MHz, is plotted in Fig. 8. The maximum error was small: less than 1.1 dB for all the combinations of the driver ratios and at C_{L0} values of 1.5, 5.5, 17, and 37 pF.

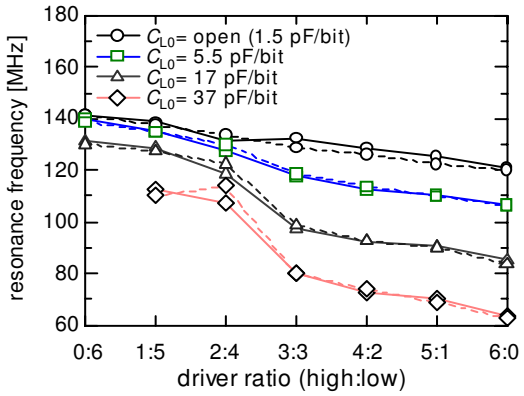

Figure 7: Measured (solid lines) and simulated (broken lines) frequency at first valley of power impedance profiles.

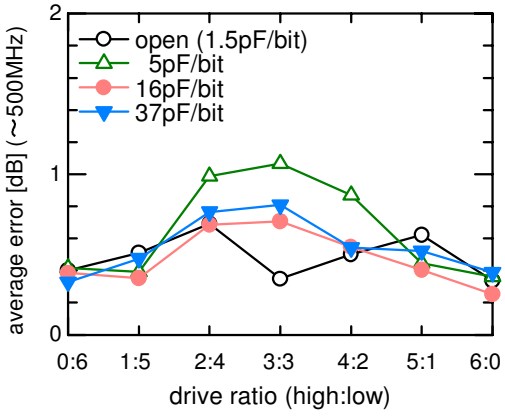

Figure 8: Impedance averaging error versus driver ratio for various loading capacitors.

4 Summary

Measurement methodology for developing a LECCS-I/O model was devised. The power current and power-pin impedances of the IC (74LVC04) measured under various combinations of high-impedance and low-impedance driver ratios and various loading capacitors can be easily modeled as a linear equivalent circuit that combines high-state and low-state circuits. The multi-bit drive LECCS-I/O model could estimate the power impedance under high and low driver loading capacitances within an average error of 1.1 dB up to 500 MHz.

Acknowledgment

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References

[1] J. Levant et al., "Power-Supply Network Modeling," Proc. of EMC COMPO 02, pp 75-78, Nov. 2002

[2] J. Levant et al., "ICEM Modeling of Micro Controller Current Activity", Proc. of EMC COMPO 02, pp. 88-91, Nov. 2002

[3] O. Wada et al., "Power Current Model of Digital IC with Internal Impedance for Power Decoupling Simulation", 4th European Symp. on EMC Proc., Vol.2, pp.315-320, Sep. 2000.

[4] O. Wada et al., "High-Speed Simulation of PCB Emission and Immunity with Frequency-Domain IC/LSI Source Mode", 2003 IEEE Symp. on EMC, Boston, MA, USA, TU-AM-SS1-2, pp. 4-9, August 2003.

[5] Y. Fukumoto et al., "Power Current Model of LSI and Parameter Identification for EMI Simulation of Digital PCBs", IEEE Int'l. Symp. on EMC, pp.1185-1190, August 2001.

[6] Y. Fukumoto et al., "Power Current Model of LSI/IC Containing Equivalent Internal Impedance for EMI Analysis of Digital Circuits," IEICE Trans. Commun., Vol.E84-B, No.11, pp.3041-3049, 2001.

[7] H. Osaka et al., "Power Current Modeling of Load Dependency for EMI Simulation", International Conference on Electronics Packaging (2003 ICEP), Tokyo,TB4-4, pp. 294-298, April 2003.

[8] H. Osaka et al., "Power Current Modeling of IC/LSI with Load Dependency for EMI Simulation", 2003 IEEE Symp. on EMC, Boston, MA, USA, TU-AM-SS1-4, pp. 16-21, August 2003.

[9] H. Osaka et al., "A Linear Equivalent Circuit and a Current Source Model with I/O (LECCS-I/O) for Simulating Multi-bit Drives", EMC COMPO 2004, Angers, France, April 2004.