Three-wire Analysis Model to Predict SI and EMC Effects

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Abstract - Accurate driver and package models are necessary to analyze the signal integrity (SI) and electromagnetic compatibility (EMC) issues on digital circuits. 2-wire models that assume an ideal power distribution system (PDS) are commonly used in modeling the SI of signal lines. This assumption makes real SI and EMC analysis worthless or at least only useful under certain restrictions. In order to account for all current return paths, the power and ground lines have to be considered as well. As such, the driver and the package are modeled as a 3-wire port and a 3-wire network, respectively.
Key words: 3-wire I/O circuits, 3-wire networks, power supply distribution (PDS), Signal Integrity (SI), Electro Magnetic Compatibility (EMC)

1. Introduction

Over the years, 2-wire models have been used in various SI and EMC analysis of digital circuits. These models assume infinite decoupling or an ideal PDS, such that the power line can be regarded as an AC ground. This assumption allows the treatment of the Input/Output (I/O) drivers as 2-wire networks and the signal interconnect between the transmitter and receiver as a 2-port network (e.g., as a single transmission line) referenced to the AC short circuited power and/or ground. To account for the power supply noise, a model is necessary which includes the parasitics on the PDS. In this work, such models are called 3-wire models. Particularly, the associated driver and package models will be called 3-wire driver models and 3-wire package models.
IBIS is the most commonly used 2-wire I/O driver model, which provides the I/O device characteristics through V/I data. A 2-wire driver model assumes an ideal PDS. However, the output waveform of a CMOS circuit is mainly determined by the relation of its input voltage to the power and ground rails. The rail-to-rail switching behavior also emphasizes the importance of including the effect of power supply voltage fluctuations in the driver model. Inversely, with a 3-wire driver model the noise on the power rails due to switching drivers can be examined as well [1]. Using a 2-wire model is obvious for simplicity sake but makes real SI and EMC analysis worthless or at least only useful under certain restrictions.
In order to capture the power supply noise and the correct behavior of the return currents, a package model that incorporates the signal, power, and ground lines is necessary as well. Also, the transition-dependent switching behavior can be observed with such a model.
With this in mind, an IC package evaluation project was started in the framework of MEDEA+ Project MESDIE [2], where it turned out that using the entire circuitry is too complex for any analogue device simulator and using the IBIS models is too simplified for EMC as the signal return current paths are not taken into account properly.
Further analysis has shown that IC package optimization is determined by:

- the measures taken at the silicon die,
- the I/O and supply bond pad allocation,
- the on- or off-chip decoupling (with core and I/O),
- the IC package layer allocation,
- the BGA ball allocation and the PCB layer application with the used decoupling.

2. 3-Wire MODEL

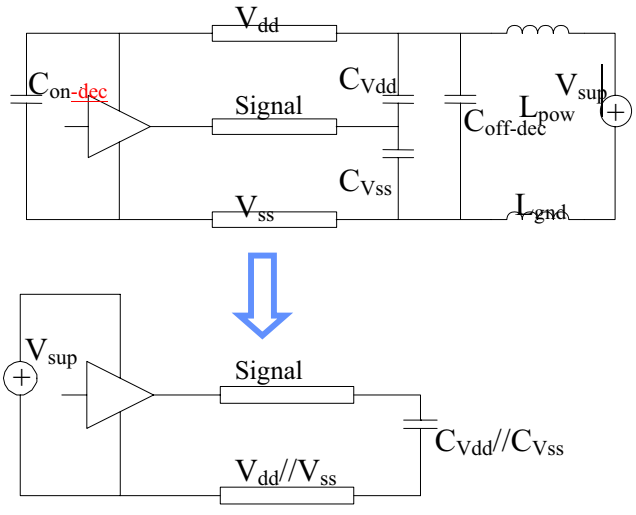

Figure 1 3-wire Model vs. 2-wire Model

In order to analyze the signal transmission in digital circuits, power and ground must be included in addition to the signal line in the interconnect model.
On top of Figure 1, a 3-wire model can be seen. The load is represented by capacitors (C_{Vdd}, C_{Vss}) to power (V_{dd}) and ground (V_{ss}), and the power supply is on the right side of the figure represented by a voltage source (V_{sup}) and parasitic inductances (L_{pow}, L_{gnd}). An arbitrary model is assumed to be available for the interconnect between the driver and the load. If the on-chip and off-chip decoupling capacitors on the driver and load side ($C_{on\text{-}dec}$, $C_{off\text{-}dec}$) provide infinite decoupling, the power line can be seen as an AC ground. Under this assumption, an equivalent 2-wire model can be obtained by parallel connecting the power and ground lines as shown at the bottom of Figure 1. With SI simulations the interconnect network will be reduced even further to asymmetric π- or T-networks. The 2-wire model is not applicable, if there is insufficient decoupling, or if there are many drivers switching simultaneously, such that the PDS cannot be regarded as ideal [3].
The 3-wire output driver circuit can be simply simulated in SPICE using voltage-controlled switches. As such, a three-wire model has been created see Figure 2.

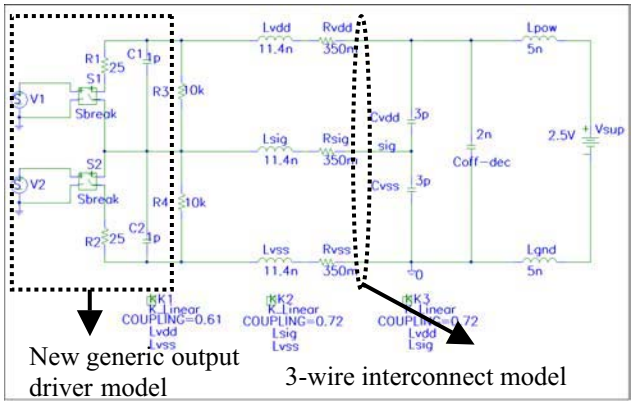

Figure 2 Three-wire models for SI and EMC analysis

The transistors forming the CMOS driver circuit are modeled by resistors (R_1, R_2) representing the on-resistance of the devices and by voltage controlled switches (S_1, S_2) with smooth characteristics. The period and the fall and rise times of the inner circuitry driving the CMOS is applied in the simulation through independent voltage sources (V_1, V_2) connected to these switches. The parasitic capacitance associated with the driver, mainly due to the protection diodes, is represented by two capacitors (C_1, C_2). Some parallel-connected resistors (R_3, R_4) with negligible admittance may represent leakage or DC currents and allow that SPICE can make a DC bias point analysis.
The power, signal, and ground lines are represented by inductors (L_{Vdd}, L_{sig}, L_{Vss}) with mutual coupling coefficients (K_1, K_2, K_3), and resistors (R_{Vdd}, R_{sig}, R_{Vss}). The interconnects modeled here consist of 3 identical coplanar traces in parallel. The distances between the left (V_{dd}) and middle (Signal), and the middle and right (V_{ss}) traces are equal, and the length of each trace is 1 cm. Such a configuration could be found by packages without any power or ground planes. The partial inductance and resistance matrices were calculated at the frequency of the first harmonic of the input signal by using a tool based on the partial equivalent electric circuit (PEEC) method [4]. Such models for the parasitic elements of chip packages are commonly used to simulate simultaneous switching noise (SSN), by including several drivers using the same PDS [5].
The power supply network up to the package is represented by a voltage source (V_{sup}) and parasitic inductances (L_{pow}, L_{gnd}), which are decoupled in the model through an ideal capacitor ($C_{off\text{-}dec}$). Finally, two capacitors to power (C_{Vdd}) and ground (C_{Vss}) represent the system load.

3. Motivation: Comparing the 2-wire and 3-wire models

Using the fact that a 2-wire model assumes an ideal PDS can make a comparison between the 2-wire and 3-wire models. Therefore, a 2-wire model can be obtained by connecting an ideal decoupling capacitor or an ideal voltage source between the power and ground wires of the driver in the 3-wire model. Figure 3 shows the voltage to ground on the load (i.e., voltage drop on C_{Vss}) for the circuit in Figure 2. Obviously, the 2-wire model gives an optimistic result. In case of SSTL 2 interface standard [6], for example, the 2-wire model would not forecast the excessive overshoot of the input voltage on the receiver, which should not exceed 2.8V.

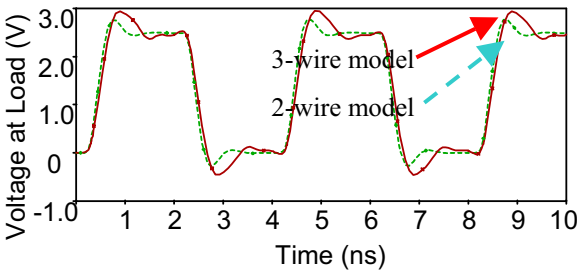

Figure 3 Comparison of the two-wire and three-wire models

The discrepancy between the results can be explained by examining the current loops. Figure 4 shows the main current loops for a low-to-high transition. The CMOS driver pulls the output to V_{dd}. The load capacitance to power (C_{Vdd}) discharges while the load capacitance to ground (C_{Vss}) charges through the off-chip decoupling capacitor. It can be seen that the signal current returns mainly through the power line. Similarly, the return current would flow through the ground line for a high-to-low transition. As stated

earlier, the 2-wire model implies infinite decoupling, so that an ideal decoupling capacitor is assumed to be connected between the power and ground wires of the driver as in Figure 5. As such, for example the L_{Vss} and L_{Vdd} inductances in Figure 2 would be connected in parallel, which is not realistic.

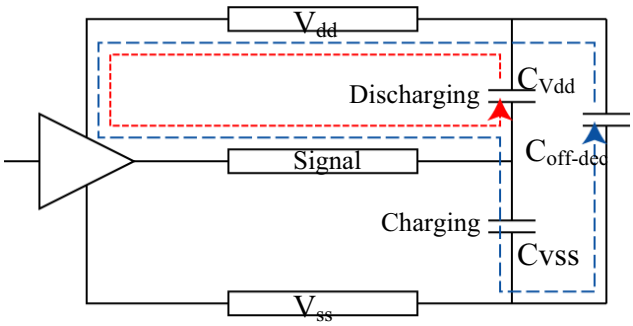

Figure 4 Actual current loops for a high-to-low transition

An on-chip decoupling capacitor would provide additional current loops to the existing ones in Figure 4. In Figure 5, it can be seen that for these current loops, the return currents flow mainly through the ground line. By superimposing the current loops in Figure 4 and Figure 5, the power and ground lines can be regarded as effectively short-circuited, so that the interconnects could be represented by a simplified 2-wire model as in Figure 1.

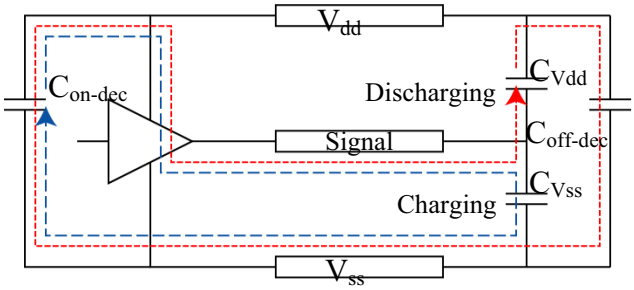

Figure 5 Additional (nonexistent) current loops for a high-to-low transition implied by the 2-wire model

If there is insufficient on-chip decoupling as in the example of Figure 2, the 2-wire model implies nonexistent current return paths. Therefore, the 2-wire model is not applicable in such a case as it can be seen in Figure 3. Furthermore, regardless of the availability of the on-chip decoupling, the package should be modeled as a 3-wire network to capture the correct current return paths, especially in case of unsymmetrical signal-power and signal-ground loops and to be able to calculate the ground bounce between the IC's substrate and the PCB's V_{ss}-layer.

4. Distributed 3-Wire Package Model

Lumped package models as in Figure 2 are only adequate up to certain frequencies. Also, the parasitic elements of the separate segments of the interconnect (e.g., wirebonds, package traces, etc.) are not distinguishable from each other. On the other hand, distributed 2-port package models assume an ideal PDS. To overcome these limitations a new distributed 3-wire package model is proposed as shown in Figure 6.

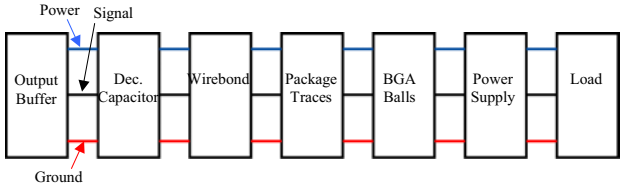

Figure 6 New Distributed 3-Wire Package Model

The three lines between the blocks in Figure 6 represent the power, signal, and ground connections, such that each block can be seen as a 3-wires, considering the output and input. By defining a (virtual) global reference point, the voltage drop along the conductors can be modeled, which is important for EMC considerations. Alternatively, by assigning one of the conductors in the package interconnect as the reference, the package can be seen as a 4-port network. In this case, the considered voltages are always locally referenced, which is suited for SI investigations.

Assuming that there is no electromagnetic coupling between the blocks (i.e., the only coupling is at the ports), each block can be characterized separately. Depending on the design of the package, various blocks can be moved, deleted, or added, such that the influence of each interconnect segment on the signal quality can be easily determined. Also, distributed models can be used for electrically long interconnects with uniform cross sections (e.g., package traces), incorporating power and ground plane models [7].

To capture the nonlinear behavior of the drivers, which can be represented by behavioral or transistor-level models [8], the circuit simulation must be done in the time domain. The equivalent electrical models of the blocks that represent a segment of the interconnect can be extracted through field simulation, measurement, or analytical methods. Cascaded blocks as in Figure 6 can represent the total package. The S- or chain matrix formulation can be applied as an alternative. By multiplying the chain matrices of the blocks, the total interconnect could be represented by a single S- or chain matrix. The implementation of such network matrices in SPICE to make simulations in the time domain is inconvenient, but possible.

The model in Figure 6 assumes that there is negligible coupling to neighboring signal lines. It can easily be extended to include the coupling between the signal lines, by including these lines in the models of the blocks and in port definitions. In case of differential signaling, for example, the total interconnect could be represented by an 4-wire

network. By including neighboring signal lines in the model, crosstalk or SSN investigations can be made.

5. Case Studies

3-wire driver model together with the distributed 3-wire package model were used to investigate the assignment of supply wirebonds in a BGA package with no on-chip decoupling. The package traces were modeled as transmission lines including the power and ground planes [9], and the BGA balls were modeled through optimization of a compact electrical model by matching the full-wave simulation of the structure. The number of the total supply wirebonds was kept constant and equal to the number of signal wirebonds (i.e., S:(G+P) = 1:1). The assignment of the supply wirebonds to power and ground was varied and three cases were investigated:

1. …GSGSGSPS… (i.e., S:G:P = 4:3:1)
2. …PSPSPSGS…. (i.e., S:G:P = 4:1:3)
3. …GSPSGSPS… (i.e., S:G:P = 4:2:2)

Figure 7 shows the voltage to ground at the load for these cases.

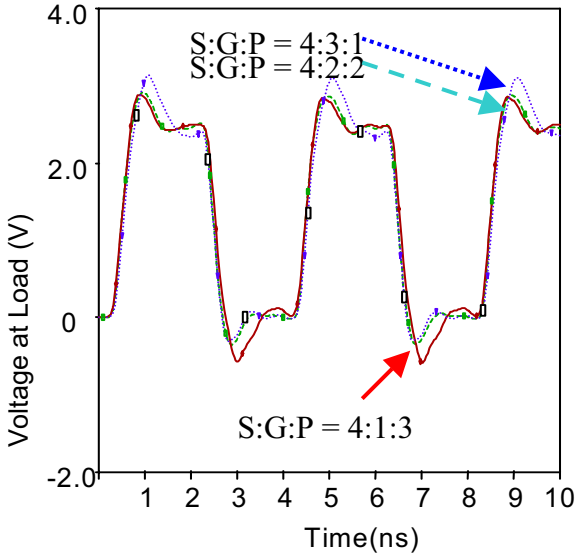

Figure 7 Influence of the assignment of supply wirebonds

As expected from the switching behavior of the CMOS driver in Figure 4, during a low-to-high transition, the signal return current flows mainly through the power line. In this case having low impedance for the signal-power loop (e.g., by providing more power wirebonds) improves the signal quality. Inversely, for a high-to-low transition, mainly the parasitics of the signal-ground loop affects the signal quality. From Figure 7, it can be seen that an optimum voltage behavior is achieved if the supply wirebonds are evenly distributed between power and ground. Even assignment provides the minimum inductance for the supply loop, and an optimum inductance for the signal-power and signal-ground loops.

6. Conclusion

With this new model, all kind of artifacts in either the circuit topology or the geometrical design can be analyzed correctly. By means of changing some lumped element values with the model, the output driver impedance can be modeled for both status transitions. Crowbar current can be taken into account with the 3-wire driver model as well. A distributed 3-wire package model that is introduced in this paper can model power supply perturbations due to package parasitics, and its influence on signal quality i.e. signal integrity. This model is applicable over a broader frequency range than the existing models.

As can be seen from the list of items that do influence package design, the output structure modeling is a dominant factor that thereafter allows a new way of approaching "old" problems. Simultaneously switching drivers with fast edge rates compels the consideration of non-ideal PDS due to the chip package parasitics.

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