Microelectronic EMC System Design for High Density Interconnect and High Frequency Environment

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Abstract: Semiconductor manufacturers continuously provide faster, more cost effective and more highly integrated devices. By the end of the decade, clock frequencies are expected to triple to 3 GHz and design dimensions will have been reduced to 45 nm compared with 130 nm today. Chip area and component density will have increased with edge lengths of 40 mm against the current 20 mm.

Due to continuous miniaturization, higher clock frequencies, faster edge rates and more functionalities on the same area, the EMC problem is causing more and more trouble for semiconductor manufacturers in various application areas, such as automotive, multimedia, telecommunications and computing facilities.

Therefore semiconductor manufacturers and their application customers have to deal with constraints on the chip level to meet electromagnetic compatibility (EMC) requirements of systems and subsystems and are therefore searching for suitable solutions.

In this contribution a coherent approach to overcoming these problems at both chip and high-density packaging levels in the frame of the MEDEA+ project called MESDIE (A509) will be presented.

Key Words: EMC, EME, system design, high density interconnect, high frequency environment, bottom up approach, EMC/EME behavior modeling, conducted emission, parasitic electromagnetic effects, signal integrity, PCB, HDI, HDP.

1. Introduction

Electromagnetic (EM) issues are of increasing use for IC designers, application engineers and product developers in analysis, simulation and modelling. By choosing the adequate and correct analysis, simulation and modelling methodologies the products developed for different kind of applications (automotive, telecommunication, consumer, ...) can be supported in terms of EMC efficiently. Only with a combined electromagnetic and circuit-analysis it will be possible to have an overall reliability of the system. Therefore the electrical interconnects and package, the printed circuit board respectively the circuit carried and the subsystem/PCB interconnect structure have to be taken into account.

The use of high-frequency EM modelling is an emerging area, as defined in the 2001 International Technology Roadmap for Semiconductors (ITRS) and the MEDEA+ EDA Roadmap [www.medea.org]. Both roadmaps state that the need for high-frequency analysis, simulation and modelling on chip, package and subsystem level will increase through 2007.

The following technology driving forces reinforce this development (higher processing speed/higher memory capacity/lower power consumption/logic voltage < 1.2 V/lithography 0.05 µm in 2010/ embedded SRAM/DRAM - 16 MB/256 MB/integrated packages and modules/clock frequency up to 10 GHz - see ITRS - and transfer rate up to 40 Gbit/s).

The growing influence of parasitic effects is not only dependent on the trend on the processor market which gets obvious in the following table.

Parameter	2002	2010	Factor
Density	350Mbit/cm²	20-40 Gbit/ cm²	80
Clock Frequency	0.1-0.4 GHz	1-1.5 GHz	4
Data Rate	0.1-0.8 Gbit/s	8-12 Gbit/s	12

Table 1: Development of memory parameters up to 2010 (source: Samsung 2002)

The circuit and system design process has become increasing by difficult due to the sharp increase in the number of radiating elements on printed circuit boards and system level; mainly due to the increase clock frequencies and chip complexity. To be able to counter the interference created by chip and other radiating elements (PCB, sub system, ...) a good prediction of the electromagnetic field strengths is required. The prediction has to be performed for a large number of complex IC and has to include the interaction with the complex structure of the IC application. Secondly it is required that the prediction of electromagnetic fields can be performed sufficiently fast to be used in the early design phases of a microelectronic system. Other examples of parasitic effects are V_{cc} and GND noise (VGN). VGN has become one of the major concerns in the present-day digital systems due to the mentioned fast edge rates, high clock frequencies, and low voltage levels. Modelling is an important feature which brings together the semiconductor manufacturers, systems houses and R&D institutes with different backgrounds in technology and design methodologies to develop a common strategy on handling radio-frequency, EMC and susceptibility issues (EMC/RF/SI) – see Figure 1 and 4.

2. State of the Art

In the past different activities to improve the SI/EMC/RF behavior on the system level have been conducted. However, the focus has been almost exclusively put on measurement based methods and additional tools for the design of printed circuit boards. In this way, a lot of especially adjusted solutions on printed circuit board and system level have been implemented successfully.

In consequence of the described rapid developments in the semiconductor level concerning increasing clock frequencies, increased signal rise and fall times and smaller dimensions as well as the continuously accelerating miniaturization and complexity of systems, the SI/EMC/RF parasitics can no longer be regarded separately concerning chip and high density packaging. It is therefore of major importance to combine the different SI/EMC/RF-experiences of chip and HDP designers.

Thus new methods for the creation of a SI/EMC/RF-compatible design of microelectronic systems have to be developed – see Figure 1. They have to integrate incipient with the chip also the package respectively high-density design level. In addition, the implementation of the developed methods and procedures in tools respectively design processes is mandatory to guarantee a fast and efficient design process.

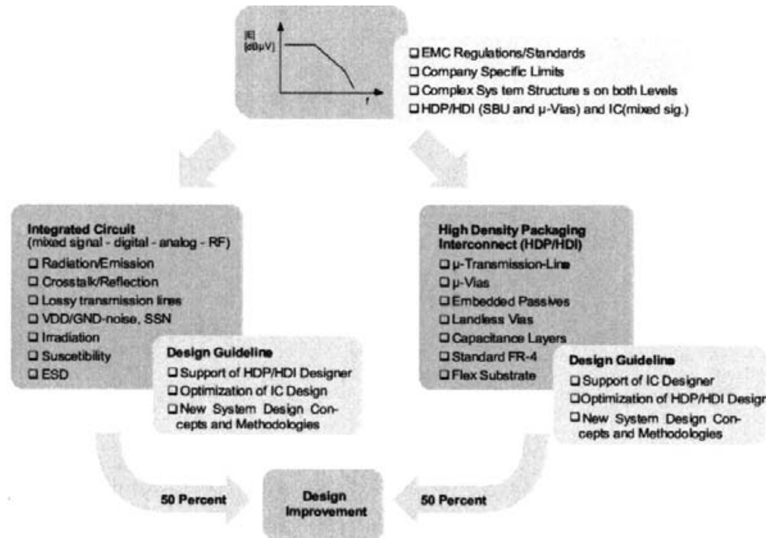

Figure 1: Parallel treatment of on chip and off chip parasitic effects (EMC/RF/SI) into the design process and concept of design improvement (source: MESDIE A 509)

Due to the contrary effects - higher switching currents versus demand for reduced emission - the semiconductor industry is challenged for research in on-silicon design measures for EMC improvement. This topic is especially critical in the area of CMOS devices like micro controllers. One important topic for the near future will be the investigation of the VGN behaviour of the combining power ground system of BGA mounted on a PCB (cost effective application in the automotive area).

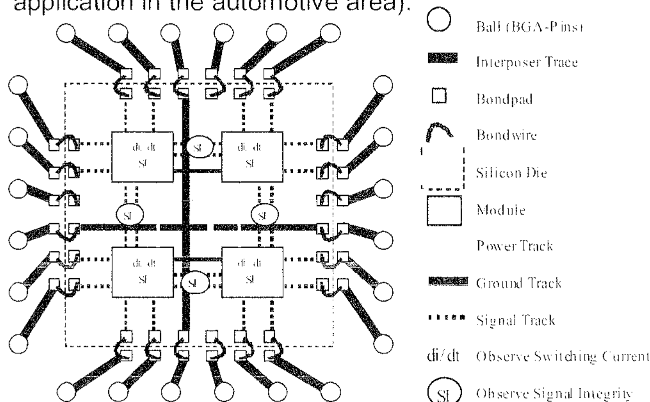

Figure 2: Hierarchical EMC/RF/SI system for BGA design (source: MESDIE A 509 – IFX)

In the case of a complex BGA interposer (small multi-layer HDI/HDP), this model becomes very complex, and abstraction methods need to be developed [5].

3. Application of IC in Complex System Environments

The knowledge available on electromagnetic compatibility, on modeling and simulation of package concerning EME is today one critical factor, the modeling and simulation package concerns EME (❶ in Figure 3). Other topics like susceptibility and ESD must not be neglected because they are EMC effects of increasing severity, especially with low-voltage designs (❷ in Figure 3).

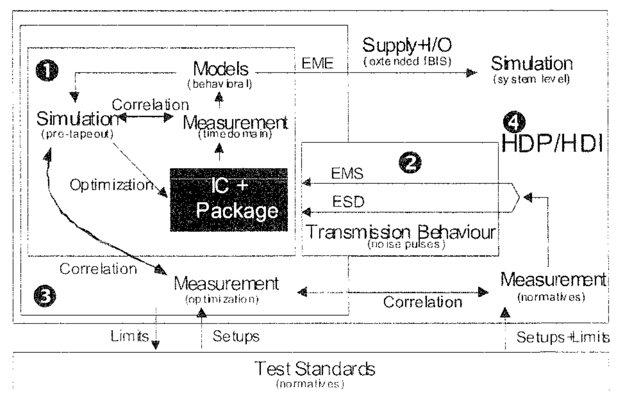

Figure 3: Working Areas of EMC modeling and simulation of on chip and off chip level (source: MESDIE A 509 – IFX)

Modeling and simulation tasks on chip level require reliable measurement techniques to verify and correlate the results and thus optimize the models

and simulation algorithms. Measurement can be done directly by on-chip sensors (silicon view at any on-chip location). Additionally, standardized IC test setups will be used to measure emission effects at the chip boundary (❸ in Figure 3). Both levels of measurements are required to verify on-chip and package EMC models. In the case of susceptibility, the impact of system-induced noise (electric fields, burst/surge pulses) via the HDP/HDI package and on chip have to be analyzed. In case of emission, we have already sufficient knowledge to start with modeling and simulation working areas. Not only the bare silicon die has to be considered, but also the package and the HDP/HDI level (❹ in Figure 3).

3.1 EMC/EME Behavior Models and Bottom Up Modeling Methodology

Due to the switching gates of VLSI IC a so called dynamic current occurs on the power ground system (PGS). The generated RF energy can not be radiated directly from the PGS (due to small geometric dimensions). The occurring noise signals will be rather transmitted via the package interconnects (conducted emission) to the IC environment (PCB, cabling, ...). The dynamic current can be used a value to characterize the conducted RF energy of complex digital systems. The related emission can be reduced noticeable by reducing the dynamic current. This can be done by investigation of emission issues during the IC design process (Figure 4). Based on the introduced bottom up approach [6] behaviour models of single gates will be developed and parameterised. For the utilization of an EMC simulation of the whole complex IC an integration of the EMC/EME models into a set libraries is required. Figure 5 shows the simulation results using the behaviour modelling approach compared to simulation on transistor level. The used analytical model (behavioural model) describes more then 180 parallel switching and cascaded logical circuits (for more details see [6]).

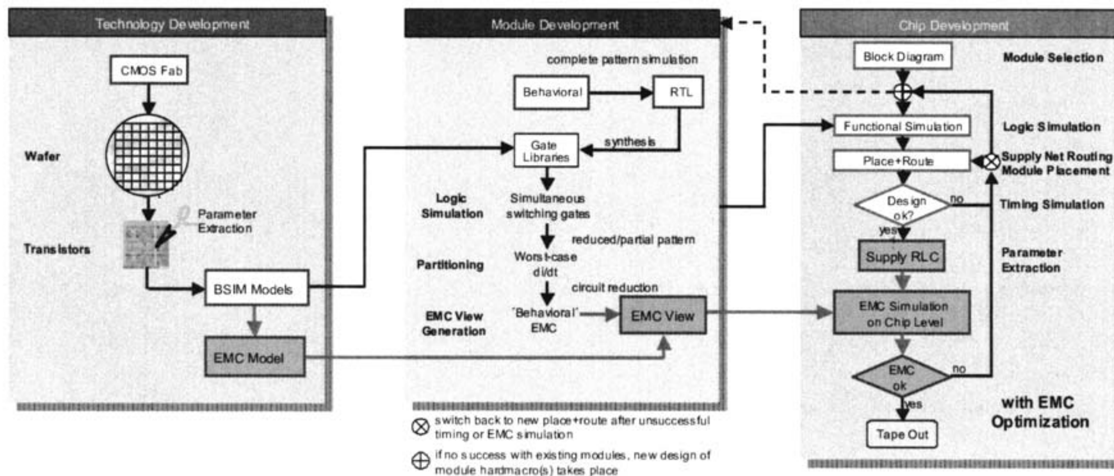

Figure 4: Bottom Up Approach/EMC/EME Behaviour Models (source: MESDIE A509 – Infineon Technologies AG)

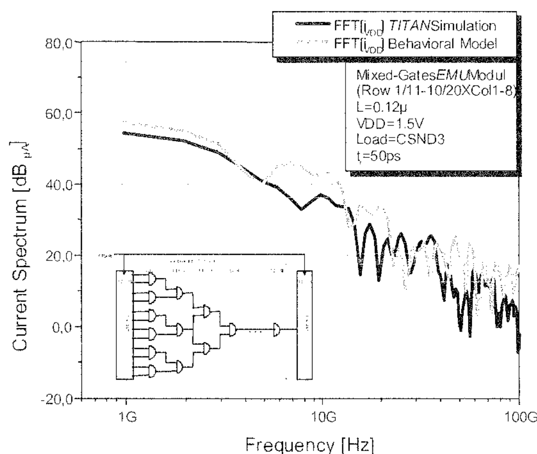

Figure 5: Comparison of simulation on behaviour and transistor level

4. Improved Design Methodology on HDI/HDP Level

Top level parasitic simulation will enable the HDI/HDP designers to avoid redesigns due to undesired parasitic behavior. EMC-relevant data have to be provided for system designers by means of e.g. enhanced IBIS or ICEM models [4]. Not only signal integrity, but parasitic noise information on supply pins and signal pins as well can then be considered in HDP/HDI-level simulations.

The following figure depict the complexity of the task to get to an efficient design-methodology for off chip applications (HDI/HDP). The existing experiences reveal that the models, design-rules and add on tools (routing, floor planning, post and pre-layout analysis) have to be considered on all design phases.

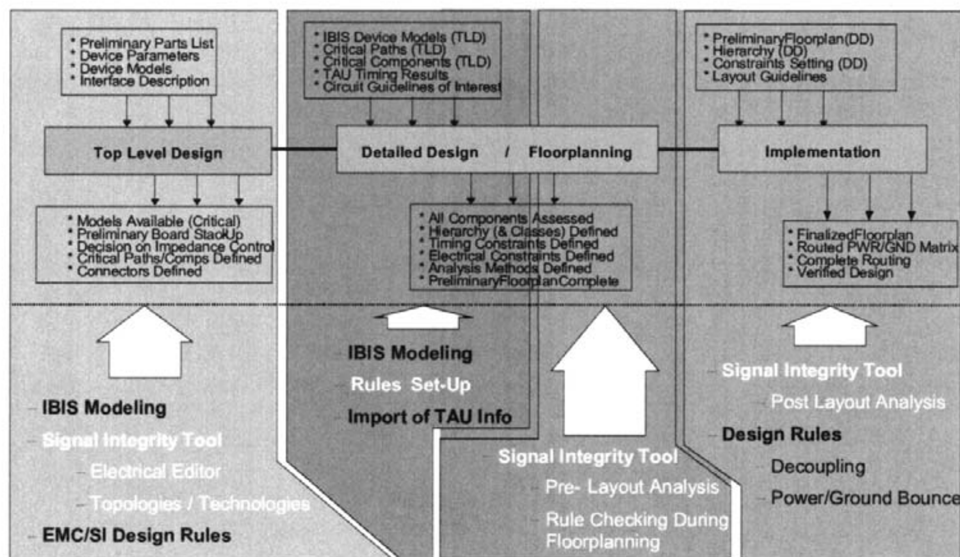

Figure 6: Design complexity on HDI/HDP level (source: MESDIE A509 – ALCATEL SEL AG)

One part of the intended synergy effect in the MESDIE project can be achieved by a parallel treatment of the parasitic effects on chip and off chip level (see Figure 1).

5. Conclusion

Based on the hitherto achieved results in MESDIE it is possible for the first time to realize EMC simulations and the related analysis in acceptably time and with acceptably data volume as well as case studies during the design phase.

Due to increased clock speed and transfer rates in the entire microelectronics arises an increasing demand for efficient treatment of parasitic effects in the complete design process of microelectronic systems. In the future, there will exist no distinction between time and frequency response (f_B *up to 110 GHz*). I.e. digital, analogue design and RF design will grow together. The parasitic effects have to be accounted for all along the design flow, starting from the early design stages, while refining the modeling and the simulation accuracy.

EMC in microelectronic systems is a killing factor. Every system has to work under every condition fail save. An intelligent EMC management of microelectronic systems in every application based on new concepts will be a key competition factor in the future.

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REMARK: A more detailed paper can be found on the MESDIE web sites (http://www.mesdie.org).