A NOVEL BEAMFORMING TECHNIQUE USING DOA ESTIMATION AND ITS HARDWARE IMPLEMENTATION

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1 Introduction

When a smart antenna beamforming system based on the DOAs (Directions of Arrival) of incident signals as the spatial channel information is considered, a beamforming technique with low complexity will be desirable for practical use. We have studied the implementation of fast DOA estimator with dedicated circuit of FPGAs (Field Programmable Gate Arrays) and proposed a simple and stable beamforming technique with a low-sidelobe beampattern of the Dolph-Chebyshev (DC) tapering window [1, 2]. It has extremely low complexity and is suitable for implementation on high-speed logic devices such as FPGAs. High-speed weight adaptation capability due to its low complexity may be extremely useful for applications in various wireless communication systems. In this paper, the hardware implementation of proposed beamformer will be described. The computer simulation and some experimental results of the performance evaluation in a radio anechoic chamber will be presented.

2 Null Steering Beamformer with Notch Beams

The proposed technique basically steers the mainlobe toward the estimated user direction and completely suppresses the interferers by low sidelobe with the Dolph-Chebyshev beampattern. The low-sidelobe beamformer has the significant advantage of low complexity without huge computation load in optimum techniques, such as ZF (zero forcing) and DCMP (directional constrained minimizing power) for explicitly nullifying interferences. However, if certain interferers exist within the broad mainlobe area (*in-beam*), the performance will be considerably degraded because of unavoidable interference reception. In this system, the interferers within the mainlobe can be canceled out by optional null-steering processing with a notch beampattern. The final beamforming weight is computed by simple convolution operations of pre-computed Dolph-Chebyshev beam and optional canceling beams of notch beams; hence, the computation load for weight generation is very small.

The cascade beamformer of a low-sidelobe DC beam and optional canceling beams was proposed in order to overcome this; this is termed Null-steering Dolph-Chebyshev Beamformer (NDC-BF) [2]. In NDC-BF, the beamformer adaptively performs beamforming for user signal and nullsteering only for the in-beam interferers with independent nulls as

$$\boldsymbol{w}_{\text{null}}^{H}\hat{\boldsymbol{v}}_l = 0, \tag{1}$$

and $\bar{\boldsymbol{w}}_{\text{beam}}$ is a low-sidelobe beam determined by Dolph-Chebyshev tapering window $\boldsymbol{C}_{DC}$, denoted by

$$\bar{\boldsymbol{w}}_{\text{beam}} = \boldsymbol{C}_{DC} \odot \hat{\boldsymbol{v}}_0, \tag{2}$$

where $\hat{\boldsymbol{v}}_0$ and $\hat{\boldsymbol{v}}_l$ are the estimated spatial signature vectors of user and interferers, respectively, by DOA estimation pre-processing. And $\odot$ denotes convolution operator. Regarding digital

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signal processing, the total beamforming weight can be computed immediately by element space convolution instead of physically cascaded structure [3] as

$$\boldsymbol{w}_{\text{NDC-BF}}^{T} = \bar{\boldsymbol{w}}_{\text{beam}}^{T} * \boldsymbol{w}_{\text{null}}^{T}, \tag{3}$$

where * denotes convolution operation and $\bar{\boldsymbol{w}}_{\text{beam}} \in \mathbb{C}^{(M-l)\times 1}$, $\boldsymbol{w}_{\text{null}} \in \mathbb{C}^{2\times 1}$. The notch beam to nulling the power in the direction θ_{null} is computed as

$$\boldsymbol{w}_{\text{null}} = \left[1, e^{-j\pi \sin\phi}\right]^{T}, \tag{4}$$

where

$$\phi = \begin{cases} \sin^{-1}\left[1 - \sin\theta_{\text{null}}\right] & 0 \le \theta_{\text{null}} < \pi/2 \\ -\sin^{-1}\left[1 + \sin\theta_{\text{null}}\right] & -\pi/2 \le \theta_{\text{null}} < 0 \end{cases}. \tag{5}$$

Moreover, in generalized version of the cascade structure for the M-element array comprising the beamforming stage and $l(< M-1)$ optional post null-steering stages with notch beams, the weight vector can be extended by

$$\boldsymbol{w}_{\text{NDC-BF}}^{T} = \bar{\boldsymbol{w}}_{\text{beam}}^{T} * \boldsymbol{w}_{\text{null,1}}^{T} * \cdots * \boldsymbol{w}_{\text{null,l}}^{T}. \tag{6}$$

Assuming there are no in-beam interferers without an optional null-steering stage, the proposed NDC-BF will have the same function as the DC-BF. However, the SINR performance in a small source separation condition will be dramatically improved. The optional null-steering stage was applied only when the source separation is below 25° (in-beam area) in 8-element array because the interference suppression by the low sidelobe has slightly better SINR characteristics than the optional null-steering process of the in-beam area.

The computation complexity, involved in NDC-BF is greatly low than that of the other optimum beamformers. Table 1 presents the computational complexity for the K-element ULA antenna in the presence of L sources. Figure 1 shows the comparison between the computational complexity in the cases of 8 antenna elements, where no operations are required for NDC-BF in the presence of the desired signal only because it refers to the precomputed beampattern for the desired signal in the ROM (Read Only Memory). It is clarified that the proposed NDC-BF has extremely low complexity.

3 Hardware Implementation

The significant feature of NDC-BF is low complexity without a huge computation load in the case of optimum techniques, such as ZF and DCMP, for explicitly nulling interferences although the SINR performance is not optimum. In the computation flow of this system, we can place nulls at desired locations by simple operations; thus, the interferers within the mainlobe can be canceled by optional null-steering processing with notch beams, which are pre-computed and stored in the ROM in the FPGA's embedded memory block. The final beamforming weight is computed by the simple convolution operation of the pre-computed DC beam and optional canceling beams; hence, the computation load for weight generation is very small.

In the case of the single null, this operation requires only two scalar multiplications and one vector addition. Therefore, fast weight generation can be realized without additional complexity. The block diagram for NDC-BF on FPGA is shown in Fig.2. The DC beams and notch beams are pre-computed and stored in the ROM. According to the DOA estimation results in preprocessing, the simple convolution operation of the pre-computed weights can be performed easily. NDC-BF consists of ROMs for the pre-computed beams, two-tap complex FIR filter for convolution operation, and complex multipliers for beamforming. The precision of the DC beams and notch beams were appropriately chosen as 12 and 8 bits, respectively.

According to the FPGA implementation results, approximately 30,000 logic gates were used and 83,160 memory bits were required. Beamforming is computed extremely fast in parallel using 16 MACs. The associated time for weight generation and beamforming is, for example, approximately 1.4μs, assuming that the information frame length N_{frame} is 136 in the three-null case.

4 Measurement Results

The BER (bit-error-rate) criteria is experimentally evaluated in order to verify the integrated system performance. In this study, the DOAs were estimated by the developed DOA estimator [1, 2]. It was assumed that the number of sources is already to be 4-one is the desired signal (0°) and the others are the interferers (−40, −20, 15°) with INR (Interferer to Noise Ratio) of 9 dB. The optional null steering processes were applied to the interferences coming from −20 and 15°. In the measurement, the data vectors were obtained by combining each data vector with a single source, and the SNR was converted for the combined version of the data vector.

The mutual coupling and receiver characteristics usually have harmful effects on the DOA estimation and beamforming performance. In the presence of mutual coupling and receiver characteristics of a practical system, the pattern nulls do not have sufficient depth and are deviated from the desired locations. The shallow nulls result in the reception of unintentional interference power; hence, the quality of the desired signal will be typically degraded. In this measurement, the antenna array was calibrated well by eliminating the mutual coupling effect. Figure 3 presents the DOA estimation results by fixed-point processor as a pre-processor [1], where SNR means user signal power ratio and those of interferences were 9 dB. The DOA estimation performance was limited by dynamic range of the fixed-point processor and noise level. Figure 4 shows the BER performance in various cases. It is clear that the performance of proposed NDC-BF is comparable to the optimum technique of ZF under the BER criteria, but the computation load is extremely low. It can also be seen that the DOA estimation errors lead to an increase in BER under the condition of low SNR.

5 Summary

This paper presented the hardware implementation of proposed beamformer. The improvement of computation complexity was also discussed. The experimental results of the performance evaluation in a radio anechoic chamber with the integrated system of the DOA estimator and NDC-BF on the developed testbed system. It is clarified that The BER performance of the proposed beamformer in a practical case was comparable to the optimum technique of ZF with greatly low complexity.

References

[1] M. Kim, K. Ichige and H. Arai, "Implementation of FPGA based Fast Unitary MUSIC DOA Estimator," *IEICE Trans. Electron.*, Vol. E87-C, no. 9, pp. 1485–1494, Sept. 2004.

[2] M. Kim, K. Ichige and H. Arai, "Real-time Smart Antenna System Incorporating FPGA-based Fast DOA Estimator," in Proc. *2004 IEEE Vehicular Technology Conference*, Los Angeles, CA, US, Sept. 2004.

[3] T. Asai, S. Tomisato and T. Matsumoto, "Field test results for a beam and null simultaneous steering S/T-equalizer in broadband mobile communication environments," *IEICE Trans. Commun.*, vol. E84-B, no. 7, pp. 1760–1767, July 2001.

Table 1: Computational load for weight computation in real operations (K elements, L sources).

	Multiplications	Additions	Total operations
NDC-BF (single null)	$8(K-1)$	$2K$	$10K-8$
NDC-BF (two nulls)	$12(K-2)+4$	$4K+2$	$16K-18$
NDC-BF (three nulls)	$16(K-3)+12$	$6K+6$	$22K-30$
DCMP	$\frac{4}{3}K^3+4K^2$	$\frac{4}{3}K^3+4K^2$	$\frac{8}{3}K^3+8K^2$
ZF	$8L^2K+4L^3$	$8L^2K+4L^3$	$16L^2K+8L^3$

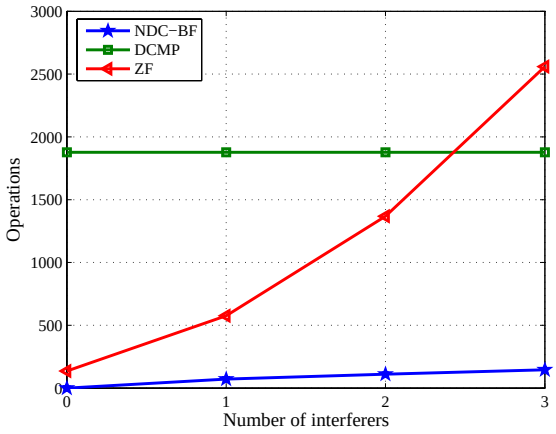

Figure 1: Computation load ($K=8$ elements).

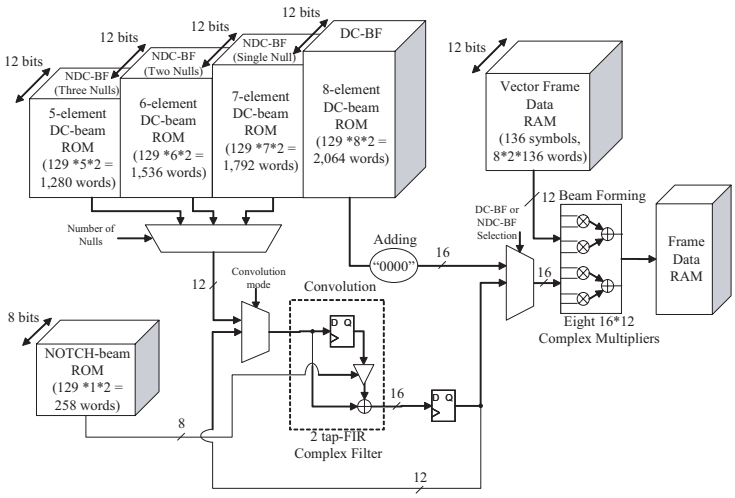

Figure 2: Processing block diagram in FPGA.

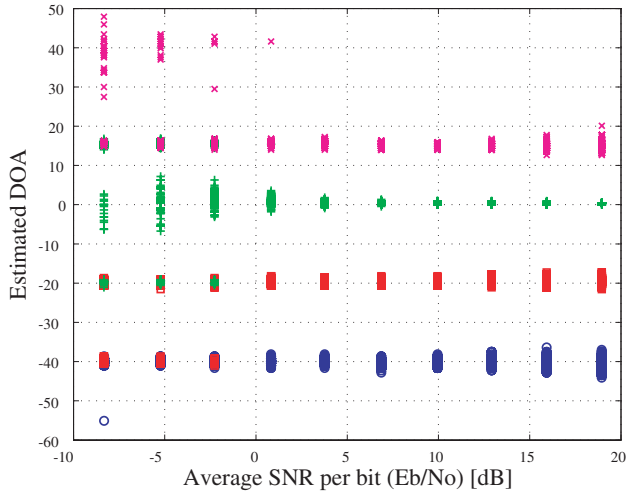

Figure 3: DOA estimation results (100 trial per given SNR).

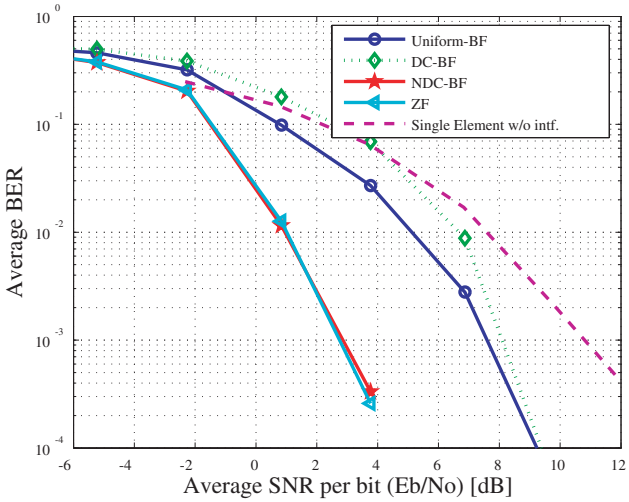

Figure 4: Beamforming results (BER).