APPLEBAUM-HOWELLS ARRAY WITH SYSTOLIC ARRAY ARCHITECTURE

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Introduction

The recent sophisticated very large-scale integration (VLSI) technology has been leading to a new concept in adaptive array antennas, known as the digital beamformer (DBF) concept. While there are various configurations for the DBF processor, DBF processors having the systolic array architecture[1], which is regularly structured, are considered as the most suitable approach to implementing the processors using VLSI technology. This paper introduces a new systolic array architecture for the Applebaum-Howells array. The proposed architecture employs the preprocessor technique[2]; the overall array consists of a preprocessor and an Applebaum-Howells processor. Assuming that the Gram-Schmidt processor[3] is used as the preprocessor, it will be shown that the orthogonality among the Gram-Schmidt processor outputs can remove the global feedback loop in the conventional Applebaum-Howells processor, and that the Applebaum-Howells array can be efficiently implemented by using the systolic array.

Applebaum-Howells Array with Preprocessor

A generic configuration for the Applebaum-Howells array with the Gram-Schmidt processor as the preprocessor is shown in Fig.1(a). The Gram-Schmidt processor transforms the original signal from the array elements u (=t)into a new set of signals v ($=t_N$), which is the input signal to the Applebaum-Howells processor. As shown in Fig.1(a), the Gram-Schmidt processor consists of N-1 rows of unit processors (cells), which are single loop LMS processors, in the form of a triangle[3]. A particular feature in the output from the Gram-Schmidt processor v is of the orthogonality, i.e.,

$$E[v_j^*(t)v_k(t)] = \delta_{jk}. \quad (E[\ ]: \text{the expected value}) \qquad (1)$$

The Applebaum-Howells array operates using the transformed array element signal v ($=t_N$) as its input signal. The differential equation for the j-th array weight x_j is then given by the following equation, assuming that the loop gain is sufficiently large[2]:

$$\frac{T}{G}\frac{dx_j(t)}{dt} + v_j^*(t)h_N(t) = s_{vj}, \qquad (2)$$

where T and G are the time constant and gain for the loop, respectively, and s_{vj} is the j-th component of the transformed steering signal s_v associated with the signal v; $h_N(t)$ is the (final) array output from the Applebaum-Howells processor and a special case with j=N for the partial sum of the array output $h_j(t)$ defined by

$$h_j(t) = \sum_{k=1}^{j} v_k(t)x_k(t), \qquad (3)$$

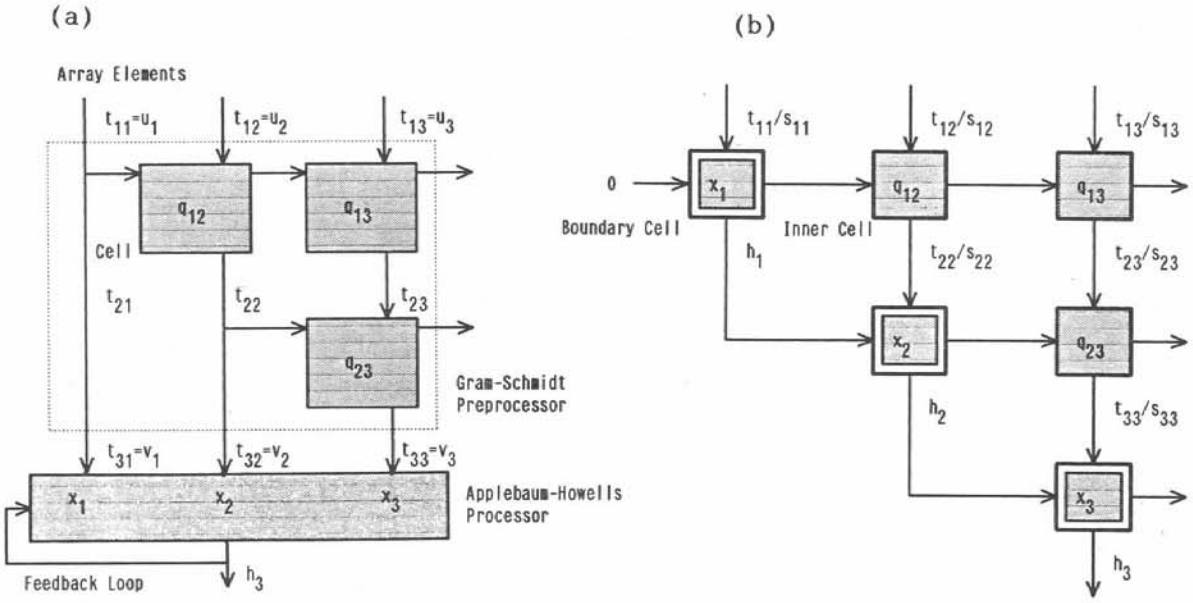

Fig.1. (a)Applebaum-Howells array with Gram-Schmidt preprocessor, (b)Its systolic array architecture.

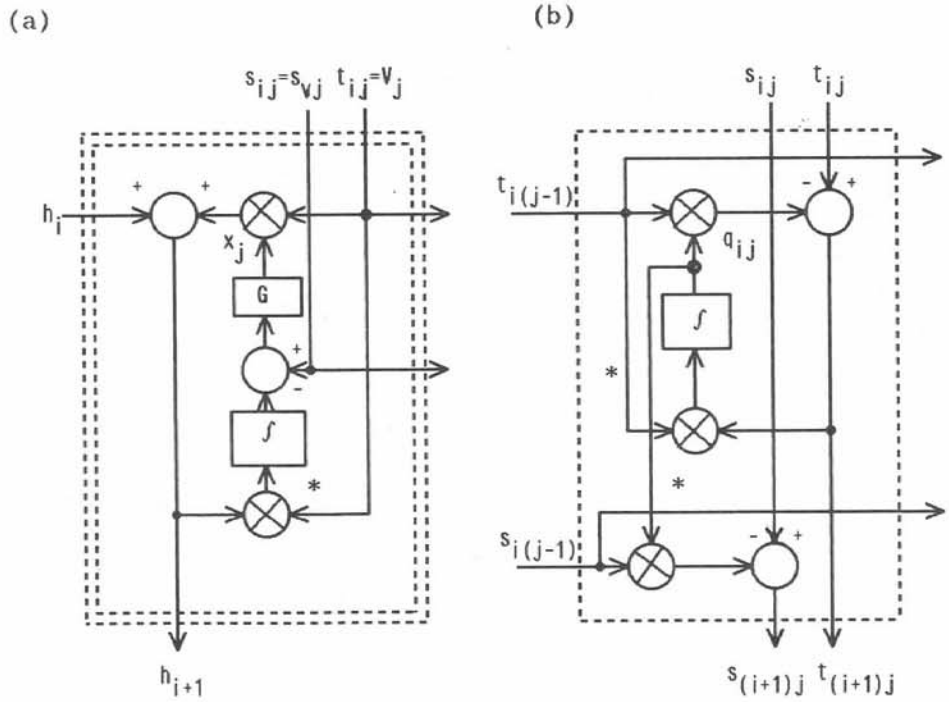

Fig.2. (a)Boundary cell with weight x_j, (b)Inner cell with transform coefficient q_{ij}.

In (2), the second part on the left-hand side represents the correlation operation of the input signal and the array output defined by (3). This operation requires an Applebaum-Howells processor to have a global feedback loop for the array output. This feedback configuration prevents the Applebaum-Howells processor from the systolic array implementation.

Systolic Array Implementation of Applebaum-Howells Array

An essential factor in the configuration of Applebaum-Howells array (processor) with systolic array architecture is to remove the global feedback loop from the input signal and array output correlation calculation. The correlation calculation can be mapped into the systolic array configuration, as follows: The correlation operation can be written in the form (in the sense of the expected value):

$$v_j^*(t)h_N(t) = v_j^*(t)\sum_{k=1}^{N} v_k(t)x_k(t) = v_j^*(t)v_j(t)x_j(t), \qquad (4)$$

because of the orthogonality among the Gram-Schmidt processor outputs defined in (1). Equation (4) shows that the correlation for the j-th weight x_j can be obtained by using only the j-th input v_j, instead of using both array output h_N and the j-th input. Therefore, the circuit for the correlation calculation requires no global feedback loop for the array output. As a result, the correlation calculation can be localized and can be implemented by employing a systolic array configuration.

Furthermore, as shown later, the following relation is useful for the systolic array implementation of the Applebaum-Howells array to make the configuration simpler and more efficient: Equation (4) can be also written in the form:

$$v_j^*(t)h_N(t) = v_j^*(t)h_j(t) \qquad (5)$$

Applying the above discussion to (3) results in the following equation for the j-th array weight x_j:

$$\frac{T}{G}\frac{dx_j(t)}{dt} + v_j^*(t)h_j(t) = s_{vj} \qquad (6)$$

The overall structure of the systolic array for the Applebaum-Howels array is depicted in Fig.1(b). The inner cells, as shown in Fig.2(b), transform both the array element signals and the associated steering signal, Note that the coefficient for the steering signal transform in each inner cell can be obtained by copying that for the array element signal transform in the same cell. No circuit is necessary to produce the transform coefficients for the steering signals.

The boundary cells in Fig.1(b) form the Applebaum-Howells processor; the configuration for the boundary cells, which realizes processing in (6), is presented in Fig.2(a). The boundary cell is a single loop Applebaum-Howells processor, having an additional circuit, to obtain the partial sum of the array output defined by (3); the final array output is thus obtained as the output of the boundary cell in the bottom. As shown in Fig.2(a), the correlation calculation can be accomplished between the j-th input v_j and the partial sum of array output h_j, exploiting the relation represented by (5). This makes the resulting systolic array architecture for the Applebaum-Howells array simpler and more regular.

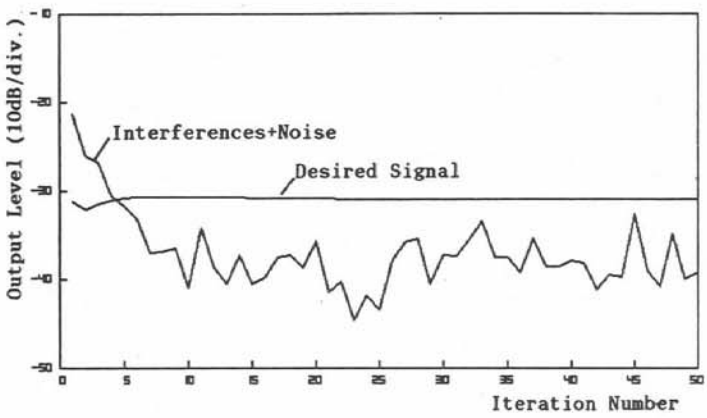

Fig.3. Transient Performance. (N=16, 2 Interferences; SINR=-3dB, INR=35dB)

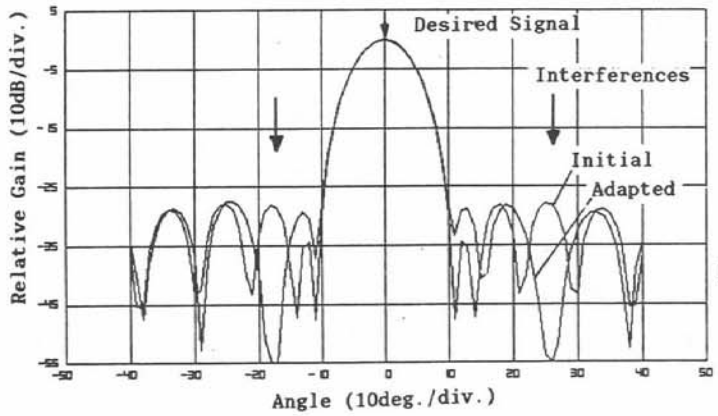

Fig.4. Radiation Patterns of Initial and Adapted. (Interation number=50 for Adapted Pattern)

Performance

Figures 3 and 4 represent the transient performance and the associated radiation patterns, respectively, for the proposed Applebaum-Howells array. In those figures, a linear array is used with 16 array elements and half wavelength element spacing. The effect of two equal power interference signals received individually at levels of 35 dB relative to the thermal noise floor at the array elemets is modeled. The model also incorporated a desired signal at a -3dB level. As shown in Fig.3, a good interference cancellation level is obtained, maintaining the level at the disired signal constant. The resulting radiation pattern, in Fig.4, shows nulls in the interference directions.

Conclusion

A systolic array architecture for the Applebaum-Howells array has been presented. The proposed architecture employed the preprocessor technique. The Gram-Schmidt processor was used as the preprocessor. It has been shown that the orthogonality in the Gram-Schmidt processor output signals can eliminate the global signal feedback loop for the Applebaum-Howells array and that the Applebaum-Howells array can be effectively implemented by using the systolic array architecture. Regarding the importance of the Applebaum-Howells array in the adaptive array field, it is concluded that the result obtained in this paper has derived a significant solution for the systolic array implementation problem for the adaptive array.

References

[1] S.Y.Kung, VLSI Array Processor, Prentice-Holl, 1987
[2] S.P.Applebaum,"Adaptive Array," IEEE Trans. Antennas Propagat., vol.AP-24, no.5, pp.585-598, September 1976.
[3] R.A.Monzingo and T.W.Miller, Introduction to Adaptive Array, Wiley-Interscience, N.Y,, 1980.