Modeling and Simulation of Conducted Emission for VLSI ICs

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Abstract: Increasing demands on electromagnetic compatibility of electronic products - especially the demands on reduced emissions of microelectronic components in combination with higher complexity of electrical circuits - require development of new circuit conception techniques. Due to postulation of decreased design cycles, this can only be achieved by EMC-relevant simulations during the design phase. On the basis of the enormous complexity of digital ICs (millions of transistors on a single unit), it is essential to develop EMC/EMI - models of single components, modules as well as of whole CMOS-VLSI-ICs (ASICs, microcontrollers, DSPs, etc.).
This article presents a modeling methodology based on a bottom-up approach which allows EMC and emission analyses of whole VLSI-ICs during the design phase.
Key words: EMC, EMI, Microcontrollers, Switching Current, BSIM, Behavioral Models, On Chip Current Measurements.

1. Introduction

It is well known that dynamic switching currents, which are generated by active switching components, are an essential cause for conducted emissions upon a chip. Basic concepts and guidelines for EMC design are available nowadays but product specifications often eliminate the possibility of predicting the physical EMI behavior of silicon chips. In consideration of EMC redesigns as well as development and production of presently necessary test chips, EMC and EMI models have to be issued for the purpose of an EMC simulation. Therefore, behaviors models have to be delivered that describe the real EMI phenomena of such complex systems [2], [3]. This paper presents a bottom-up approach for generation of EMC/EMI behavior models with special focus on conducted emission.

2. Bottom-Up EMC Modeling Methodology

For characterization the conducted emission, firstly the dynamic switching current has to be modeled. It is certainly possible to perform circuit simulations of individual gates but an evaluation of millions of transistors is admittedly not possible in an adequate extend. Thus, it is necessary to initially develop an analytical description of the dynamic switching current. For the purpose of a future integration into the design process and for the incorporation of technology-dependant parameters, the mathematical behavior model is based on BSIM3v3 transistor models [4].
Figure 1 shows a bottom-up methodology which implements first EMC models of simple individual gates. With respect to circuit topology and circuit times, whereby a continual statistic evaluation is an important premise, behavior models of individual modules (e.g. clock units) which are based on simple gate models, can be generated in a second step. For future EMC simulations of the whole chip, it is necessary to integrate the EMC/EMI models into libraries. In combination with the parasitic elements of the wiring system (RC and L), it will be possible to perform an EMC/EMI simulation of the whole chip.

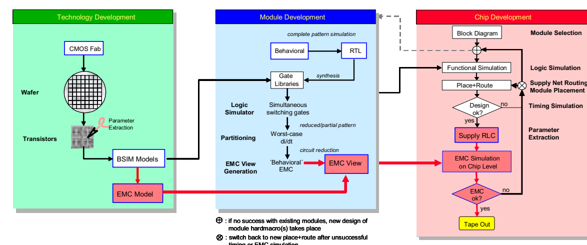

Figure 1: Bottom-up approach for generation of EMC/EMI behavior models of complex ICs

3. Behavior Modeling

The switching gates of VLSI ICs generate dynamic currents which again produce high-frequent voltages on supply lines. Due to the small dimensions of the chip, these interferences cannot be emitted directly but are conducted to peripheral elements via package interconnects. Therefore the generated dynamic current is proportional to the RF energy and can be considered as a measure for conducted emission of complex digital systems.
If a reduction of dynamic currents is possible while the product specifications are adhered to, less emission of the chip can be achieved. But the aim of decreased emission is bound to an implementation of emission aspects into the design process.

For future integration into the IC-design flow, the described behavior models are based on technology-dependant BSIM3v3 transistor descriptions. The bottom-up approach initially creates behavior models of single gates [3]. The next step comprises expansion of these analytical models with local parasitic elements of the supply system. The extraction of these RLC-elements is described in the next chapter.

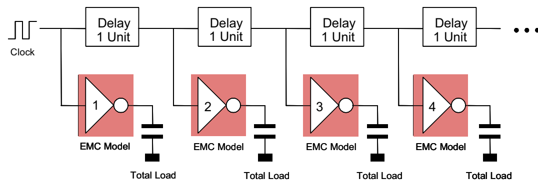

Figure 2: Principal of behavior modeling of cascaded gates

Cascaded gates are consolidated to a single behavior model by taking the local load and the delay times into account (figure 2). Figure 3 confronts the results of a transient circuit simulation to the behavior model of a row of eight cascaded NAND gates.

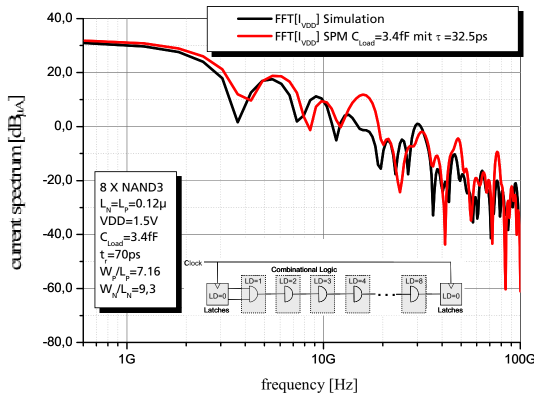

Figure 3: Comparison of the behavior model of 8-cascaded NAND gates with circuit simulations

If the cascaded gates are not of the same type or dimension, the gate with the fastest switching behavior is determined in order to allow a worst-case examination. This can be achieved by a one-time transient simulation of all existing gate types or by extraction from technology dataset. All slower gates are then replaced by the fastest gate, whereas the delay time over all elements is averaged according to the real delay time of each gate type (technology dataset).

In reality one logical depth provides not only a single gate but n parallel gates of different type and activation. The degree of activation can be differentiated between *inverting* and *not inverting* by pre-examination of the layout or by statistical evaluation. Principally, the amplitude of the generated switching current of one logic depth behaves proportionally to the number of parallel switching gates. This is represented by the factor K in equation (1). Whereas the averaged delay time is represented by factor τ. The switching currents of all n-times logical depths can be calculate according to equation (1) under account of the effects mentioned above.

$$i_{VDD\,total}(t) = \sum_{k=1}^{N} K_{col(k)} \cdot i_{VDD(k)}(t-(k-1)\tau) \qquad (1)$$

The mathematical description of the behavior model delivers the entire time-domain switching current of the module under view. Hereby, i_{VDD} represents the supply current of the *worst-case*-gate (fastest gate) with respect to the local supply net parameters RLC.

By forming the partial derivative of equation (1), the dynamic switching current of complex modules can be determined.

$$\frac{\partial i_{VDD(k)}}{\partial t} = \sum_{k=1}^{N} K_{col(k)} \cdot \frac{\partial i_{VDD(k)}(t-(k-1)\tau)}{\partial t} \qquad (2)$$

As shown in figure 4, this procedure has been applied to the EMU-module realized on the TASC test chip (chapter 5).

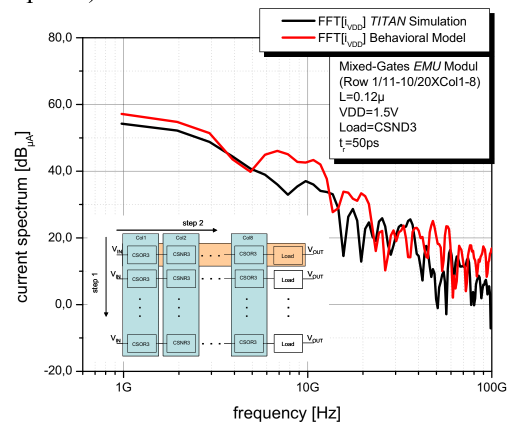

Figure 4: Comparison between the behavior model of 180 mixed gates and the related circuit simulations

The entire module consists of a total number of 180 parallel switched and cascaded logic gates of different type and size (20x9 matrix), whereas the last logical depth is realized as load of NAND gates.

4. Modeling of Power Supply Parasitics

For prediction or analysis of the EMI behavior of an integrated circuit it is necessary to perform an examination of the appearing dynamic current on the IC (∂i/∂t-analysis). Besides the analysis of the active components (gates), such a dynamic current analysis of a specific VLSI design requires an extraction of the parasitic elements of the power supply lines.
In combination with the supply currents which are originated by the switching gates, the parasitic elements cause voltage drops at the supply lines. The static currents cause so called “IR-drops” at the

resistors and the dynamic currents cause voltage drops at the line inductors:

$$V = L \cdot \frac{\partial i}{\partial t} \quad (3)$$

This can exemplarily be validated by performing a circuit simulation of a CMOS gate which is connected to V_{DD} via a non-ideal supply line (see figure 5).

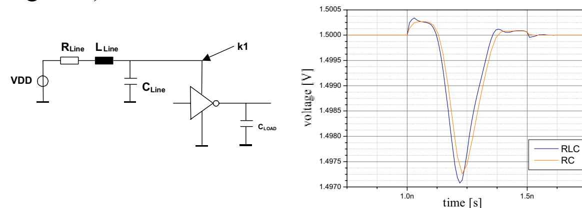

Figure 5: Simulation model of CMOS gate with local parasitic elements RLC; voltage drop at node k1

The supply line corresponds to typical supply line structures. The line length was set to 1mm while the width and height were set to 1µm and 0.29µm respectively. The extraction of line parameters delivers values of R=75ohms, C=81fF and L=1nH.

The voltage breakdown at node k1 which is caused by the switching operation of the CMOS inverter is shown in figure6. Additionally, the simulation results show also the influence of the parasitic inductance of the supply line. If condition

$$\omega L << R \quad (4)$$

is fulfilled, an IC line can be considered only as RC line and the inductance can then be neglected.

Simulations have shown that rise times of 500ps at a 0.13µm gate cause currents on the supply line with frequency rates up to 2GHz. This implies that values for ωL of lines which find application in current copper-based IC technologies are in the same range as their resistance R.

The above described results plus the fact that the inductance per mm of a line is located in the same range as the inductance of package bonding wires follows, that it is important also to extract the parasitic inductance.

An automatic extraction of the parasitic resistances and capacitances from the layout data can presently be achieved with several tools available on the market [6], [7]. When regarding the calculation of parasitic inductances, there are currently no tools available which would perform an automatic extraction from layout data satisfyingly and fulfill the needs of the application described in this paper.

Together with the EMC/EMI modeling approach, investigations concerning an inductance extraction have been made. Good results have been achieved by using the PEEC method based tool Fast Henry [5]. This tool leads to satisfying results in low frequency ranges where substrate effects are not necessarily taken into account. To integrate the substrate effects, a model is under development which uses substrate current loops to describe the behavior of lossy substrate.

5. On Chip EMC-Measurements

For correlating the behaviour models with measurements as well as to improve the quality of those models a test chip has been developed which is able to measure the dynamic current and the voltage on silicon.

The *TASC* (Test chip for Analysis of Switching Currents) is fabricated in a 130nm CMOS technology and provides numerous test structures for the systematic analysis of on-silicon switching noise which are generated by synchronously clocked digital logic and conducted through the supply system topology to the supply pads. The *TASC* contains basically 3 test modules, which are located on the test chip according to figure 7:

- The EMI Modeling Unit (EMU) contains regular and irregular arrays of standard cells for verification of the behavior models described in chapter 3
- The Power Routing Unit (PRU) consists of various local and global supply topologies for the evaluation of different supply concepts and for the correlation with the extracted RLC-models
- The Port Switching Unit (PSU) contains 16 configurable pad output drivers for estimation of simultaneous switching noise.

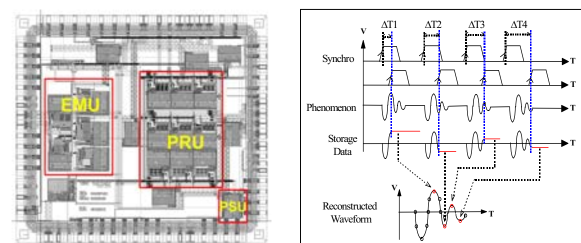

Figure 6: *TASC* test chip layout; on chip measurement sample and hold principal

The overall goal of the TASC test chip is to provide accurate time domain measurements of the switching currents in power supply traces for blocks consisting of many digital standard cells. Since the development of behavioral models is based on the BSIM model of single transistors (chapter 3), the logic under test is configurable from only one single switching gate up to several hundred simultaneously switching gates.

Thus the on-chip current sensor has been designed to provide a sensitivity range of 500µA/V up to 500mA/V. It is built as a differential high gain amplifier configurable from 12dB to 72dB [1]. The

current is calculated from the voltage drop over a small shunt resistor chained into the power supply line.

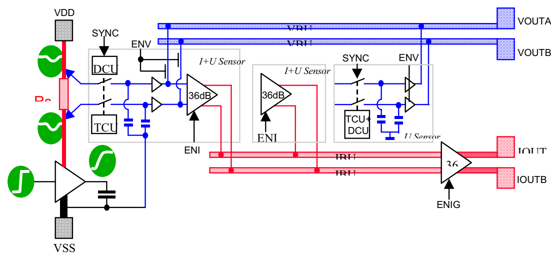

Figure 7: On chip current- and voltage sensor

All on-chip signals are measured by a sampling technique shown in figure 7. A periodically recurring trigger signal forces the logic to switch, and the resulting switching edge or switching current is sampled with slightly increased time delays. Finally, all gained voltage and current values are combined to recreate the original waveform. Time step resolutions are in the range of a few picoseconds which leads to a bandwidth of several GHz. The complete measurement cycle and waveform reconstruction is controlled by the user interface running on a PC.

The test setup for on chip measurements consists of

- Control software for a PC-controlled *TASC* measurement
- An interface card providing digital and analog control voltages and receiving analog measurement data
- *TASC* test board
- *TASC* test chip on the test board.

The signal exchange between PC and test board takes place with a sampling rate of 10 kHz.
The test board was designed to allow also standard-conforming measurements in frequency domain, e.g. measurement of conducted emission according to IEC 61967.4 and measurement of radiated emission according to IEC 61967.2.

6. Conclusion

Modern high-speed silicon systems require new concepts and approaches to a *pre-tapeout* EMC-evaluation. Netlist-based examinations fail due to the inacceptable amount of data and simulation duration. The digital functional modules of complex chips are reduced to simple replacement gates which have a switching current behavior similar to the original modules. In that step some assumptions have to be made, e.g. about the activity level. However, since these current models are mainly to be used for comparison of several power routing schemes, absolutely realistic numbers are not required - worst case assumptions can be made instead.

The RLC parameters of the IC's power routing will be back-annotated from the layout and will be added to the previously derived behavioral models. This new net list can than be simulated with Spice, for example. It is important to include inductances of supply traces into the simulation net list since their physical influence cannot be neglected.

Both behavioral and RLC models have to be correlated with the physical reality. The test chip *TASC* offers regular modules which can be configured in a wide range. Current and voltage sensors are integrated on silicon. Test modes and measurement sequences are controlled by comfortable software running on a PC. In addition to on-chip measurements performed in time domain, the conducted and radiated RF noise emission can be measured in frequency domain according to the IEC standard 61967.

Thus the presented approach allows predicting the emission behavior of an IC during the design phase. This is done by determining the dynamic current considering the parasitic elements and using simplified models for the active devices.

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