ABSTRACT MODELING OF SIGNAL BEHAVIOUR IN INTERCONNECTED INTEGRATED CIRCUITS BASED ON BLACK BOX APPROACH AND MODEL ORDER REDUCTION

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Abstract: This paper presents combined approach for black box modeling of Integrated Circuits (ICs) and interconnecting paths in High Density Packaged (HDP) applications. With this method numerically effective analysis and simulation of the whole (driver, interconnect, receiver) signal path is possible.
Key words: black box, behavioural modeling, macromodeling, model-order reduction, high-speed interconnects, packages

1. Introduction

Modern electronic circuits constitute very complex systems, which call for effective models in order to perform system level simulations for Signal Integrity applications.

The modeling approach to the chip description based on transistor level circuits and symbolic analysis requires very long computation times. Full wave analysis of the whole interconnects structure is computationally inefficient. On the other hand conventional approach based on transmission lines modeling with cascaded π-T lumped element segments leads to very large networks that render the computation process impractical.

Recently a new black box based approach for ICs ports modeling occurred [1]. This method takes advantage of system identification theory and allows to create numerically effective description of a chip behaviour. IC ports are represented by mathematical expansions which relate voltage and current waveforms at each of the IC ports. Constructed models are able to capture nonlinear behaviour of a chip port, are numerically effective and easy to implement in a Spice simulator environment.

On the other hand Model Order Reduction (MOR) approach to interconnects description is a vital alternative to common interconnects modeling methods [2], as it delivers very compact and fast time-domain macromodels that are easily applicable to Spice system level simulations. This approach is based on mathematical reduction of the order of the transfer function by capturing its dominant poles that determine electrical behaviour of the interconnect. In this way port characteristics of the system are maintained while significant speed-up of simulation time is achieved.

The aim of this paper is to show possibility of analysing the whole signal path with combined black box and MOR abstract approaches.

2. Modeling Methodology

2.1 Modeling Outline

For the modeling of signal flow in a HDP module the structure under consideration (fig. 1) is divided into driver (output port of a chip), interconnects and receiver (input port of another chip). Drivers are modeled by black box Radial Basis Functions (RBF) expansions, interconnects are represented by reduced order circuits models. For the considered problem receivers are represented by a capacitance (it is possible, however, to represent them by black box RBF description).

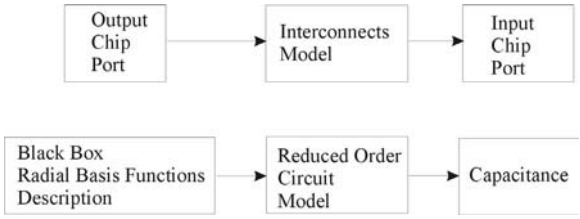

Fig. 1: Signal flow modeling in a HDP module: driver – interconnects – receiver configuration (above) represented by the abstract model (below)

2.2 Active Part Modelling

Output chip ports are represented by black box RBF models. The method originally presented in [1] bases on the observation of current and voltage waveforms at the modeled chip port. By applying to the port proper input identification signal (voltage waveform) and sampling output identification signal - chip response (current waveform), necessary information about the chip is collected. Recorded signals constitute the base for creating of mathematical RBF expansions, where the basis function is assumed to be Gaussian. Constructed macromodel (1) expresses present value of the port

current $i_o(k)$ as a function of the present and past value(s) of the port voltage and the previous value(s) of the port current (contained in the regressor vector $\bar{x}(k)$).

$$i_o(k) = \sum_j \theta_j \exp(-|\bar{x}(k) - \bar{c}_j|^2 / 2\beta^2) \quad (1)$$

The expansion (1) approximates recorded port current waveforms by estimation of the Gaussian functions expansion parameters. This procedure is repeated twice, for high and low logical port state, which gives two RBF submodels. Both submodels constitute the chip representation, where the switching between submodels is suited to the logical activity of the IC.

Concept of active part modeling is presented in the fig. 2. In the first step transistor level model of a chip is implemented in Spice simulator. By applying identification signals current and voltage port waveforms are recorded. Basing on this data RBF expansion parameters are estimated (e.g. in Matlab environment). This expansion is implemented in the Spice environment and can be used in the circuit simulations.

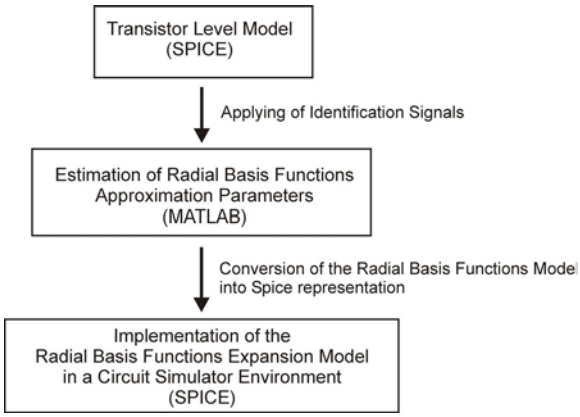

Fig. 2: Active part modeling concept

One of the most important steps in the outlined method is estimation of the RBF expansion parameters (including weight parameters θ_j and RBF centers vectors $\bar{c}_j$; spreading parameter β is assumed to be constant). Although there exist efficient algorithms for estimation of the RBF expansions parameters, e.g. Orthogonal Least Squares (OLS) algorithm [3], obtained IC port macromodels are very often not suited to the Spice implementation. As number of functions in the expansion (1) grows, the approximation of the chip response improves, but the RBF model tends to be not applicable to the Spice simulator, as it causes convergence problems during simulations.

Recently improved, regularized OLS algorithms occurred [4,5], which by penalizing large weight coefficients θ_j help to overcome implementation problems in Spice environment. Expansions obtained by means of these algorithms are sparse, i.e. contain few RBFs, and easily applicable to time-domain simulator environment.

2.3 Passive Part Modelling

Starting point of the interconnect macromodeling concept is partitioning its structure into generic elements (multiconductor transmission lines and discontinuities), behaviour of which can be described with equivalent circuit models. In case of discontinuities (bends and vias) lumped element models are synthesized from S-parameters that are obtained from full-wave simulations. Transmission lines are represented with Telegraphers equations with frequency dependent parameters in order to account for skin-, proximity- and edge-effect. The solution of Telegraphers equations is approximated with Matrix Rational Approximation (MRA) algorithm [6], the outcome of which is a cascade of lumped element sections. MRA algorithm is formulated analytically in terms of predetermined coefficients and per unit length parameters and is much more efficient than a conventional one [7] with respect to number of elements and CPU time for required accuracy in the given frequency range.

Models for the substructures, making up the signal path in interconnects, are connected through terminals to form a network, and subsequently modified nodal analysis formulation is set up in the Laplace domain:

$$\left(\bar{\bar{G}} + s\bar{\bar{C}}\right)\bar{X}(s) = \bar{\bar{B}}\bar{v}_p \qquad \bar{i}_p = \bar{\bar{B}}^T \bar{X}(s) \qquad (2)$$

where $\bar{\bar{G}}$ and $\bar{\bar{C}}$ are matrices containing memoryless and memory circuit elements respectively, $\bar{X}$ is a vector containing node voltages appended with independent voltage source currents and inductor currents, whereas $\bar{\bar{B}}$ is an incidence matrix of the network. Vectors $\bar{v}_p$ and $\bar{i}_p$ contain port voltages and currents. The transfer function of the interconnect can be derived from (2) as follows:

$$\bar{\bar{H}}(s) = \bar{\bar{B}}^T (\bar{\bar{G}} + s\bar{\bar{C}})^{-1} \bar{\bar{B}} \qquad (3)$$

In case of complex interconnect structures size of the resulting matrices is large. Thus to simplify the electrical model of the signal path passive model order reduction algorithm based on congruent transformations is used [8]. The algorithm captures only dominant poles of the network, i.e. the ones that are close to the imaginary axis and hence reduces the order of the network while maintaining port

characteristics in the given frequency range determined by the spectral bandwidth of the propagating digital signals. Reduced order transfer function can be represented with the following equation:

$$\overline{\overline{H}}_r = \overline{\overline{B}}_r^{\,T} \left(\overline{\overline{G}}_r + s\overline{\overline{C}}_r \right)^{-1} \overline{\overline{B}}_r \qquad (4)$$

Equation (4) describes reduced interconnects in the frequency domain. In order to apply it in the system level simulations of the entire signal path together with nonlinear components, its time domain equivalent representation must be generated. Upon expressing (4) in terms of pole and residue pairs and transforming it back into time domain, a corresponding differential equations system in the state-space is obtained. The resulting system of equations can in turn be easily represented with simple Spice elements: voltage controlled current sources, capacitors and resistors, the values of which depend solely on the poles and residues of the reduced interconnect [9].

Described passive part modeling concept is sketched in the block diagram fig. 3.

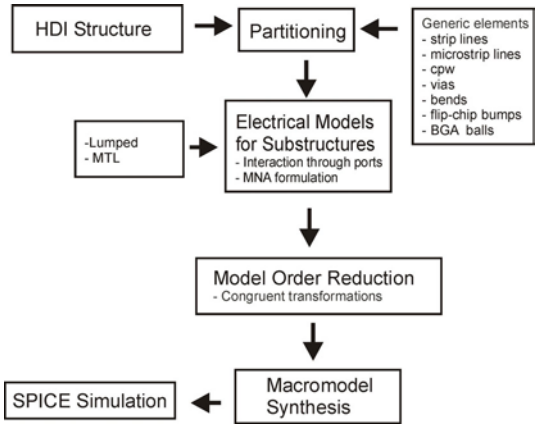

Fig. 3: Passive part modeling concept

3. Modeling Results

3.1 Modeled Structure

In order to prove possibility of combining RBF black box chip modeling with MOR interconnects modeling, a simple structure outlined in the fig. 1 was simulated. Output chip port is represented by transistor level model (fig. 4) of four inverter stages CMOS buffer [10], while interconnects geometrical structure shown in the fig. 5 is built of striplines and a microstrip connected with vias.

3.2 Chip Port RBF Model

Black box RBF model of the considered buffer is represented by 12 RBFs for both high and low internal logical state. The structure of the RBF model consisting of R,C elements and controlled sources is sketched in the fig. 6. Inputs w1, w2 reflect logical activity of the port and stand for time varying switching coefficients between the two RBF submodels Ef1 (low internal state) and Ef2 (high internal state). Ex1, Ex2 provide previous values (samples) of the port current and voltage, while Gy represents output current of the modeled chip port.

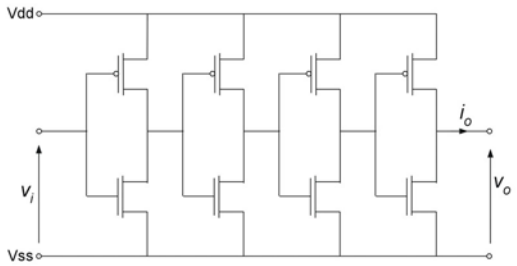

Fig. 4: Four inverter stages CMOS buffer

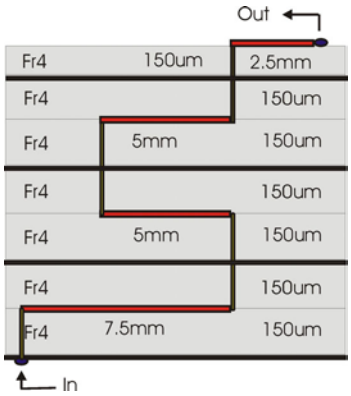

Fig. 5: Interconnects geometrical structure

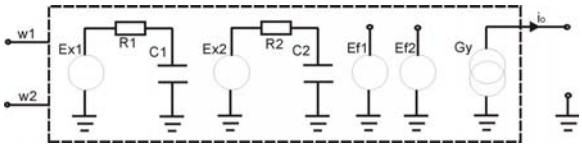

Fig. 6: RBF chip port model

3.3 Interconnects MOR Model

For the interconnects structure original amount of 209 poles is reduced by MOR to 1 real pole and 3 complex poles. Based on the reduced poles, differential equations method [9] is used in order to generate time-domain macromodel, which consists of voltage controlled current sources, resistors and capacitors, as depicted in fig. 7. Ui and Um stand for input and output voltages of the interconnect structure, Aq and Bq are real and imaginary parts of the given pole, whereas kij, kmn (cij, cmn) are residues of the given real pole (complex pole) influencing the input and output ports, respectively.

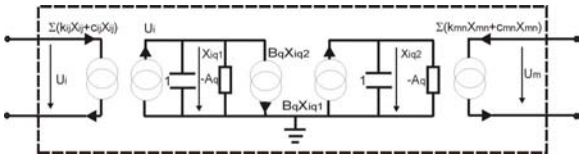

Fig. 7: MOR interconnects model

3.4 Simulation Results

To exemplify applicability of the proposed approach a simple interconnects structure (fig. 5) represented by transmission lines with frequency dependent parameters, driven by transistor level output chip port model (fig. 4) and loaded by 1pF capacitance was simulated in Spice. Obtained results were compared with combined black box RBF and MOR models simulations and are presented in the fig. 8. The output signals waveforms of both approaches agree very well for the considered transient analysis time.

Combined approach offers the potential to significantly speed-up simulation time with reference to conventional methods. For the presented example speed-up with the factor of 10 was achieved. For more complicated structures, including full transistor level chip models and high density interconnect boards even greater speed-up ratios are possible.

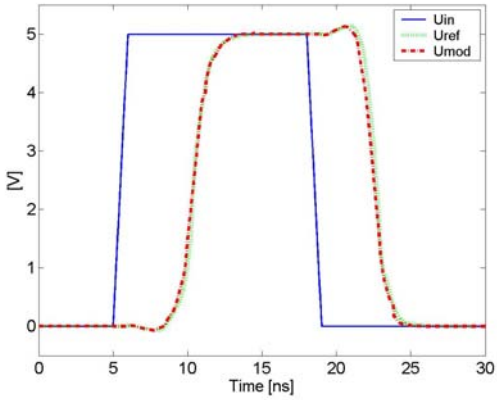

Fig. 8: Voltage waveforms at the 1pF load for a transistor level chip port model and transmission lines interconnects model (Uref), combined black box RBF and MOR approach (Umod), for a given logical activity of the chip port (Uin)

4. Conclusion

In this paper combination of two abstract modeling approaches for the whole signal path analyse in time-domain simulator environment is presented. Black box RBF approach allows for numerically effective modeling of ICs ports, while MOR method provides fast macromodels of passive interconnects. Proposed methodology delivers accurate results and considerable speed-up of simulation time.

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