Influence of Technological Constrains of HDI Organic Substrates on RF Characteristics of Embedded Inductor Component

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Abstract: The use of passive components like inductors embedded in the board substrate offers attractive opportunities for miniaturization and cost reduction. More and more HDI organic substrates are used due to the moderate costs. Design of these embedded passives is one of the greatest challenges in the future. Applying an optimized components' design the RF characteristics of the passive components is limited by the substrate technology. Technological constrains of HDI substrates like the surface roughness in the interface between the metallization line (copper) and the dielectric and etching angle of metallization line influence the RF characteristics of embedded components.
This paper, for the first time, introduces and summarizes the effects of technological constrains of HDI organic substrate on RF properties of embedded inductor component. Methods for effective RF modeling will be introduced. RF models are validated using measurement.

Key words: embedded passives, embedded inductors, HDI organic substrate, surface roughness, etching angle, via, EM field computation, RF measurement, RF modeling, technological constrains

1. Introduction

Wireless communication business is one of the most important areas in electronic industry. Short development cycles, high density, more functionality, greater performance and miniaturization of systems are needed. RF module packaging is one of the low cost solutions for future wireless products [1].
In typical RF modules, the number of passive components is significantly high. The use of passive components like inductors embedded in the board substrate offers attractive opportunities for miniaturization and cost reduction. Designing these embedded passives is one of the greatest challenges. Applying an optimized components' design, the RF characteristics of the passive components is limited by the substrate technology. Technological constrains which cause non ideal geometries affect the RF performance of components. For HDI organic substrates the technological constrains are: surface roughness, etching angle and the hollow via form. These aspects will be investigated in this paper.

First the HDI organic substrate is introduced with its characteristics and constrains. The relevance and effects on RF properties of embedded inductor components are shown. Methods for an efficient RF modeling will be introduced. Finally the models are validated by RF measurement.

2. Multilayer HDI Organic Substrate

2.1 Layer Stackup

Figure 1 shows the cross section of an multilayer HDI organic substrate. A typical stack-up starts with an FR4 core that is constructed using standard printed circuit board techniques. This is followed by one or more ~2-3 mils thick layers of copper-clad polyimide deposited on one or both sides of the core. These are the HDI layers in which the passive components are fabricated.

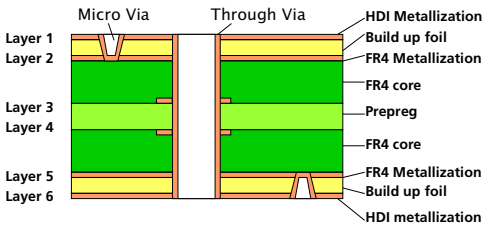

Figure 1: Cross Section of HDI Substrate

2.2 Material Properties

Typical material properties for these compound substrates are given in Table 1. The conductivity of pure copper is $5.7 \cdot 10^7$S/m according to the data sheets. Due to contaminations, the conductivity of the copper layers in practice lies mostly below this ideal value at about $4.8 \cdot 10^7$S/m.

Table 1: Material properties of HDI organic substrate

Material	Relative Permittivity ε_r	Loss Tangent tanδ
FR4	4.6–5.2 (typically 4.8)	0.01–0.03 (typ. 0.014)
HDI (Polymer)	3.0–4.3 (typically 3.9)	<0.01–0.03 (typ. 0.026)
Solder Mask	4–5 (typically 4.2)	0.02

More process details and information on suppliers can be found in [2].

2.3 Technological Constrains

Cross section of typical HDI organic substrates show geometrical peculiarities of metallization lines. Structures differ from ideal geometries due to respective fabrication processes. These characteristics can influence the RF properties of components.

On the bottom interface between metallization and substrate the lines are rough. Figure 2 shows a cross section of the investigated HDI organic substrate with surface roughness. A deepness of surface roughness with about $2\sigma=7\mu m$ (see below) was measured under an optical microscope.

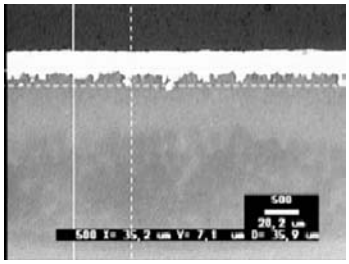

Figure 2: Surface roughness in HDI metalliziation

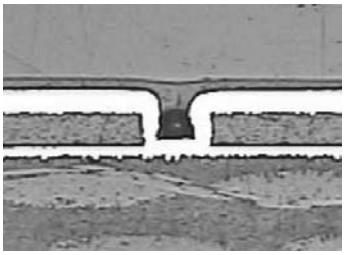

Figure 3: Via interconnection in HDI substrate

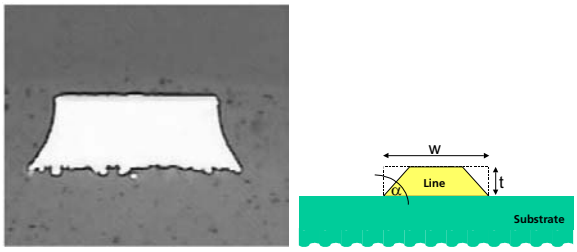

Figure 4: Etching angle of metallization in HDI substrate

Via interconnection show specific form. Compared to other technologies the vias are not fully metallized (figure 3). The metallization thickness of hollow via is about 20µm.

Correlating with figure 4 the line structures have no ideal rectangular cross section. The etching process during fabrication causes trapezoid lines. Etching angle can be defined. For HDI metallization etching angles α from 70° to 75° (typical 72°) are observed. For HDI metallization etching angle α lies between 50° up to 60° (typically 50°).

3. Embedded Inductor Design

The basic design of the embedded inductor is shown in Figure 5. The inductor loops are defined in the HDI metal layers 1 and 2 in Figure 1. Thickness of HDI metallization is 36µm whereas the thickness of FR4 core metallization is 13µm.

The inductor loops are squares, connected by a via, and surrounded by a coplanar ground ring. The electrical feed lines have a grounded coplanar configuration. The number of loops, the inner loop diameter and line width are variable parameters [3].

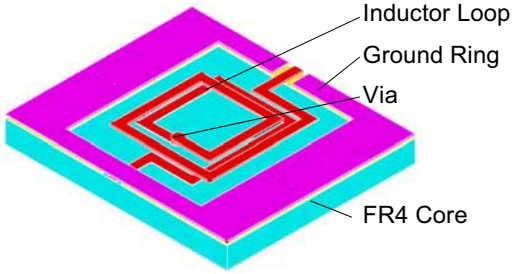

Figure 5: Design of an embedded inductor component

3. Influence of Technological Constrains on RF Characteristic of Embedded Inductor Component

3.1 Surface Roughness

The surface roughness increases mainly the ohmic losses in the microstructure [5]. The current distribution within the metallization line is influenced by the skin effect. That means the alternating current follows within a limited depth on the surface of the metallization line. With increasing frequency, the layer in which the current is actually flowing decreases. In case of rough surfaces, the current distribution will be inhomogeneous. This causes an increase of line attenuation per unit length from the value α_p for a smooth interface up to the value α_{peff} for a rough substrate.

The inner inductance is also increased by the inhomogeneous surface in much the same way as bends in a transmission line give rise to an additional inductance through current crowding. This effect can be neglected. However an inductor component is designed, of course, to have a large and thus dominating outer inductance.

The influence of an improved surface structure on transmission line characteristics was investigated in [4]. The ohmic resistance of the metallization of inductor component considering surface roughness $R_{geo,SR}$ can be calculated correlating to [6] using equation (1).

$$R_{geo,SR} = \rho\left[1+\frac{2}{\pi}\arctan\left[1{,}4\left(\frac{\sigma_{eff}}{\delta}\right)^2\right]\right]\cdot\left[\frac{l}{A-(w-2\delta)\cdot(t-2\delta)}\right] \quad (1)$$

where δ represents the skin depth, σ_{eff} the effective surface roughness, ρ the specific resistivity, A the

cross area of conductor line, *w* the line width, line length *l* and *t* the line thickness.
Figure 6 shows the frequency dependent resistance including the roughness effect for an embedded inductor for frequencies up to 15GHz. For this example (the line width) *w* is 100µm and (the line thickness) *t* is 36µm. The line length l can be calculated from the decoiled inductor. For the inductor with *N* = #loops = ½ the total line length is 4mm. The resistances including roughness are compared with the resistances of the structure neglecting the roughness. With increasing frequency, the gap between both values increases. For frequency ranges above 500MHz, this roughness (2σ=7µm) has to be accounted for. For lower frequencies, the roughness can be neglected. This statement is valid for other geometry dimensions of inductor components as well.

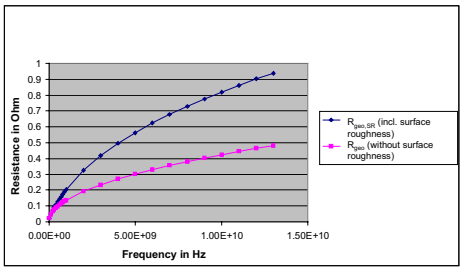

Figure 6: Frequency dependent resistance of embedded inductor considering surface roughness. Example of inductor considering number of loops N=½, inner radius IR=250µm, line width w=100µm

3.1 Via Interconnect

The metallization thickness is able to affect the resistance and inductance of via. Due to the skin depth δ which is for interesting frequency ranges (δ(f=1GHz)=2.3µm; δ(f=10GHz)=0.73µm) smaller than the matallization thickness (20µm) of via the hollow via has nearly the same RF characteristic compared to filled via. Detailed values for resistance and inductance can be calculated correlating to [7].
For a via structure with diameter of 100µm and height of 60µm the resistance of hollow via lies for frequencies of 1GHz in the order of 2mΩ. This value is about 1.2mΩ smaller than resistance of filled via. Compared to ohmic losses of complete inductor component (160mΩ up to 1.6Ω) this error (lower than 5%) can be neglected.
The via inductance has a value of about 4.8pH. Compared to filled via this value is about 0.9pH smaller. This small differences are neglectable for complete inductor component (values between 1nH up to 15nH).
This results show that the hollow via will not limit the RF performance of embedded inductor mainly. EM field computation can be performed using filled approximation. A modification of technology to fabricate filled vias to improve RF properties is not needed.

3.1 Etching Angle

To investigate the influence of etching angle on RF performance of embedded inductor 2 dimensional field computation on line structures were performed. The computations showed, that the etching angle causes increasing of line inductance L' and line resistance R' mainly. Effects on line capacitances C'can be neglected.
Figure 7 and 8 show results of 2dimensional field calculation for inductance and resistance values. Etching angles between 45° and 90° were investigated. Angle of 90° correlates with a rectangular cross section. With decreasing of etching angle (increasing of deviation from rectangular shape) the resistance and inductance per unit length increase. Lines with width of 100µm and thicknesses of 36µm (HDI metallization layer) and 13µm (FR4 core metallization layer) were considered. For given etching angles inductances increas with up to 25%, whereas resistances increasing with up to about 35%. These effects needs to be considered in RF design.
3 dimensional modeling of etching angle in inductor design leads to a high modeling and computation effort in EM field calculation. To reduce these effort a rectangular line geometry with a effective line width w_{eff} can be defined. The effective line width has to be determined, that the increasing of resistance and inductance values are captured. Effective line width w_{eff} can be calculated on base of original line width *w* subtracted by correction term Δw (2).

$$w_{eff} = w - \Delta w(t,\alpha) \qquad (2)$$

The correction term Δw depends on line thickness *t* and etching angle α. For different line width the correction term will have the same value.
Using modeling methodology to extract parameterized equations for design library components structures [3] the equation for Δw was extracted (3).

$$\Delta w[mil] = a_0 - a_1\alpha + a_2 t - a_3 \cdot \alpha \cdot t \qquad (3)$$

with *t* in mil, α in degree.
Figure 9 shows the correlation between FEM calculation results and extracted equation.

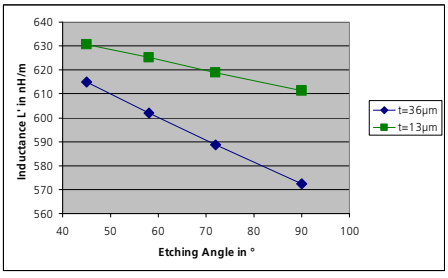

Figure 7: Line inductance L' as a function of etching angle α for various metallization thickness t

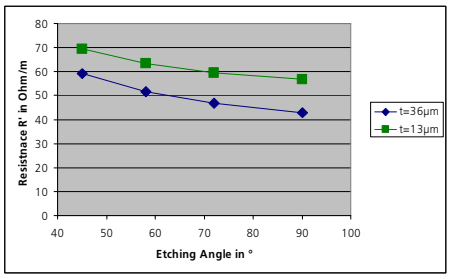

Figure 8: Line resistance R' as a function of etching angle α for various metallization thickness t

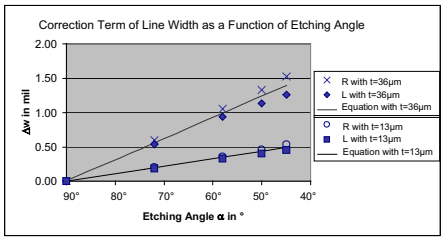

Figure 9: Correction term Δw as a function of etching angle α and metallization thickness t;

3. Model Validation using RF Measurement

To validate the EM calculation model an organic substrate test board was fabricated. Figures 10 shows the results of both EM calculation and measurement in terms of the raw S-Parameters.

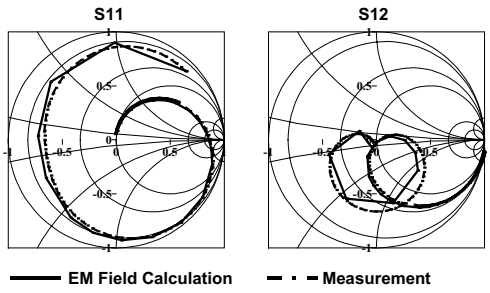

Figure 10: S-Parameters of an embedded inductor, measurement results versus EM field calculation

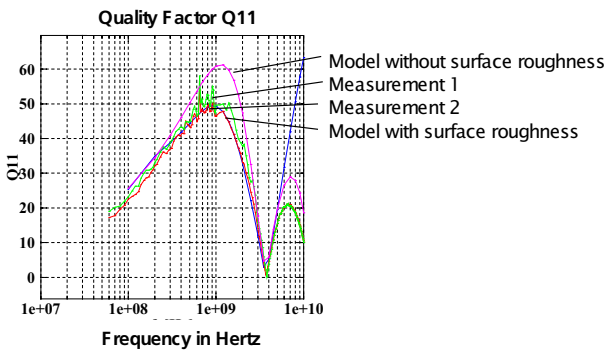

Figure 11: Quality factor of embedded inductor, comparison of RF models and measurement, example of inductor: number of loops N=1.5, inner radius IR=500µm, line width w=100µm

Comparison of measured and calculated data with respect to quality factor shows the importance of considering the surface roughness. For embedded inductors the one-port quality factors Q11 and Q22 are given by equations (4).

$$Q_{ii} = \left| \frac{\mathrm{Im}(Yii)}{\mathrm{Re}(Yii)} \right| \tag{4}$$

where i = 1 or 2, Yii represents the appropriate diagonal element of the two-port Y-parameter matrix for the inductor. The agreement between measurement and RF model is excellent.

7. Conclusion

The influence of technological constrains of HDI organic substrate on RF characteristics of embedded inductor components was investigated. It was shown that surface roughness and etching angle influence the RF characteristics significantly. The Influence of hollow via can be neglected.

For surface roughness and etching angle RF modeling procedures were introduced. Electrical values with respect to rough deepness and etching angle were given. Modeling methods base on EM field computation. The models were validated using RF measurement.

References

[1] A. Ostmann, A. Neumann, J. Auersperg, C. Ghahremani, G. Sommer, et. al; "Integration of Passive and Active Components into Build-Up Layers"; EPTC 2002 Shanghai.

[2] E. Jan Vardaman, Frank Bachner, Doug Feicht; "High Density Microvia Substrates: Markets, Applications, and Infrastructure", 1999 TechSearch International, Inc, 4801 Spicewood Springs Road, Suite 150, Austin, Texas 78759, July 1999.

[3] G. Sommer et. al; "Development of a Design Library for Embedded Passive RF Components in HDI Organic Substrate Material", submitted to IEEE conference EMC 2003, Istanbul, May 2003.

[4] R. Schulz, E. Klusmann, J. Schulze, H. Meyer, H. Reichl, G. Sommer et. al; "The morphology of the Metal-Polymer Interface and its Implication to High Frequency Signal Transmission", IPC Printed Circuit EXPO 2001, April 2001, Anaheim Calif.

[5] R. K. Hoffmann; "Integrierte Mikrowellen-schaltungen"; Springer Verlag, Berlin Heidelberg New York Tokyo 1983; p. 201, 202.

[6] G. Sommer, et. al; „Influence of Surface Roughness on RF Characteristics of Embedded Inductor Components in HDI Organic Substrate Material"; IMAPS, 14th European Microelectronics and Packaging Conference & Exhibition, Friedrichshafen, Germany, 23-25 June 2003

[7] B. C. Wedell; "Transmission Line Design Handbook"; Artech House, Inc., 1991, ISBN 0-8900