EXPERIMENTAL EVALUATION OF A LOW EMI MULTILAYER PCB STRUCTURE FOR HIGH SPEED DIGITAL CIRCUIT

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Abstract: The effectiveness in EMC characteristics of a multilayer Printed Circuit Board (PCB) structure, the power bus of which consists of coplanar traces embedded in the two ground layers, is experimentally determined. Investigation of radiated EMI, voltage fluctuation between power and ground, and ESD immunity is performed using 6-layer high-speed controller PCBs. The results indicate that radiated EMI can be reduced without damaging power integrity. At the same time this structure has better resistance to ESD than conventional structure. It is concluded that this structure is optimum for high-speed circuits considering EMC characteristics up to 2 GHz.
Key words: PCB, Power Bus, EMI, Power Integrity, Voltage Fluctuation, ESD.

1. Introduction

Recently, a number of reduction techniques have been published for radiated EMI caused by power bus noise [2-5]. One technique utilizes capacitors that control the current reflection at the edges of the power and ground planes and reduces emissions along the edges [2,3]. But the effectiveness is restricted by the intrinsic inductance of the capacitors at higher frequencies and adding extra capacitors is undesirable. Another technique utilizes the enhanced capacitance between adjacent power and ground planes in multilayer PCB [4]. But this technique requires high relative permittivity material and adds extra layers.

Segmented power planes are commonly employed to isolate devices that put noise on power buses [5]. But return current path discontinuities caused by a segmented power plane can be sources of radiated EMI and affect the signal integrity of a high-speed bus [6,7].

In the previous paper we introduced a new multilayer PCB structure which we call SGGS structure in connection with the arrangement of the layers (Signal-Ground-Ground-Signal in 4-layer PCBs) as shown in Figure 1 [1]. The basic idea is to adopt low power bus radiation and low signal trace impedance that are considered to be irreconcilable with the smallest possible number of layers. The power traces embedded in the two ground layers do not necessarily need to be low-impedance as far as substantial decoupling capacitors are mounted in the vicinity of high-speed devices. Consequently we combined power traces and low impedance decoupling capacitors near devices.

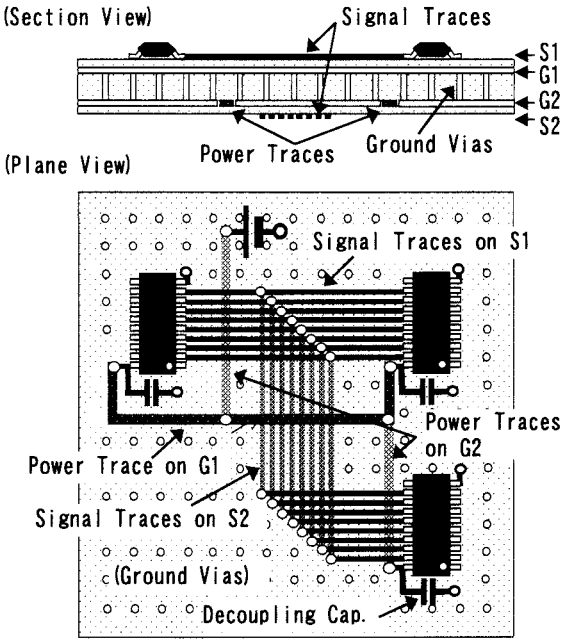

Figure 1. Basic configuration of SGGS structure PCB [1].

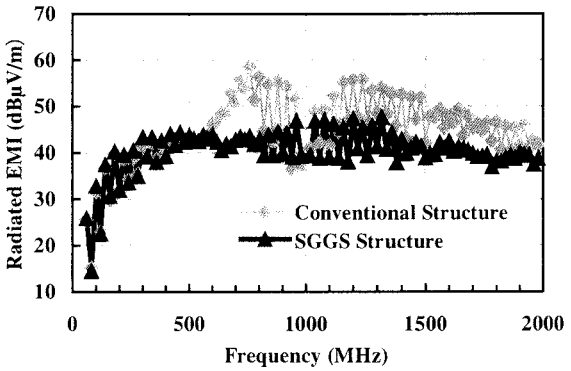

Figure 2. Radiated EMI comparison for SGGS and conventional structure using 4-layer test PCBs [1].

The power traces must have substantial ampacity in order to avoid voltage drop. The two ground layers are tightly connected each other with the vias at regular intervals in order to eliminate the plane resonance and maintain continuity of the return current paths.

Because there is no plane resonance regardless of the spacing between two ground layers, the smallest spacing between the signal layer and the ground layer can be adopted. In consequence this structure can be optimum for high-speed circuits. The power traces have freedom to perform layer transitions between the two ground layers to avoid discontinuities of the signal return current on the ground planes. In consequence common-mode radiation can be diminished at the same time.

Radiated EMI studies using simple 4-layer test PCBs were conducted comparing SGGS and conventional structure as shown in Figure 2. The trend clearly demonstrates that the radiation from the SGGS PCB is lower than conventional PCB in higher frequencies up to 2 GHz.

This paper extensively investigates the effectiveness in EMC characteristics of the SGGS structure using 6-layer high-speed controller PCBs; radiated EMI, voltage fluctuation between power and ground, and ESD immunity.

2. EMI Evaluation of 6-Layer Controller PCB

2.1 Description of The Controller PCBs

Radiated EMI studies using 6-layer high-speed controller PCBs were conducted comparing SGGS and conventional structure. The PCBs equip 300MHz PowerPC Micro Processing Unit (MPU) with one memory bus of 100 MHz connected to 4 on-board SDRAMs and 1 DIMM as shown in Figure 3. Two ASICs for image processing are connected to the 33 MHz PCI bus. The power pins of every LSI are fully decoupled with 0.1 μF ceramic capacitors.

The size of the PCBs was 247mm x 152 mm. One PCB is SGGS 6-layer (actually S-G-S-S-G-S) structure and the other is conventional 6-layer SGVS (S-G-S-S-V-S) structure shown in Figure 4. The components are arranged identically on the two PCBs and the artworks are identical except for the power buses. Figure 4 also shows the main 3.3 V power traces of the SGGS PCB. The SGGS PCB has ground-ground vias at intervals of about 10 mm.

Most part of the 3,3 V power trace is routed on the Layer 2 carefully avoiding return current path discontinuities of the high-speed buses. The power trace is connected to the power islands beneath the LSIs shown in Figure 4 via surface layers. For comparison, the conventional PCB has the identical power islands.

The current carrying capacity of a power trace is a function of the cross sectional area of the trace and the allowable temperature rise on the conductor as indicated in ANSI/IPC-D-275. At the same time voltage drop caused by resistivity, for instance about 280 mΩ/m for 1 mm wide and 35 μm thick copper, should be considered. So the widths of the power traces are carefully determined according to the amount of current and the length.

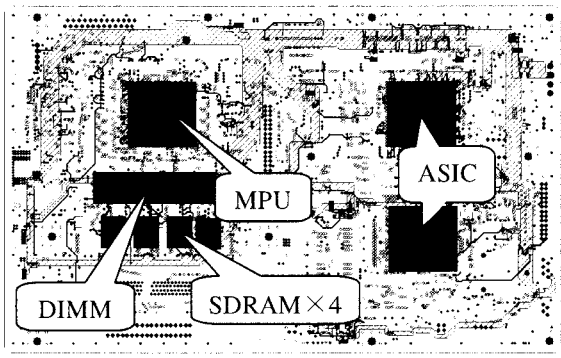

Figure 3. Power traces and device arrangement of SGGS controller PCB.

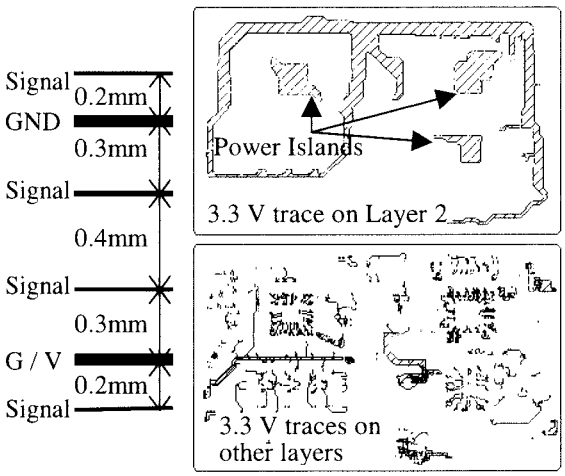

Figure 4. Layer arrangement of the controller PCBs (left) and 3.3 V power traces of the SGGS PCB (right).

2.2 EMI Measurement Results

The PCBs were tested in a 3m anechoic chamber to measure the radiated EMI. The PCBs were mounted on a metal plate of 610mm x 460 mm as a frame ground and placed horizontally in the chamber at the height of 800 mm. The distance between the PCB and the metal plate was 5 mm. The larger value between the horizontal and vertical emission was chosen for radiation intensity at each frequency unless otherwise stated. Measurements are done during repetitive SDRAM read/write operations.

Figure 5 shows the radiated EMI of the controller PCBs of SGGS and conventional structure without connecting peripheral cables. The trend clearly demonstrates that the radiation from the SGGS PCB

is lower than conventional PCB in higher frequencies up to 2 GHz, but not drastically comparing to the result shown in Figure 1. It is presumably because the number of the decoupling capacitors is increased tenfold from the test PCB so that the impedance of the power bus is low.

As mentioned in the previous paper [1], it is contemplated that the SGGS PCB has less common mode current on the ground, so we have evaluated the effect of common mode interference using cables and metal covers.

Figure 6 shows the radiated EMI spectra of the PCBs with USB and parallel I/O cables attached and the effect of an aluminum cover on the PCBs. The aluminum cover, 25 mm high and attached to the metal plate, has apertures of up to 100 mm wide for connectors and cables.

The cables increase the radiated EMI from the conventional PCB especially below 600 MHz. The aluminum cover decreases the radiated EMI of both PCBs at higher frequencies than 1.5 GHz. The radiation from the conventional PCB increased at below 1.5 GHz by adding the cover, but there were no such significant change for the SGGS PCB.

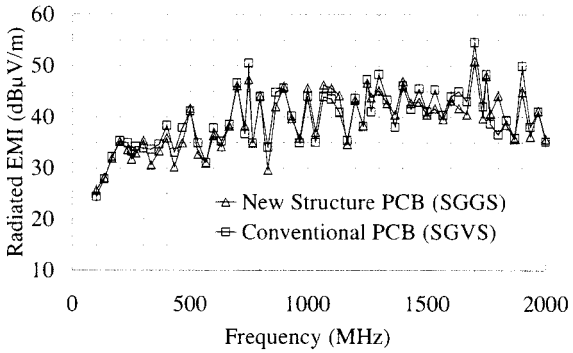

Figure 5. Radiated EMI comparison for 6-layer controller PCBs of SGGS structure (S-G-S-S-G-S) and conventional structure (S-G-S-S-V-S) without connecting peripheral cables.

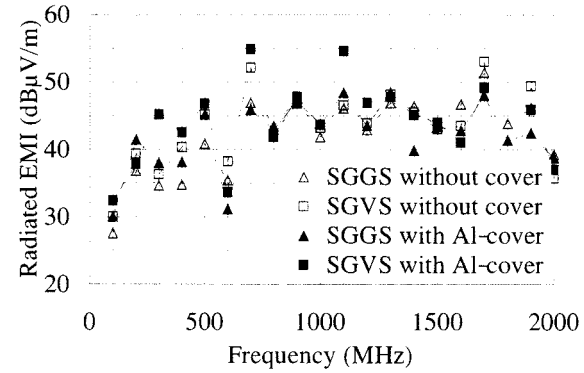

Figure 6. Radiated EMI comparison for controller PCBs with peripheral cables, with/without aluminum covers (harmonics of 100 MHz only).

3. Power-Ground Voltage Fluctuations

The power-ground voltage fluctuations of SGGS PCB are measured at seven points (A-G) on the 3.3V power traces, SDRAM power pins, and the power islands of the MPU and the two ASICs shown in Figure 7 and compared with those of the same locations on the power plane of the conventional PCB. Measurements are done during repetitive SDRAM read/write operations, while the ASICs are running idle.

Table I shows the voltage fluctuations on the power trace. Voltage fluctuations of SGGS PCB are larger at the points where actual distance from MPU and DRAM is larger (B, D, and F). Point E is also in the vicinity of MPU but shows smaller fluctuations because a decoupling capacitor of 0.1μF is in closer vicinity. To confirm the effect of capacitor, we added a 0.1μF capacitor in the vicinity of the point F. As a result, the fluctuation is reduced from 464 mV to 156 mV.

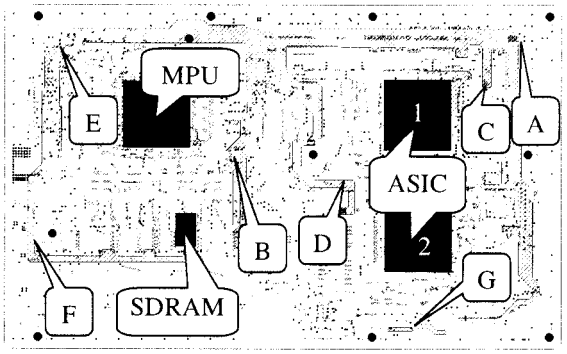

Figure 7. Measurement Points of Voltage Fluctuation on 3.3V Power Traces.

Table I Voltage Fluctuation on 3.3V Power Trace

Measurement Point	SGGS (mV)	SGVS (mV)
A	72	120
B	272	236
C	72	124
D	216	140
E	144	152
F	464	208
G	72	108

Table II Voltage Fluctuation on SDRAM Power Pins and 3.3V Power Islands of MPU and ASICs (mV)

Measurement Point	SGGS	SGVS
SDRAM Power Pins (Ave.)	430	424
Center of MPU	208	264
MPU Power Pins (Ave.)	272	298
Center of ASIC-1	62	80
Center of ASIC-2	60	86

Table II shows the voltage on power pins of one SDRAM and the 3.3V power islands of the MPU and the two ASICs. Voltage fluctuations on the power islands are smaller for SGGS PCB, because the islands are well decoupled and isolated each other by the power trace. At the power pins of the SDRAM, one of the major noise sources, fluctuations are slightly larger for the SGGS PCB, presumably because the pins are directly connected to the high-impedance power trace.

4. ESD Immunity Comparison

ESD immunity is tested by contact discharge at up to 9kV using a test-gun which integrates a test socket and an appropriate pulse generator for the test in accordance with IEC-6100-4-2. The test points on the ground plane are shown in Figure 8. Points A-E are directly connected to the metal ground plate with metal spacers.

No damage is noted at all the test points except H and G while voltage is increased to 9kV. As shown in Table III, system halt occurs at points G and H in the vicinity of the MPU of the conventional PCB. As for the SGGS PCB, read/write error of the SDRAMs is observed at 9kV at point G.

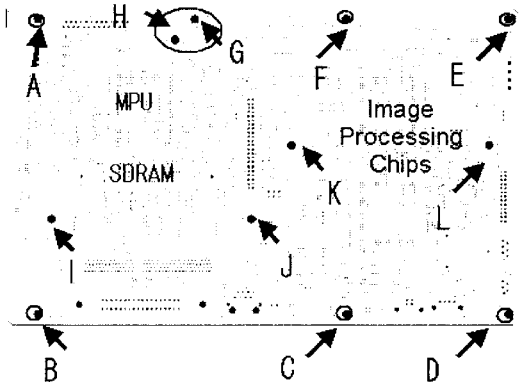

Figure 8. ESD Test Points of The Ground.

Table III ESD Test Results

Test Point	SGGS	SGVS
G	+9kV Pass -9kV R/W error	+7kV Halt -8kV Halt
H	±9kV Pass	±7kV Halt

5. Conclusion

The effectiveness in EMC characteristics of a multilayer PCB structure, the power bus of which consists of coplanar traces embedded in the two ground layers, is experimentally determined. Radiated EMI can be reduced especially when peripheral cables are attached or a poor-shielding metal is in close vicinity, because of less common mode current on the ground. Power integrity is not diminished and better noise isolation is obtained when power islands for LSIs are employed. ESD immunity test is performed by contact discharge to the ground and better resistance than conventional structure is obtained.

It is concluded that this structure is optimum for high-speed circuits considering EMC characteristics up to 2 GHz.

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