

Investigation of Capacitor Allocation to Reduce EMI Arising from a Via-Hole Penetrating through Power-Distribution Planes

Takashi Harada, Naoki Kobayashi,
Takahiro Yaguchi*, Akira Wakui*, and Seishi Eya*

Jisso Research Laboratories, NEC Corporation

*NEC Informatec Systems

E-mail:t-harada@bl.jp.nec.com

Abstract: The dependence of voltage disturbances between the power-distribution planes to allocation of a capacitor nearby the via is investigated. Power-distribution plane resonance in multi-layer printed circuit boards (PCBs) is one of the main sources of electro-magnetic interference (EMI). Via penetrating through the power and ground planes gives a rise to the voltage disturbance between these two planes. Voltage reduction effectiveness to allocate a decoupling capacitor is evaluated quantitatively by using an equivalent circuit model. Calculated results have showed the optimized capacitor allocation. A simple analytical formulation has also been introduced about the relation between the space of the power-distribution planes and the distance from the via to the decoupling capacitor in order to determine disturbances of power distribution planes within certain thresholds. Design rule for allocations of decoupling capacitors is also described.

Key words: multi-layer PCB, power-distribution planes, via, decoupling capacitor, EMI

1. Introduction

Power-distribution plane resonance in multilayer printed circuit boards is one of the main causes of radiated electro-magnetic interference (EMI). A via penetrating through the power and ground planes gives a rise to the voltage disturbance between these two planes [1][2]. The discontinuity of return currents flowing on the both planes generates the displacement current between them and excites a voltage. Connecting the both planes by a decoupling capacitor near by the via is a well-known EMI reduction technique. The capacitors achieve lowering the impedance between the planes and suppress the voltage. To incorporate this technique into PCB EMC design process, quantitative evaluation of this effect has to be performed. In this paper, we investigate the dependence of voltage disturbances between the power-distribution planes to allocation of the capacitor near by the via by using an equivalent circuit model, and extract some important characteristics. The effect of the via and the power-distribution planes is expressed by a current source and a two-dimensional equivalent circuit model.

2. Equivalent Circuit Model of Via, Capacitor and Power-Distribution Planes.

Figure 1 shows the cross sectional view of a via structure in a four-layer PCB. The via interconnects traces routed on the both surfaces and penetrate through the power-distribution planes. The second plane and third planes are corresponded to the ground plane and the power plane, respectively. A capacitor is placed nearby the via to reduce the voltage disturbance between these two planes.

Figure 2 shows the two-dimensional equivalent circuit model of the power-distribution planes, which consists of small segments approximating planar circuits. The capacitance C , inductance L and resistance R of each planar segment are represented by:

$$C = \varepsilon_0 \varepsilon_r \frac{l^2}{t} [F], \quad (1)$$

$$L = \mu_0 t [H], \quad (2)$$

$$R = 2 \frac{\rho}{s} [\Omega], \quad (3)$$

where l and t represent the length and thickness of the planar segment, respectively. ε_0 and μ_0 are permittivity and permeability in free space, respectively. ε_r represents a relative permittivity of the material constituting the PCB and its value is about 4.4~4.7 in the case of the FR4. ρ represents a resistance per unit length and its value is about $1.72 \times 10^{-8} \Omega \cdot \text{m}$. s represents the skin depth of the planes where it is assumed to be much smaller than the thickness of the planes. In our calculations, the power-distribution planes are assumed to be square

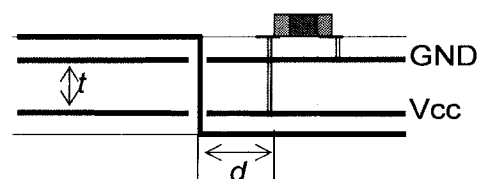


Figure 1. A via penetrating through the power and ground planes for a 4-layer PCB

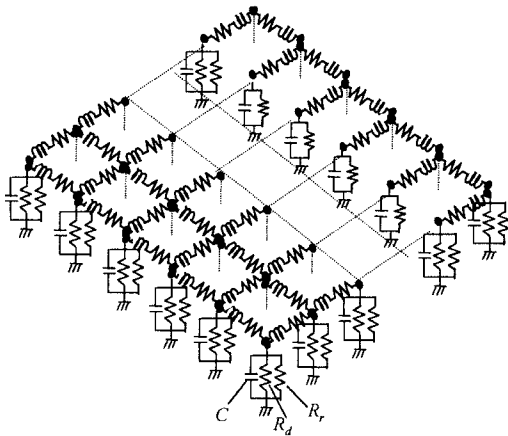


Figure 2. Two-dimensional equivalent circuit model of power distribution-planes

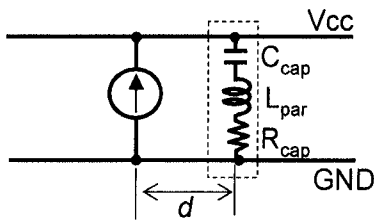


Figure 3. Equivalent circuit model of the via and the capacitor

whose sides are 130 mm, and are divided into small planar square segment whose sides are 5 mm. Then C and L are represented by:

$$C = \frac{9.96 \times 10^{-16}}{t} [F], \quad (4)$$

$$L = 1.26 \times 10^{-6} t [H], \quad (5)$$

$$R = 6.7 \times 10^3 [\Omega], \quad (6)$$

Although the skin depth s is inversely proportional to the square root of frequency, the value at 300MHz (30 μ m) is utilized in order to simplify the analysis.

Figure 3 shows the equivalent circuit model of the via, the decoupling capacitor and the power-distribution planes. The via is regarded as the current source [1] and capacitor is expressed as capacitance C_{cap} , interconnect inductance L_{int} which consists of the equivalent series inductance of the capacitor and parasitic inductance of pads and via holes connecting the capacitor to the both planes, and the equivalent series resistance of the capacitor R_{cap} . The C_{cap} , L_{int} and R_{cap} in the equivalent circuit model, we used here, were 0.01 μ F, 1.6nH and 60m Ω , respectively.

EMI depends on the voltages between the power and the ground planes at edges [3]. Since the effect of the via was represented as current source, the transfer impedance between the via and the edge of the

power-distribution planes, Z_{21} , is an important criteria to evaluate the EMI emission level. Positions of the current source and the observation point of voltages are allocated at both edges of the power-distribution planes which are connected by a diagonal line of the square

3. Transfer Impedance Properties of Power-Distribution Planes

The transfer impedance Z_{21} of the power-distribution planes was calculated for different values of the space t between the power and ground planes. Figures 4(a), (b), and (c) show the frequency dependency of the transfer impedance Z_{21} for different values of distances between the decoupling capacitor and the current source, when $t=1.0$ mm, 0.6mm, and 0.2mm, respectively. Note that since 1 A current is used as a source, the voltages are equal to the transfer impedance Z_{21} . The transfer impedance depends on the plane space and via-capacitor distance. The impedance becomes lower if the space t is narrower. The impedance also becomes lower when the decoupling capacitor is brought closer to the current source. These characteristics mean that putting the capacitor as near as possible to the via, and narrowing the plane space are necessary to reduce the EMI from the power-distribution planes. In these figures, the peaks of voltages due to resonances are observed at specified frequencies. The first peak in the frequency-band around 100MHz is a parallel resonance due to the capacitance of the power-distribution planes and the interconnect inductance of the decoupling capacitor. At these frequencies, since the size of the planes is much smaller than the wavelength, these planes act as a parallel plate capacitor. And the interconnect inductance is dominant, because the frequency is higher than the self resonance of the decoupling capacitor. The peaks appeared at the frequencies higher than 500MHz are resonances due to cavity modes regarding power-distribution planes.

4. Design rule for allocations of a decoupling capacitor

It is very difficult to extract an important information about the distance between the via and the decoupling capacitor at the resonant frequencies. Therefore, we have investigated the voltage properties at the frequencies except resonant ones. Figure 5 shows the dependence of Z_{21} on the distance between the current source and the decoupling capacitor for values of t at 300MHz. One can know from this figure that the dependence of the transfer impedance to the via-capacitor distance is significant when the space t is large. At narrower space, however, this dependency is small. This means that if the space between power-distribution planes is small,

one can allocate a decoupling capacitor at further position from the via.

It is desirable to allocate decoupling capacitors as close as possible to the via. Actually, it is difficult to allocate all decoupling capacitors near by them. Therefore, investigating acceptable threshold of the distance between the via and the decoupling capacitor is very important. Figure 5 shows that the voltage level increases as the distance between them becomes larger. This tendency is more apparent when the interval t is large. A certain relation

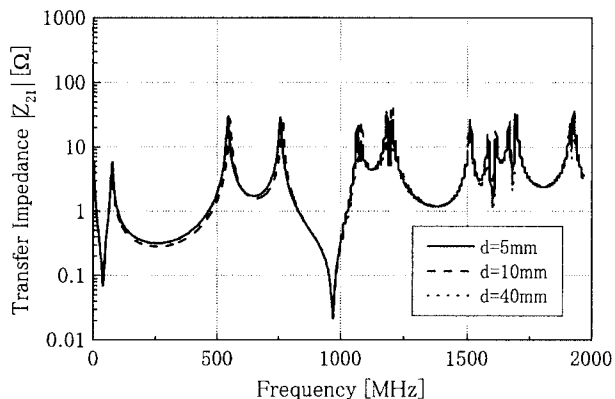
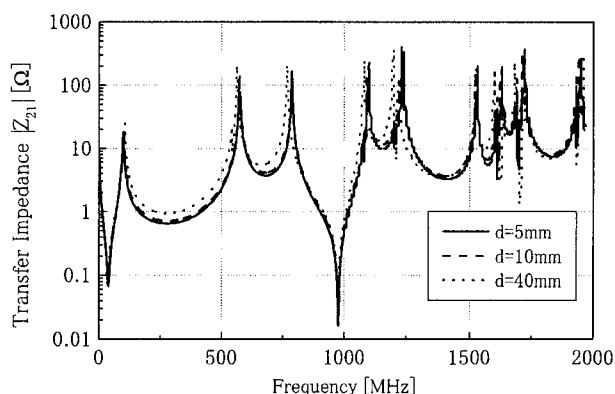
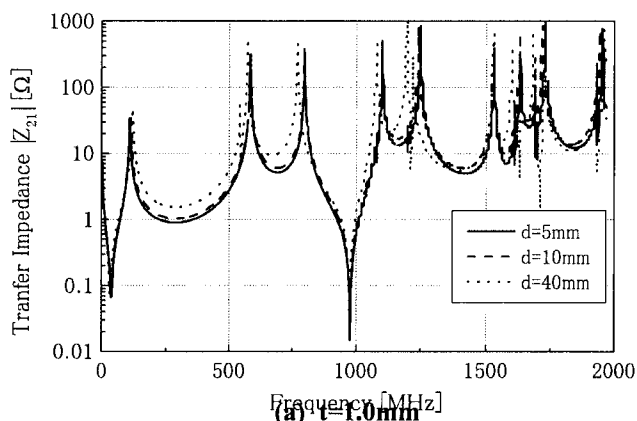


Figure 4. Frequency dependence of transfer impedance Z_{21}

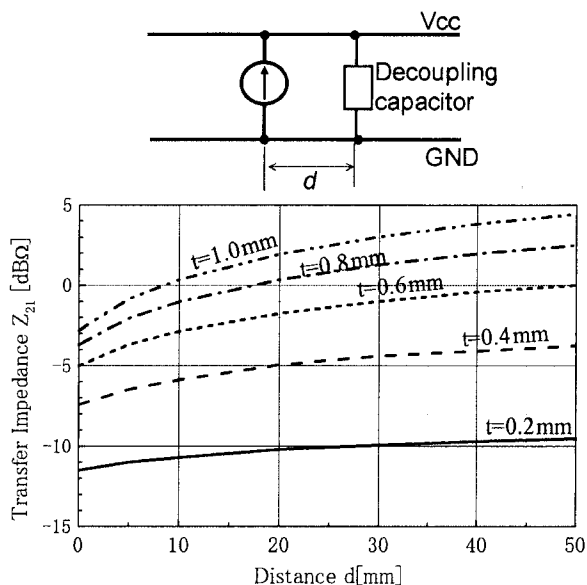


Figure 5. Dependence of transfer impedance Z_{21} on the distance between the current source and the decoupling capacitor at 300MHz

between t and d_{acpt} is introduced when the threshold of voltage increasing is set within 3dB based on the levels of $d=0$. Figure 6 shows the relation between t and d_{acpt} to satisfy the threshold. This relation is approximately represented by a function:

$$d_{acpt} = Kt^{-1.33} \quad [dB] \quad (7)$$

K is constant which depends on a target for EMI suppressing level. When the threshold level is set by 3dB, K becomes 8.0. This simple form is very useful for practical PCB design about allocations of decoupling capacitors

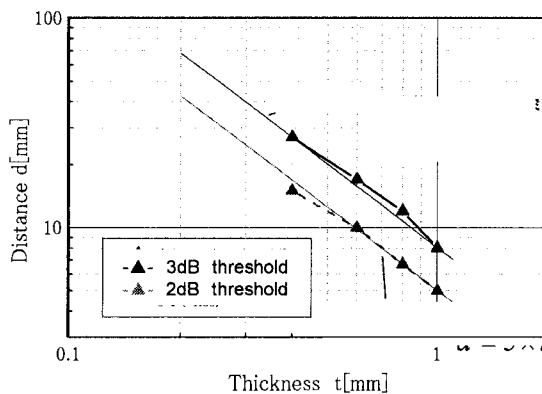


Figure 6. Relation between the space separating the power and ground planes and distance from a via to the decoupling capacitor to make the voltage disturbance within certain thresholds

5. Conclusion

The dependence of voltage disturbances between the power-distribution planes due to allocating capacitors near by the via is investigated. The via penetrating through the power and ground planes gives a rise to voltage disturbance between these two planes. Voltage reduction effectiveness to allocate the decoupling capacitor is evaluated quantitatively by using the equivalent circuit model. Calculated results have showed the effect of decoupling capacitor is better as the distance between the via and the capacitor is shorter and the space between power-distribution planes is smaller. From obtained results, a simple analytical formulation has been introduced about the relation between the plane space and the distance from the via to the decoupling capacitor in order to allow the disturbances within certain threshold levels. This guide is available for achieving practical EMC PCB design.

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