USING CAVITY-MODES FOR MODELING OF VIA-CONNECTED POWER BUS STACKS IN MULTILAYER PCBS

Zhi Liang Wang, Osami Wada, Takahiro Yaguchi*, Takuya Miyashita, Yoshitaka Toyota and Ryuji Koga

Faculty of Engineering, Okayama University, Japan

* NEC Informatec Systems, Ltd, Japan

E-mail: zlwang@cne.okayama-u.ac.jp

Abstract: Power bus noise problem has become a major concern for both EMC engineers and board designers. A fast algorithm, based on the cavity-mode model, was employed for analyzing resonance characteristics of multilayer power bus stacks interconnected by vias. The via is modeled as an inductance and its value is given by a simple expression. Good agreement between the simulated results and measurements demonstrates the effectiveness of the cavity-mode model, together with the via model.

Key words: Power bus stack and modeling, Cavity-mode model, Via interconnect, EMI

1. Introduction

Power bus resonance in multilayer printed circuit boards (PCBs) not only cause radiated emission as EM interference (EMI), but also affect ground bounce due to switching noise in a digital system. As a result, power bus noise problem has become a major concern for both EMC engineers and board designers. Power bus resonance characteristics have been investigated with various models or approaches. The full cavity-mode model [1] is one of the useful models and can be employed for fast simulation. The fast algorithm is attributed to a closed-form expression for the impedance Z-matrix of the power/ground planes, which is in the form of a fast converging single series [2-4]. This is assuming that the pattern of the power/ground planes is rectangular. Combined with the segmentation method, the fast algorithm has been extended to various power bus geometries [5,6].

Multilayer power bus stacks, viz., using multiple power/ground plane sets for dc power distribution, are common scenarios in multilayer PCB designs. The solid power and ground planes are typically of appreciable electrical extent, and may function as radiating microstrip-patch antennas or effective coupling paths at high frequencies. One recent study of power-bus geometries with multiple power/ground plane pairs could be found in [7], where the finite-difference time domain (FDTD) method was used for modeling, and the effect of ground plane stitching by vias on radiated EMI was primarily discussed. The work presented herein focuses on modeling of via-interconnected power-bus stacks using the fast algorithm based on the cavity-mode model. It was found that the via inductance affects significantly the resonance characteristics of a via-connected power-bus stack, thus estimating the via inductance value is quite important for achieving accurate simulation.

2. Full Cavity-Mode Model

The full cavity-mode resonator model is an analytical description of the impedance matrix (Z-parameters) of an unloaded power/ground plane structure (a bare board). For a rectangular power/ground plane structure with length a and width b, an expression for fast calculation of the transfer impedance between two ports on the power/ground planes was developed as follows [2]:

$$Z_{ij}^{(\mathrm{rec})} = \sum_{n=0}^{\infty} \frac{\omega\mu_d h a}{\mathrm{j}\,2b} C_n \cos(k_{yn} y_i) \cos(k_{yn} y_j) \times \mathrm{sinc}^2(k_{yn}\mathsf{w}) \frac{[\cos(\alpha_n x_-) + \cos(\alpha_n x_+)]}{\alpha_n \sin\alpha_n} \quad (1)$$

where $\mathrm{sinc}(x) = \sin(x)/x$, $k_{yn} = n\pi/b$, $\alpha_n = a\sqrt{\kappa^2 - k_{yn}^2}$, $x_\pm = 1 - (x_i \pm x_j)/a$, (x_i, y_i) and (x_j, y_j) are the coordinates of the center of the ith and jth ports in the x- and y-directions, respectively, w is much less than the wavelengths of interest and represents the port half width, h is the dielectric thickness between the power/ground planes, ω is radian frequency. For simplicity it is assumed here that the port sizes in the x- and y-directions for the ith and jth ports are the same. The constant C_n is assigned as $C_n = 1$ if $n = 0$,

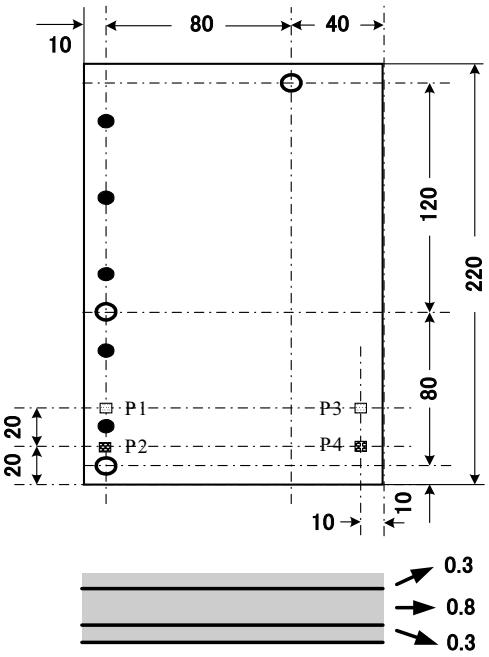

Fig.1: Layout and stack-up of the test board 1 with 5 vias interconnected two power planes. All dimensions are in millimeters (mm).

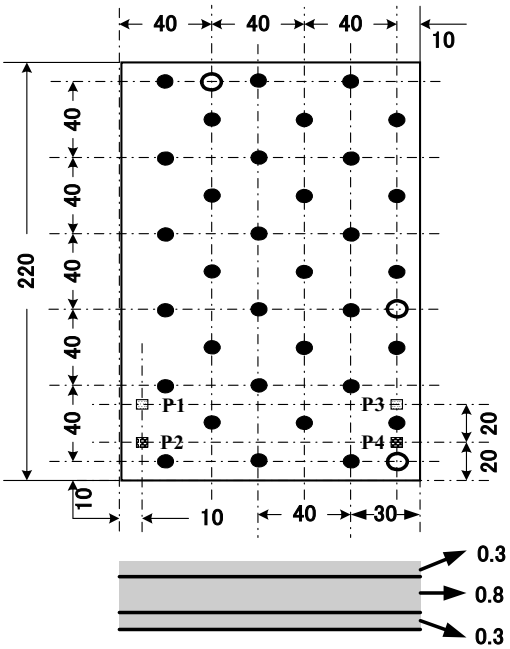

Fig.2: Layout and stack-up of the test board 2 with 33 vias interconnected two power planes. All dimensions are in millimeters (mm).

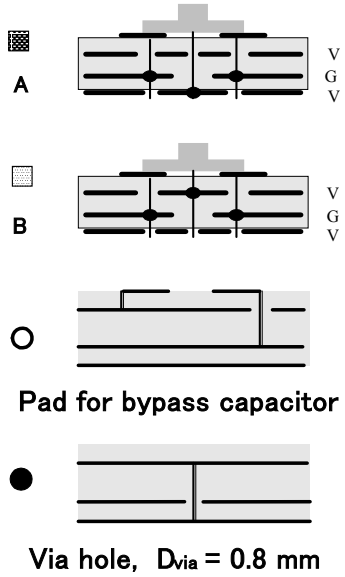

Fig.3: Side views of the SMA connectors and interconnecting vias.

and $C_n = 2$ if $n \neq 0$, and the constant $\mathrm{j} = \sqrt{-1}$. The complex transverse wavenumber κ is obtained as $\kappa^2 = \omega^2 \mu_d \varepsilon_d - \mathrm{j}2\omega\varepsilon_d Z_S/h$, where μ_d and ε_d are the permeability and permittivity of the dielectric, and Z_S represents the surface impedance of the power/ground conductors. To obtain sufficiently accurate resonance characteristics, both the dielectric and conductor losses must be taken into account. The dielectric loss naturally appears in the imaginary part of the dielectric constant ε_d, while the conductor loss is incorporated into the surface impedance Z_s of the conductors.

When the original double summation of the power bus impedance is reduced to the single summation, an error appears due to the approximation [4]. It is found that the error can be disregarded for the transfer impedance (Z_{ij} between two ports at different locations) but has to be considered for the self input impedance (Z_{ii} between two ports at the same location). A numerical study shows that the error for the self input impedance is merely proportional to the spacing h between the power/ground planes and regardless of other board dimensions and parameters. Moreover, the error appears as an overestimate on the inductive component and can be compensated by substracting $\mathrm{j}\omega L_h$ when calculating the self input impedance Z_{ii} using the expression (1). The numerical fitting suggested that $L_h = 0.139 * h$ (nH) with h in millimeters.

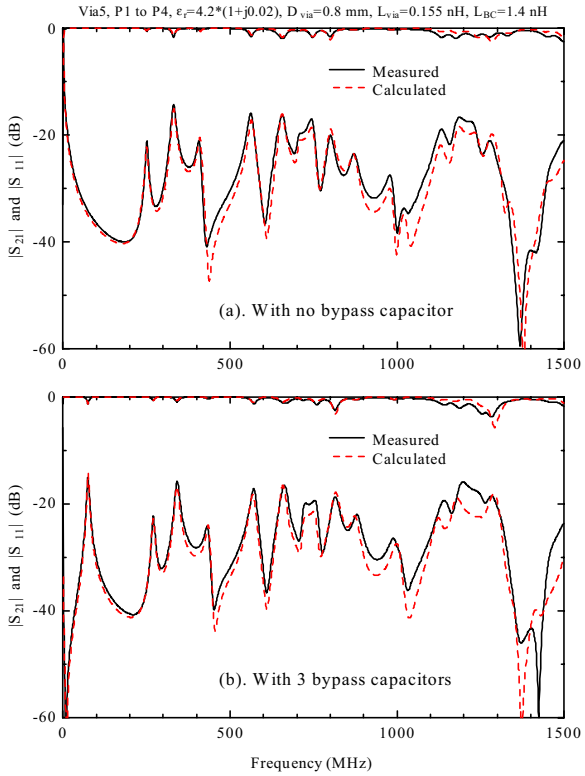

Fig.4: Cavity-mode model simulated and measured $|S_{11}|$ and $|S_{21}|$ for the test board shown in Fig.1. The number of vias used for interconnecting the two power planes is 5. (a) No bypass capacitor mounted, and (b) 3 bypass capacitors mounted.

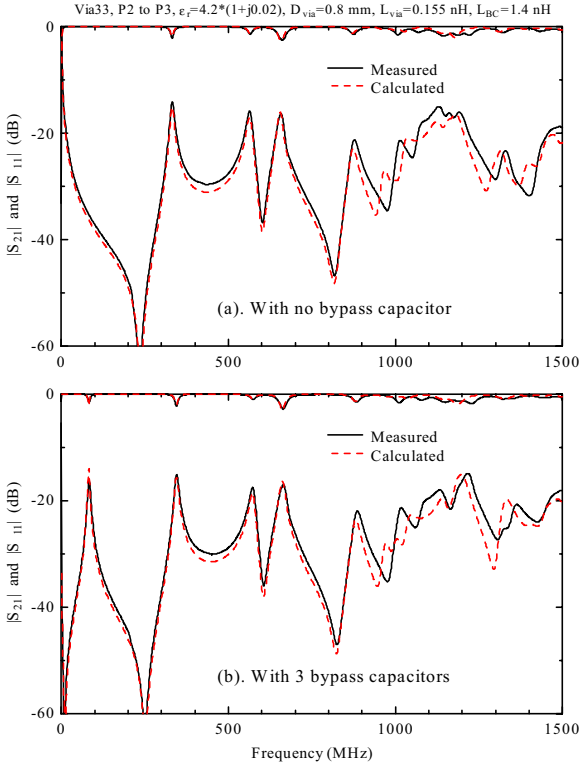

Fig.5: Same as Fig.4 but for the test board shown in Fig.2.

3. Results and Comparisons

A multilayer power bus stack can be treated as power bus cavities interconnected by vias. The impedance matrix for each power bus cavity can be calculated with the aforedescribed cavity-mode model for the rectangular geometry or a combination of the cavity-mode model and the segmentation method for more complicated geometries [5,6]. The interconnect via is commonly modeled as an inductance [8] with its value given by

$$L_{\text{via}} = \frac{\mu_0\, l}{2\pi} \ln\left(1 + \frac{4\, l}{\pi\, D_{\text{via}}}\right) \quad \text{(Henries)} \qquad (2)$$

where l is the length and D_{via} the external diameter of the via. The only difference between the expression (2) and the one in [8] is the unit term inside the logarithm and it is introduced to avoid a negative inductance as l is less than $(\pi/4)\, D_{\text{via}}$.

The layout and stack-up of the tested boards are shown in Figs. 1 and 2. The side views of the SMA connectors and the vias interconneting the top and bottom metal planes are shown in Fig. 3. Both boards have a PWR-GND-PWR layer stack-up and the pads for mounting SMT bypass capacitors. The board 1 contains 5 vias and the board 2 contains 33 vias interconnected the top and bottom power planes. Since a portion of the vias pass through a power/ground pair and another portion of the vias pass through another power/ground pair, the total via inductance should be the sum of the contributions from these two portions, each is determined by the expression (2).

The evaluated via inductance value is $L_{\text{via}} = 0.155$ nH for the via diameter $D_{\text{via}} = 0.8$ mm. Using this inductance value, the overall Z-matrix are derived and calculated in a similar way as being done in [5]. The overall scattering S-parameters can easily be obtained from the overall Z-matrix. In the cavity-mode modeling, the relative complex dielectric constant was assumed to be $\varepsilon_d = 4.2*(1.0-\text{j}\,0.02)$ for FR-4 over the frequency range considered. Each bypass capacitor was modeled by an ideal capacitor in series with a resistor (ESR) and an inductor (ESL). The nominal capacitance used was 0.1 μF, the parastic resistance was 20 mΩ, and the parasitic inductance of the capacitor was

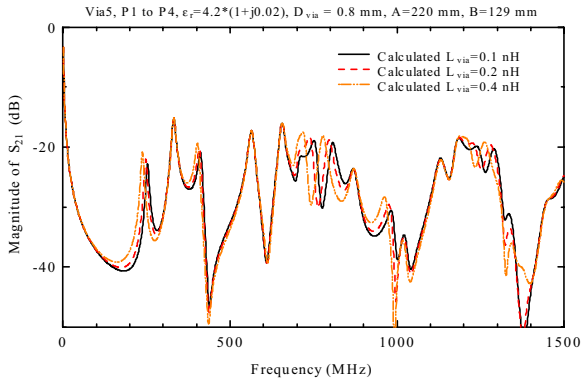

Fig.6: Cavity-mode model simulated $|S_{21}|$ for the test board shown in Fig.1 with different via-inductance values.

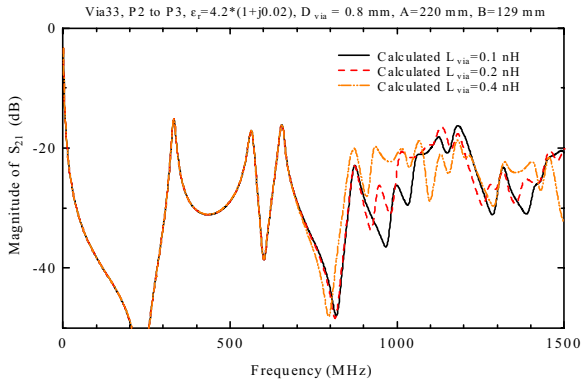

Fig.7: Same as Fig.6 but for the test board shown in Fig.2.

taken to be 1.4 nH, including both the contributions from its connecting vias and traces.

A two-port S-parameter measurement was conducted using $HP8753D$ network analyzer with the two test boards, for the two cases without any capacitor and with 3 bypass capacitors mounted on the boards. The measued and calculated results of $|S_{11}|$ and $|S_{21}|$ are plotted in Figs. 4 and 5 for the two test boards, respectively. Good agreement was achieved for both boards and both the cases with and without bypass capacitors. The simulated results of $|S_{21}|$ with different via inductance values are shown in Figs. 6 and 7 for the two boards. The results indicate that the via inductance value and the number of the vias affect significantly the frequency response of a via-connected power-bus stack.

4. Conclusions

Multilayer power-bus stacks have been modeled using the fast algorithm based on the full cavity-mode model and an inductance model for the interconnecting vias. Good agreement between the modeled results and measurements demonstrated the effectiveness and accuracy of the modeling. The via inductance value was found to be quite important for achieving accurate simulation.

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