Analysis of Power/Ground-Reference Planes for EMC & Functionality

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Abstract
Analysis of decoupling capacitors on high speed print circuit boards is often confusing. In order to reduce this confusion, we consider the two main purposes of decoupling capacitors: EMC and functionality. These two purposes require a different analysis technique in order to insure optimum design for each purpose. An important part of the decoupling capacitor performance is the inductance associated with the mounting of this capacitor.

Keywords
Decoupling, Capacitors, EMC, Time-Limited Analysis, Steady-State Analysis

Introduction
There are two primary purposes for using decoupling capacitors between power and ground-reference planes. The first purpose is for functionality, that is, the decoupling capacitor is a charge storage device, and when the IC switches state and requires additional current, the local decoupling capacitor is intended to supply this current through a low inductance path. If the capacitor is able to supply all of the current required by the IC, then the voltage at the IC power pin remains constant at the desired supply voltage. If the capacitor is not able to supply the required current, then the voltage at the IC power pin is lowered temporarily until adequate current is provided, or until the need for the current is ended. If sufficient current is not provided, the IC may experience a functional failure. It is important, therefore, to locate decoupling capacitors close to the demand for current (IC power pins) in order to minimize the loop inductance of this current path. It is also important to provide a low impedance path from the IC power pins to the power plane, from the IC's ground-reference pins to the ground-reference plane, and from the decoupling capacitor to the power and ground-reference planes. Capacitors used for this charge delivery function must have low equivalent series resistance (ESR) and low equivalent series inductance (ESL).

The second purpose for decoupling capacitors is to reduce the noise injected into the power and ground-reference plane pairs and thus reduce the EMI emissions from the edge of the circuit board. For example, the edge of a board may be near the seams of the metal enclosure or near an air vent area, allowing this noise to escape the enclosure. Another possibility is for this noise to couple onto I/O connector pins and be directly coupled out of the metal enclosure through any of the cables. There are a variety of coupling mechanisms that are possible once this noise is created.

The source of this injected noise can be either: (1) the temporary lowering of voltage at the IC pin power pin when sufficient current is not provided from the decoupling capacitor (creating a short duration voltage pulse), or (2) the noise signal injected between the power and ground-reference planes due to an intentional current (e.g. a clock signal, bus signals, or other fast switching signals) transitioning to different PC board layers on a via. Measurements on active ICs have shown that the relative magnitude of typical power and ground-reference plane noise sources are approximately equivalent. [1]

Time-Limited Analysis
As stated earlier, one of the main functions for decoupling capacitors is to provide charge to the ASIC/IC. Typically, the ASIC/IC switches from a high impedance to a low impedance very quickly. Therefore, the demand for current changes very fast, and this fast current draw results in high frequency components of the current. Whenever high frequency current is required, the inductance of the current path becomes the limiting factor of how rapidly this current can be provided.

There are a number of parallel current paths to consider. The most obvious is the individual decoupling capacitors. Each capacitor will have its own inductive current path. The separation between the capacitor pins (L_{cap}), the separation between the ASIC/IC's pins (L_{IC}), and the distance between the capacitor and ASIC/IC ($L_{apparent}$) [2] will all contribute to the overall inductance path for this current. Figure 1 shows an example for a single capacitor case.

In addition to this current source from each capacitor, the distributed capacitance between the two planes serve as an additional current source. However, we cannot consider these two planes as a traditional capacitor where the entire area between the planes serve (equally) to provide charge to the ASIC/IC. These two planes should be considered as a number of very

small capacitors, each providing a small amount of charge, and each with a different loop inductance. Figure 2 shows an example of this distributed capacitance model, where the overall capacitance between the plates is broken in to many individual, smaller, capacitors

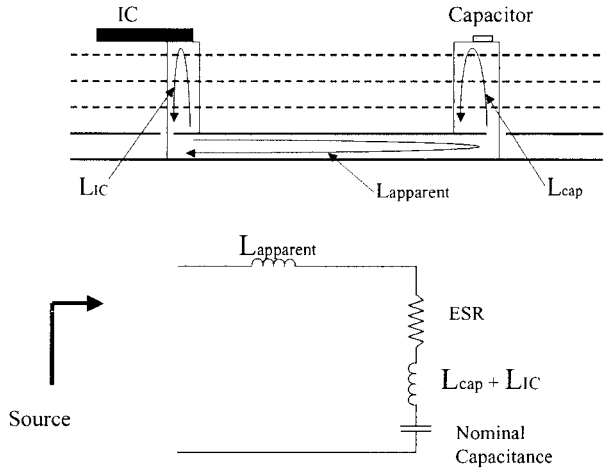

Figure 1 Current Loop Illustration for IC and Decoupling Capacitor

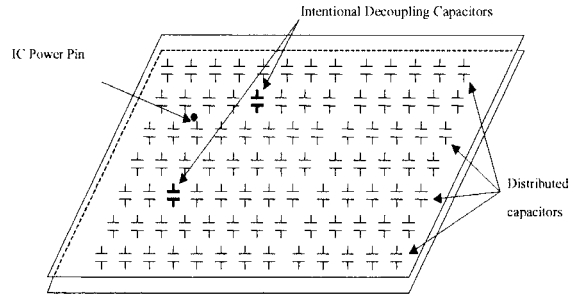

Figure 2 Distributed Capacitance Between Planes

With this distributed capacitance model for two parallel planes, it is clear that the displacement current through each of the distributed capacitors will be different, since the loop inductance for each path will be different. The effect of the loop inductance will naturally be larger at higher frequencies where the path impedance for distributed capacitors at further distances will be significantly greater.

Figure 3 shows an example of the displacement current between two parallel planes at 500 MHz when a 'perfect capacitor' (shorting via) is placed approximately 1 cm from the ASIC/IC power pin. The amount of displacement current decreases very fast as distance to the portion of distributed capacitance increases.

In order to properly analyze the current/charge delivery as the ASIC/IC switches from a high impedance to a low impedance, the time delay from both the individual capacitors, and the distributed capacitance (with varying displacement current) must be considered. The combination of the conductive current path between the planes and the IC and capacitor, and the displacement current path results in this 'apparent inductance'.

Traditionally, frequency domain analysis (used to find an impedance of the power/ground-reference planes) results in a steady-state solution which does not allow for the individual time delays from all the various portions of capacitance available. A steady-state solution assumes that all time delays are equal, and that current can travel from all locations on the PC board within the time required. However, since the ASIC/IC only requires current for a short time, current traveling from (inductively) distant portions of the board will not arrive before the demand for current is done (for that cycle). This charge delivery analysis must be performed in the time domain, so that these time delays can be included. Alternatively, if a frequency domain analysis is preferred, then a time-limited apparent inductance must be used in place of traditional parallel plate capacitor analysis.

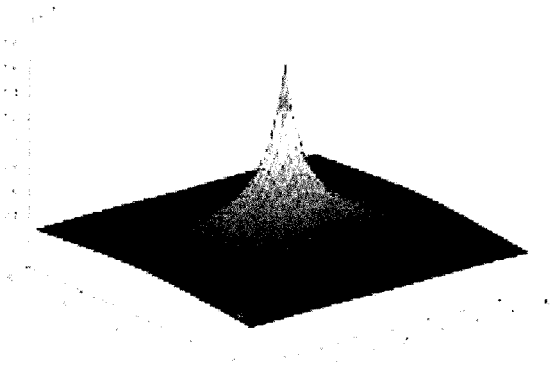

Figure 3 Distributed Displacement Current Between Planes at 500 MHz with Shorting Via at 1cm distance from source

Steady-state analysis for EMC

The second concern regarding decoupling of parallel power/ground-reference planes is the possibility that noise created at the ASIC/IC power pins may propagate to the edge of the board, and radiate from the edge of the board through shielded enclosure apertures, etc. This concern means that the transfer function from the noise source to the edge of the board (or other observation point) is the important parameter.

Also, since EMI emissions are often enhanced when structures become resonant, a frequency domain (steady-state) analysis is appropriate.

This transfer function analysis will include the effects of structure resonance, and will show the relative amplitude of the amount of noise from the source that arrives at the edge of the board. Figure 4 shows an example measurement of this transfer function from the center to the corner of a 10" x 12" printed circuit board with a 35 mil separation between planes and no decoupling capacitors. Note that at frequencies above ~ 450 MHz, the resonant peaks are not attenuated by the addition of capacitors. The physical size-based resonances will begin at frequencies where the cavity created between the two metal plates is one-half wavelength (or integer multiples of half wavelengths). The electric field is assumed to not vary in the z-direction (normal to the plates). This size-based resonant frequency can be found from (1). The actual resonant frequencies on the board will be defined by (1) when there are no decoupling capacitors. Adding decoupling capacitors will change the resonant frequencies, however, (1) will serve as a rough indication of where resonant frequencies will begin.

$$f_{mn} = \frac{1}{2\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \qquad (1)$$

where:
m and n are the mode number (only 1 can be zero)
and a and b are the dimensions of the PC board.

When decoupling capacitors are distributed evenly across the entire PC board they are considered *global* decoupling capacitors. They are not intended to provide decoupling to any specific IC, but instead to the entire PC board. The number of decoupling capacitors and the density of their placement is important to maintain a low transfer function across the board.

For the following example, all the capacitors used are 0.01 uF SMT (0805 size). To illustrate the effect of different capacitor densities, the example 25cm x 30cm board was populated with 25, 50, or 99 (approximately every two centimeters) capacitors. In each case the capacitors were evenly distributed across the board. The results and conclusions for the various source and observation locations were consistent at high frequencies. While the individual resonances might shift slightly, the overall envelope of the S_{21} transfer function is not affected by the shift in resonant frequency.

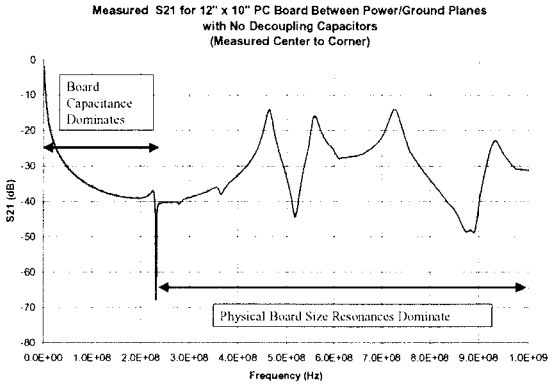

Figure 4 Example Transfer Function From Center to Corner of Test Board with No Capacitors

As can be seen in Figure 5, adding capacitors lowers the S_{21} transfer function in the lower frequency ranges (below 200 – 400 MHz). At higher frequencies, the overall envelope for the S_{21} transfer function decreased only very slightly (despite a resonant frequency shift) as more capacitors were added.

The maximum number of capacitors populated was 99 distributed capacitors, representing one capacitor every two square centimeters across the PC test board. This is a much more dense capacitor placement than is often possible with real products. Even with this dense capacitor distribution, the decoupling transfer function was only improved below approximately 400 – 600 MHz. This frequency limitation is due to the connection inductance of the vias, traces, pads, etc., which are inherent in the capacitor attachment.

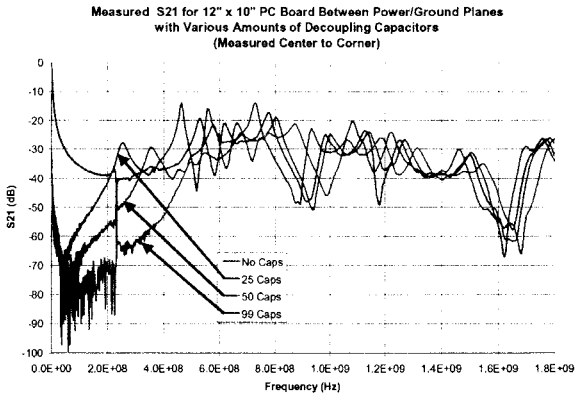

Figure 5 Transfer Function From Center to Corner of Test Board with Various Number of Capacitors

Decoupling Capacitor Via Placement

It is clear from the previous discussions that the inductance associated with the decoupling

capacitors must be minimized in order for these capacitors to be effective. Unfortunately, inductance is one of the least understood parameters within electrical engineering.

The first-order effect that governs inductance is the loop area. Therefore, the loop area associated with the decoupling capacitors and the power/ground-reference planes must be minimized in order to minimize inductance. Figure 6 shows a diagram of this loop area including the distance between the capacitor pads and vias, as well as the distance from the surface capacitor to the planes.

Since the loop area dominates this inductance, then the layout of the vias associated with the decoupling capacitor are very important. Long traces that connect between decoupling capacitor pads and the associated via are obviously undesirable. However, depending on the size of the decoupling capacitor, and the manufacturing technology used on a particular printed circuit board, the loop area (and therefore the inductance), can be minimized further. Figure 7 shows a few possible via/pad configurations.

Summary

Design and analysis of decoupling capacitor performance requires consideration of the two primary purposes for these capacitors: EMC and functionality. EMC analysis is usually a steady-state analysis of the board resonances and the transfer function from a possible noise source location to the edge of the board (or other susceptible location). Functionality analysis must include a time-limited analysis to account for the local effects of the displacement current and the decoupling capacitors.

For both types of analysis, the inductance associated with the loop area of the decoupling capacitor is important. The distance between the ASIC/IC's power pins and the decoupling capacitor is usually a major part of this loop area. The spatially-varying displacement current between the planes, and the difference is conductor size (planes and vias) must be included to ensure an accurate estimate of the decoupling capacitor's performance. In this work, we use the term 'apparent inductance' to include these effects.

References

[1] Wei Cui, *Modeling and Design of DC Power Bus Interconnects, Segmentation, and Signal Via Transitions in Multi-Layer Printed Circuit Boards using FDTD and a Mixed-Potential Integral Equation Approach with Circuit Extraction*, PhD, May 2001.

[2] B. Archambeault, J. Wang, S. Connor "Power and Ground-Reference Plane Impedance Determination As Decoupling Capacitor Distance Increases," IEEE International Symposium on EMC, August 2003

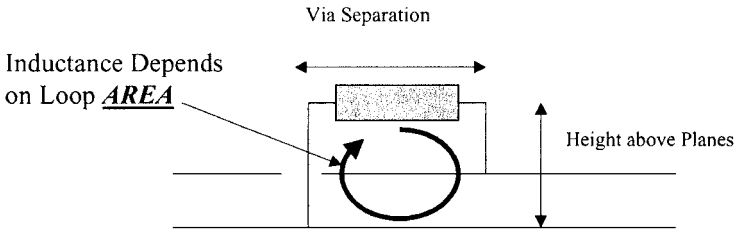

Figure 6 Loop Area Associated with Decoupling Capacitors

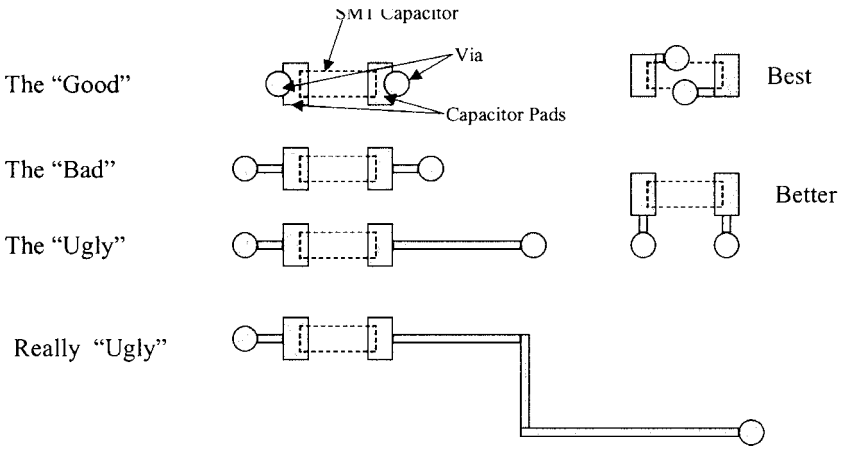

Figure 7 Examples of Decoupling Capacitor Via Placement