COMMON-MODE CURRENT DUE TO TRACE AND SLIT IN GROUND PLANE AND EFFECT OF GUARD BAND

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Abstract: The common-mode (CM) current due to a trace near the PCB edge and across a slit in the ground plane is treated experimentally and by FDTD modeling. The width of the slit was 2 mm and the length was varied. The effect of a guard band with a 5 mm width is also discussed. As the slit length becomes longer, $|S_{21}|$ related to the CM current significantly increases. When the slit penetrates to the center of PCB, $|S_{21}|$ becomes almost the same value. As the guard band functions as one of the return paths, it is effective to suppress the CM current when a trace is nearer to the guard band.

Keywords: common-mode current, EMI, PCB, slit, guard band

1. Introduction

An electromagnetic interference (EMI) problem is typically comprised of a noise source, EMI antenna, and a parasitic coupling path between the noise source and EMI antenna. The increased impedance of a finite reference (ground) plane in a printed circuit board (PCB) results in a current-driven noise source, which may drive the EMI antenna [1], [2].

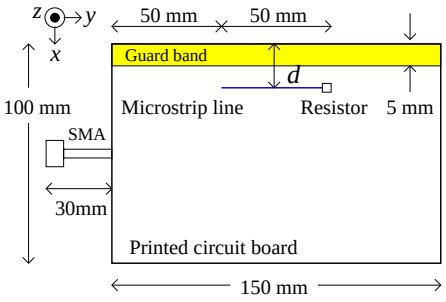
In circuit design, slits (or gaps) are often used in ground planes, which is needed to isolate analog and digital circuit sections. It has been reported that slits intensify EMI radiation, because of an increase in the partial inductance of the reference structure [3], [4]. However, a design guidelines for suppression of the EMI radiation remain unclear. It is therefore necessary to accumulate a lot of data for the common-mode (CM) current, impedance, and EMI coupling paths in PCBs with a slit, and make suggestion for the design guideline.

So far, the authors have discussed the CM current of an EMI antenna, a noise source that results from the finite impedance of the PCB ground plane to determine the necessary "keep-out" area on the board periphery for high-speed trace routing [5]. And the suppression effect of a guard band on CM current due to a trace near a PCB edge has been studied [6].

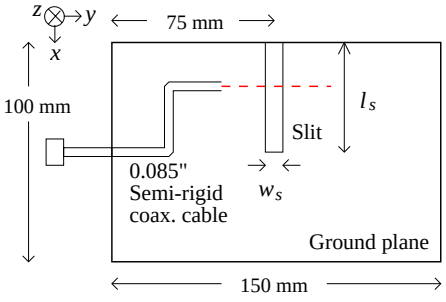
In this study, the CM current due to a trace near the PCB edge and across a slit in the ground plane is treated experimentally and by FDTD modeling. And the effect of a guard band to suppress the CM current is discussed.

2. PCB Geometry

The geometry of a PCB layout is illustrated in Fig. 1. The PCB had two layers, with the upper layer for a signal trace, and the lower for the 100 mm×150 mm ground plane. The trace, with 0.51 mm width and 50 mm length, was centered lengthwise on a 1.09 mm thick dielectric substrate with ε_r=4.5. Different configurations in which the distance d between the trace and the PCB edge [5], as shown in Table 1, were prepared. The characteristic impedance of the trace of the 'center' case and the case where the trace were near a PCB edge ($d \leq$6.35 mm [250 mils.]) was approximately 90 and 98 Ω by TDR measurement, respectively. In order to make the impedance matching, the trace was terminated with 91 and 100 Ω SMT resistors, as shown



(a) Top view



(b) Bottom view

Fig.1 Geometry of the PCB layout.

Table 1 PCBs under test.
(d: distance between the trace and the PCB edge)

	d [mm]	Guard band width [mm]	Terminating resistor [Ω]
d50	1.27	–	100
d250	6.35	–	100
d250GB		5	
d400	10.16	–	91
d400GB		5	
d600	15.24	–	91
d600GB		5	
center	49.75	–	91

Table 2 The size of slit in the ground plane.

w_s	2 mm
l_s	10, 30, 50, 70, 90 mm

in Table. 1. The length l_s of the slit in the ground plane was varied and the width w_s was 2 mm, as shown in Table 2. The cases with l_s=30 mm and the 'd600' case are used only for FDTD modeling.

PCBs of the same configuration with a guard band (GB) of width 5 mm [6], was also prepared, as shown in Table 1. As the guard band, copper tape was used and connected along an adjacent edge of the ground plane to the upper layer along the side of the PCB.

3. Experimental Method

The CM current on the outer shield of the feed cable was measured with a current probe (Fischer F-2000), and a network analyzer (Agilent E8358A), as shown in Fig. 2 [5]. The current probe is mounted adjacent to the aluminum plate and encircled the feeding cable. A ferrite sleeve (100 Ω at 100 MHz) is mounted around the probe connector to reduce coupling to the current probe. A 500 mm×500 mm aluminum plate was used to isolate the PCB from the cable dressing leading to the network analyzer. The $|S_{21}|$ with Port 1 and Port 2 was measured in the frequency range from 50 MHz to 1 GHz. Port 1 was connected to the 0.085" coaxial cable to drive the signal line, and Port 2 was connected to the current probe. Measured result in each experiment was averaged 1024 times.

The calibration of the network analyzer and removal of the frequency response of the current probe, and the relationship between $|S_{21}|$ and the CM current are described below [5]. A copper ring which is tightly wrapped around the probe was used for the calibration. The current I_1 in the copper ring at low frequencies is given by $I_1 \approx V_S/50$, where V_S is the RF source voltage of the network analyzer, and

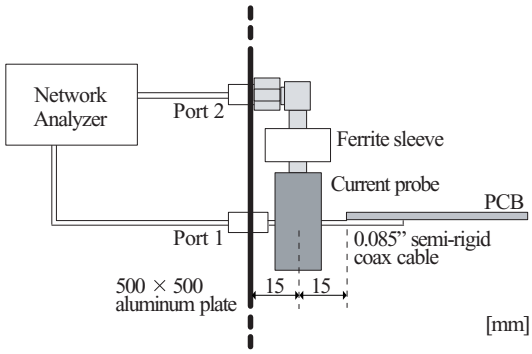


Fig.2 Experiment setup for CM current measurement.

the source impedance of the network analyzer is 50 Ω. The voltage at Port 2 is given by $V_2^- = 50I_2$, where I_2 is the current sensed by the current probe. The currents in Port 1 and Port 2 are related by the frequency response of the current probe $H_{pr}(f)$, therefore $I_2 = H_{pr}(f)I_1$. As the source impedance is matched to the characteristic impedance of the cable, the voltage at Port 1 is given by $V_1^+ = V_S/2$. Then $|S_{21}|$ before calibration is given by

$$|S_{21}| = |\frac{V_2^-}{V_1^+}| = |\frac{50H_{pr}(f)V_S/50}{V_S/2}| = |2H_{pr}(f)|. \quad (1)$$

Therefore, the calibration procedure removes the factor $2H_{pr}(f)$, and the relationship between $|S_{21}|$ and the CM current I_{CM} is given by

$$|S_{21}| = |\frac{50I_{CM}}{V_S}|. \quad (2)$$

This is used to compare between the experimental and numerical results.

4. FDTD Modeling

The FDTD method [7] is used for simulating CM current on the PCB. PMLs (Perfectly Matched Layers), eight cells deep, were used as the absorbing boundary condition. The cell size was Δx= 0.254, Δy=1.0 and Δz=0.546 mm. The total computational domain was 491×232×183 cells, in the x,y, and z dimensions, respectively. The time step was Δt=0.635 ps from the Courant stability condition [7]. The PCB substrate was modeled as a dielectric two cells deep with ε_r=4.5. An SMT resistor was modeled as a one cell lumped element in the PCB substrate. The trace was modeled as a PEC (Perfect Electric Conductor), two cells wide. Th ground plane and aluminum plate were also modeled as a PEC. The aluminum plate used in the experiments was included as an infinite ground plane. A sinusoidally modulated Gaussian pulse was used as the source with a resistance of 50 Ω. The CM

current was calculated by the loop integral around the cable at the current probe position.

To shorten the calculation time, the vector and parallel computation method for a super computer (NEC SX-7) was used in FORTRAN 90.

5. Results and Discussion

5.1 CM Current when Varying Slit Length

Measured and calculated $|S_{21}|$ related to the CM current of the 'center', 'd50', and 'd250' cases when varying the slit length l_s are shown in Fig. 3 to 5, respectively. There is a good agreement between measured and calculated results, although the difference is in approximately 4 dB when the slit length is longer. In all of cases, $|S_{21}|$ significantly increases, as the slit length becomes longer. The difference between $|S_{21}|$ of the cases with l_s= 90 mm and without slit is approximately 30 dB. However, the difference between the 'center' cases with l_s=30 mm and without slit is in approximately 3 dB. In this case, the trace is not across a slit. The first peak is at approximately 270 MHz, and is related to the total length of the PCB model, 28 cm (PCB width and length, and cable length), which is comparable to $\lambda/4$. And the second resonance is slightly shifted to lower frequency as the slit length becomes longer.

Comparison between $|S_{21}|$ of the cases with l_s= 50 mm where the trace position is different is shown in Fig. 6. $|S_{21}|$ of all cases except 'center' is almost the same. In the cases with l_s=70 and 90 mm, $|S_{21}|$ is also the same. In the cases with l_s=30 mm, the difference between the 'd50' and 'd600' case is approximately 4 dB. These results indicate that the effect of the trace position is small for an increase of the CM current when the slit length is much longer than the distance d, i.e. the slit penetrates across to the center of PCB.

5.2 Effect of Guard Band

Measured and calculated $|S_{21}|$ of the 'd250' case

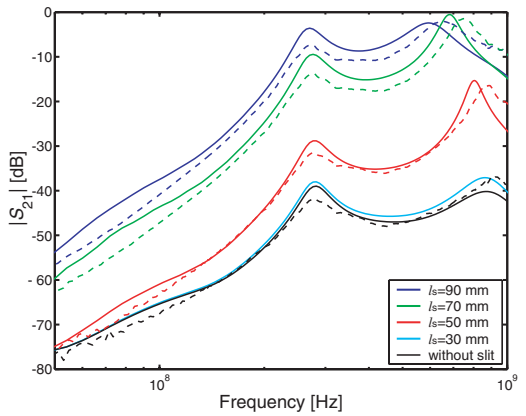


Fig.3 $|S_{21}|$ related to CM current of the 'center' case when varying the slit length (Solid line: calculated result, Dashed line: measured result).

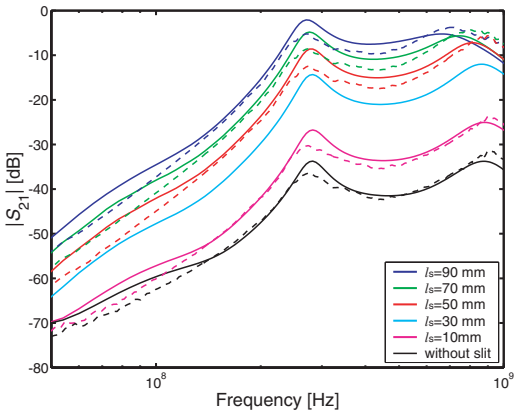


Fig.5 $|S_{21}|$ related to CM current of the 'd250' case when varying the slit length (Solid line: calculated result, Dashed line: measured result).

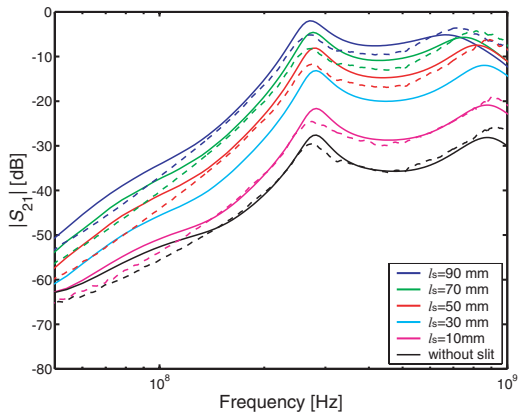


Fig.4 $|S_{21}|$ related to CM current of the 'd50' case when varying the slit length (Solid line: calculated result, Dashed line: measured result).

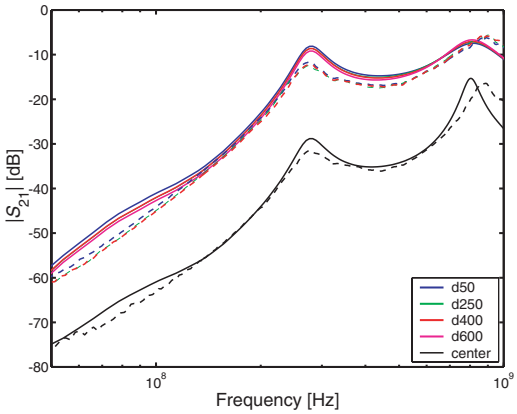


Fig.6 Comparison between $|S_{21}|$ of the cases with l_s=50 mm (Solid line: calculated result, Dashed line: measured result).

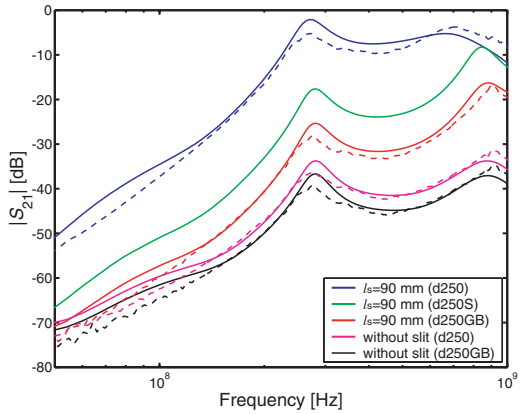


Fig.7 The effect of a guard band in the 'd250' case with l_s=90 mm (Solid line: calculated result, Dashed line: measured result).

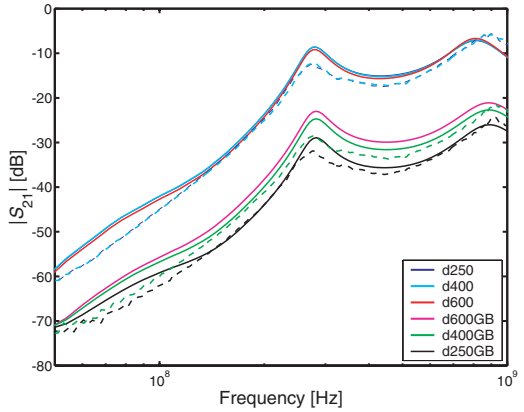


Fig.8 Comparison of the effect of a guard band in the case with l_s=50 mm (Solid line: calculated result, Dashed line: measured result).

with a guard band (GB), 'd250GB', with l_s=90 mm are shown in Fig. 7. There is a good agreement between measured and calculated results. $|S_{21}|$ of the case with GB is significantly smaller than that without GB. In Fig. 7, 'd250S' shows the calculated result in the case where the slit was shorted at the PCB edge by a thin wire in the FDTD modeling. $|S_{21}|$ decreases approximately 15 dB. This indicates that a GB becomes one of the return paths. However, $|S_{21}|$ of the case with a GB is approximately 7 dB smaller than the 'd250S' case.

Comparison of the effect of the GB in the cases with l_s=50 mm is shown in Fig. 8. The effect of a GB to suppress the CM current is larger, when the trace is nearer to the GB. In the cases with different slit length, this tendency is identically observed. These results indicate that a GB may be effective to suppress the CM current.

6. Conclusion

The CM current due to a trace near the PCB edge and across a slit in the ground plane was discussed experimentally and by FDTD modeling. The slit length was varied. The effects of the varied slit length and a guard band with a 5 mm width was discussed. As the slit length becomes longer, $|S_{21}|$ related to the CM current becomes significantly larger. When the slit length is much longer than the distance between a trace and the PCB edge, $|S_{21}|$ becomes almost the same value. A guard band becomes one of the return paths, and then is effective to suppress the CM current.

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