IEICE Proceeding Series

# Dynamically Reconfigurable Switched-Capacitor DC-DC Converters

Mian Li, Michael Peter Kennedy

Vol. 1 pp. 280-283
Publication Date: 2014/03/17
Online ISSN: 2188-5079

2012 International Symposium on Nonlinear Theory and its Applications
NOLTA2012, Palma, Majorca, Spain, October 22-26, 2012

# Dynamically Reconfigurable Switched-Capacitor DC-DC Converters

Mian Li[†,‡] and Michael Peter Kennedy[†,‡]

†Department of Electrical and Electronic Engineering, University College Cork
Western Road, Cork, Ireland, and
‡Tyndall National Institute
Lee Maltings, Dyke Parade, Cork, Ireland
Email: peter.kennedy@ucc.ie

**Abstract**—Switched-capacitor DC-DC converters will become more attractive for power-supply-on-chip applications if they can provide variable output voltages. This paper describes how the topology of a SC DC-DC converter can be reconfigured dynamically in order to realize this goal. We describe a three-stage converter with coarse and fine control of the output voltage.

## 1. Introduction

DC-DC converters are widely used in portable electronics. Traditional, DC-DC converters have used switched L-C (SLC) topologies, such as the buck converter shown in Fig. 1. The input voltage is applied between the terminals

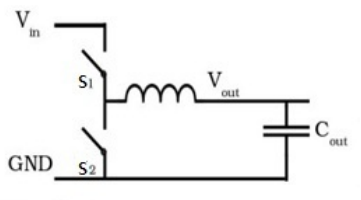


Figure 1: Buck Converter.

labelled $V_{in}$ and $GND$. Switches $S_1$ and $S_2$ are controlled by non-overlapping clocks.

While SLC buck converters are suitable for system integration at board and package level, it is difficult to integrate magnetics in system-on-chip (SoC) solutions. Therefore, there is an increasing interest in developing switched-capacitor (SC) DC-DC converters which are suitable for fully integrated Power-Supply on Chip (PwrSoC) [1]–[4].

Fig. 2 shows a basic SC DC-DC converter. Once again,

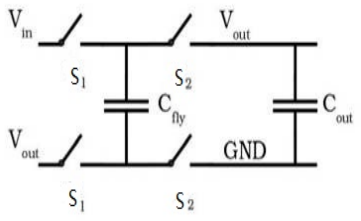


Figure 2: Basic SC DC-DC converter.

the input voltage is applied between the terminals labelled $V_{in}$ and $GND$ and the switches labelled $S_1$ and $S_2$ are controlled by non-overlapping clocks.

The output voltage of a SLC DC-DC converter can be regulated by adjusting the *duty cycle* of the switch clocks. By contrast, the output voltage of a SC DC-DC converter is determined by the *topology* of the converter; if the circuit topology is fixed, so is the output voltage.

To realize SC DC-DC converters with variable outputs, it is necessary to vary the topology of the circuit. In this paper we describe how the topology of a SC DC-DC converter can be reconfigured dynamically in order to achieve the goal of variable division ratios. We describe a three-stage converter with coarse and fine control of the output voltage. Such a converter could potentially meet the requirements of applications such as envelope tracking [5, 6].

In Sec. 2, we describe the operation of a basic SC DC-DC converter. We explain the operation of a reconfigurable SC DC-DC converter in Sec. 3. Secs. 4 and 5 address coarse and fine control of the output voltage. The complete system is described in Sec. 6.

## 2. SC DC-DC converter

The basic switched-capacitor DC-DC converter, shown in Fig. 2, consists of only switches and capacitors. The capacitor on the left, denoted $C_{fly}$ is known as the "flying capacitor." The capacitor on the right, denoted $C_{out}$, is called the output capacitor or bypass capacitor.

By driving the four switches labelled $S_1$ and $S_2$ with appropriately sequenced non-overlapping clocks, the connectivity of the circuit changes dynamically. As a result, this converter achieves power conversion from the input to the output with a fixed conversion ratio of 1/2. Thus,

$$V_{out} = \frac{1}{2} V_{in}.$$

## 3. Reconfigurable SC DC-DC converter

Fig. 3 shows a reconfigurable SC DC-DC converter [3]. With appropriate control signals applied to the switches, the circuit can be configured to provide three different conversion ratios, namely 1/3, 1/2 and 2/3.

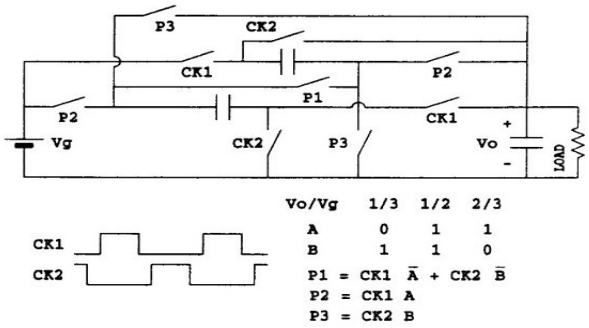


Figure 3: Reconfigurable SC DC-DC converter with three conversion ratios.

The three conversion ratio configurations are coded by two logic signals $A$ and $B$, and the corresponding control signals ($P1, P2, P3$) for the switches are shown in Fig. 3.

By changing the logic signals $A$ and $B$, different conversion ratios can be selected on the fly.

### 3.1. Example

Fig. 4 shows SPICE simulations of the output voltage $V_o$ when the converter is cycled repeatedly through conversion ratios of 1/3, 1/2, and 2/3 with an input voltage of $V_g$ = 6 V.

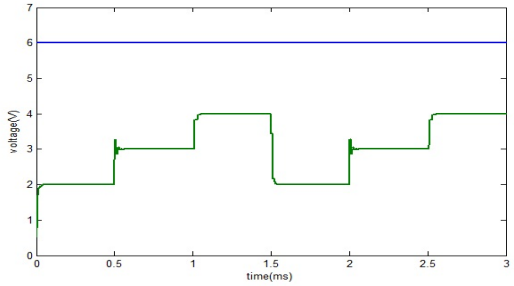


Figure 4: SPICE simulation of a three-ratio reconfigurable SC DC-DC converter cycling through conversion ratios of 1/3, 1/2, and 2/3.

The switches are clocked at 50 kHz. The topology is changed once per 0.3 ms. The output voltage cycles through 2 V, 3 V, 4V, as expected. The transient between steps lasts approximately five cycles of the switch clock.

## 4. Reconfigurable SC DC-DC converter with eight output levels

A larger number of capacitors and switches can be combined to provide a larger set of conversion ratios. Fig. 5 shows a reconfigurable SC DC-DC converter with eight possible output levels. It is formed by cascading two three-level reconfigurable SC DC-DC converters of the type shown in Fig. 3.

Each constituent converter has three possible conversion ratios: 1/3, 1/2 and 2/3. By adding two switches $S1$ and $S2$ to connect them together, we can produce eight different division ratios, as shown in Table 1.

| Constituent conversion ratios | Overall ratio $\times \frac{1}{36}$ |
|---|---|
| $\frac{1}{3} \times \frac{1}{3}$ | 4 |
| $\frac{1}{2} \times \frac{1}{3}$ | 6 |
| $\frac{2}{3} \times \frac{1}{3}$ | 8 |
| $\frac{1}{2} \times \frac{1}{2}$ | 9 |
| $\frac{1}{3}$ | 12 |
| $\frac{2}{3} \times \frac{2}{3}$ | 16 |
| $\frac{1}{2}$ | 18 |
| $\frac{2}{3}$ | 24 |

Table 1: Conversion ratios in the eight-level cascaded SC DC-DC converter shown in Fig. 5.

### 4.1. Example

Fig. 6 shows SPICE simulations of the output voltage $V_o$ when the converter is cycled repeatedly through all eight conversion ratio with an input voltage of $V_g$ = 36 V.

The switches are clocked at 50 kHz. The topology is changed once per 0.3 ms. The output voltage cycles through the prescribed levels, as expected. The transient between steps lasts approximately five cycles of the switch clock. Unlike the three-level case, the levels are not uniformly spaced in this example.

The control logic signals required to produce the cyclical pattern of eight levels are shown in Fig. 7.

The first and second stages in the cascade structure shown in Fig. 6 are coded by $A_1, B_1$ and $A_2, B_2$, respectively, where $A_i$ and $B_i$ has the same meanings as $A$ and $B$ in the individual three-level stages of the type shown in Fig. 3. $S1$ and $S2$ provide a unity conversion ratio when required.

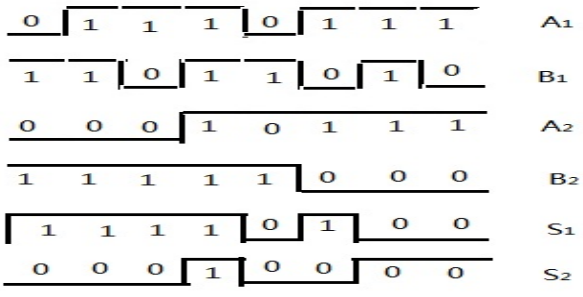


Figure 7: Eight-level reconfigurable SC DC DC Converter control signals.

This cascaded two-stage structure can realize coarse control of the output voltage; we next describe how to realize fine control.

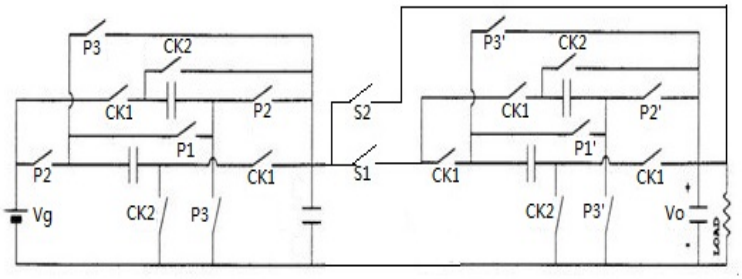


Figure 5: Eight-level reconfigurable SC DC-DC converter.

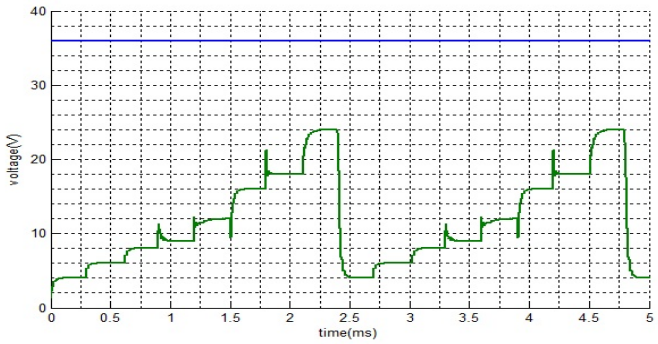


Figure 6: SPICE simulation of eight-level reconfigurable SC DC-DC converter cycling through the eight output conversion ratios shown in Table 1.

## 5. Fine control SC DC-DC converter

Fig. 8 shows a SC DC-DC converter which is capable of implementing fine control of the output voltage. When the

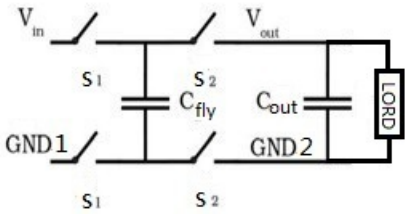


Figure 8: Fine control SC converter.

switches labelled $S1$ are closed, the flying capacitor $C_{fly}$ is charged to the input voltage $V_{in}$. When $S1$ is opened and $S2$ is closed, the flying capacitor discharges to the output.

$S1$ and $S2$ are controlled by two non-overlapping clocks, both of which have the same duty cycle. The conversion ratio of this SC DC-DC converter depends on the duty cycle.

The function of $C_{fly}$ is to transfer energy from the input to the load and to the output (storage) capacitor $C_{out}$. The function of $C_{out}$ is to maintain the output voltage and to make its ripple as small as possible.

The required values of the capacitors are defined by

$$C_{out} = \frac{I_0 \times t_1}{\Delta V_r}, \quad (1)$$

$$C_{fly} = \frac{\Delta Q}{V_{in} - V_{out}}, \quad (2)$$

where $V_{in}$ is the input voltage, $V_{out}$ is the output votage, $I_0$ is the load current, $t_1$ is the time for which the switches $S1$ are closed, $\Delta V_r$ is the output voltage ripple, and [2].

The charge $\Delta Q$ lost by $C_{fly}$ in the interval $t_2$ during which the switches $S1$ are open is given by [2]

$$\Delta Q = I_0 t_2 + C_{out} \Delta V_r. \quad (3)$$

Rearranging Eqs. (1), (2), and (3), we obtain

$$V_{out} = \frac{V_{in}}{1 + \frac{T}{C_{fly} R}}, \quad (4)$$

where $T = t_1 + t_2$ is the period of the clocks.

Note that the output voltage depends on the values of $C_{fly}$, the output current, the switching frequency $(1/T)$ and the input voltage. Once the values of $C_{fly}$, $I_0$ and $V_{in}$ are known, the switching frequency can be adjusted to set the desired output voltage.

### 5.1. Example

Fig. 9 shows a simulation of a SC DC-DC converter with fine control. In this example, the input voltage is $V_{in}$ =

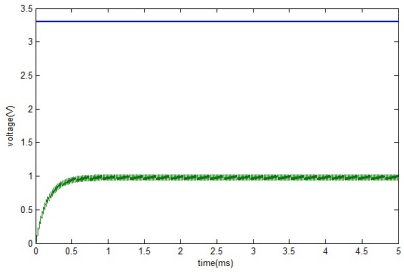


Figure 9: SC DC-DC converter with fine control.

3.3 V and the target output voltage is $V_{out}$ = 1 V. The switching period is $T = 20$ $\mu$s and the duty cycle $D$ is 0.1 (giving $t_1$ = 2 $\mu$s and $t_2$ = 18 $\mu$s). The output power is 1 W and the load is 100 $\Omega$ resistor; thus, $I_0$ = 10 mA. The maximum allowed output voltage ripple is 0.08 V; hence, the required values of the capacitors are $C_{out}$ = 2.25 $\mu$F and $C_{fly}$ = 0.086 $\mu$F, respectively.

## 6. Three-stage reconfigurable SC DC-DC converter with eight output levels and fine control

Fig. 10 shows a three-stage reconfigurable SC DC-DC converter with eight fixed output levels and fine control. This comprises the eight-level reconfigurable SC DC-DC

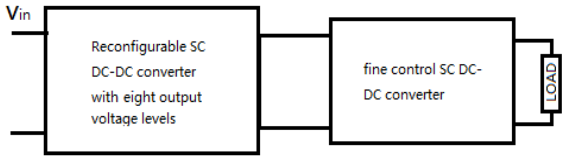


Figure 10: Three-stage reconfigurable SC DC-DC converter with eight fixed output levels and fine control.

converter decribed in Sec. 4 and the fine control stage described in Sec. 5 connected in cascade.

### 6.1. Example

Fig. 11 shows a simulation of this converter. The input is a 36V DC. The "coarse" stage (eight-level reconfigurable SC DC-DC converter) reduces this to 24 V with a fixed (topology-determined) conversion ratio of 2/3. The fine control converter further reduces this to 20 V.

## 7. Conclusions

We have described a three-stage SC DC-DC converter having coarse and fine control of the output voltage. Two cascaded stages can be reconfigured dynamically to give

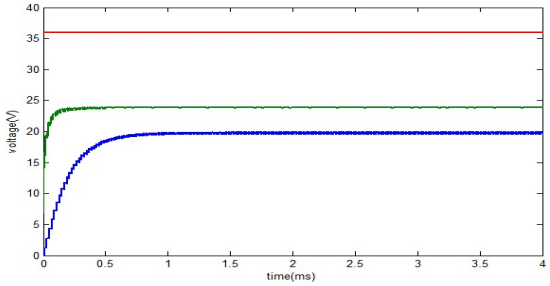


Figure 11: SPICE transient simulation of a three-stage converter. Top: input (36 V); middle: output of coarse stage (24 V); bottom: output (20 V).

eight fixed output levels. The final stage gives fine control of the output voltage by modulating the switching frequency. This type of architecture has the potential to address the needs of envelope tracking [5, 6] for efficient power amplifiers in wireless communication systems. Our ongoing research addresses this problem.


## Acknowledgment

This work has been funded in part by Science Foundation Ireland under grant 08/IN.1/I854.


## References


[1] M. Steyaert, T. Van Breussegem, H. Meyvaert, P. Callemeyn, M. Wens, "DC-DC Converters: From Discrete Towards Fully Integrated CMOS,"*Solid-State Device Research Conference (ESSDERC), 2011 Proceedings of the European*, pp. 59–66, Sept. 2011.

[2] P.K. Peter, V. Agarwal, "Analysis and Design of a Ground Isolated Switched Capacitor DC-DC Converter,"*Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, pp. 632–637, July 2010.

[3] M. S. Makowski, D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters,"*Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE* , pp. 1215–1221, vol.2, Jun 1995.

[4] M.D. Seeman, S.R. Sanders, "A 32nm Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/$mm^2$ at 81% Efficiency,"*Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp. 210–211, Feb. 2010.

[5] Ken Chan, "GC5325 Envelope Tracking Application Note,"*Texas Instruments Incorporated*, 2010.

[6] "Nujira $HAT^{TM}$ Power Modulator, "*Nujira Limited*, 2008