Immunity Estimation to Electrostatic Discharge by Circuit Simulation and Conducted Immunity Measurement of ICs

Yasuhiro SHIRAKI

Advanced Technology R&D Center, Mitsubishi Electric Corporation
8-1-1,Tsukaguchi-Honmachi, Amagasaki, Hyogo 661-8661, Japan
Shiraki.Yasuhiro@db.MitsubishiElectric.co.jp

***Abstract*— The author proposed an immunity estimation technique to electrostatic discharge (ESD) in the early design stage. The immunity estimation technique was applied to the immunity estimation of ICs on printed wiring boards (PWBs). It consists of a conducted immunity measurement of ICs and a circuit simulation. In the conducted immunity measurement, conducted noise from an ESD-gun is directly injected between a power terminal and a ground terminal of ICs and increased up to a malfunction of the IC. The input voltage at the IC terminals is measured when the IC malfunctions. In the circuit simulation, equivalent circuits are created by modeling the structure of the ESD-gun and the PWBs. The equivalent circuits were analyzed by the circuit simulation and calculated induced voltages between a power layer and a ground layer of the PWBs. Finally, threshold failure levels of the ICs on the printed wiring boards to ESD were defined as ratio of the input voltage in the conducted immunity measurement and the induced voltage in the circuit simulation. The results of the immunity estimation technique were verified experimentally.**

Key words: ESD, Immunity, ICs, Circuit Simulation

I. INTRODUCTION

It is necessary for electric and information products to take immunity test against the transient electromagnetic (EM) fields with broadband frequency spectra and high voltage caused by an electrostatic discharge (ESD). The ESD immunity test becomes task prior to introducing an electronic product into the market, which is prescribed in IEC 61000-4-2 standard [1]. It relates to the immunity requirements and test methods for electrical and electronic equipments subjected to ESD. On the other hand, it has been difficult to take effective ESD countermeasure, because of miniaturization and high-density mounting of products. As a result, ESD countermeasures should be tried at all stages like a design stage and a trial stage. If the products are evaluated at the trial stage and the countermeasures are needed, the development lead-time and cost are increased because they should be re-designed. Therefore it is important for products development to implement estimation and countermeasure for ESD at the early design stage.

In recent years, many fundamental studies have been done, for example, FDTD simulation and measurement for estimating output current of an ESD-gun. However, there are few studies about ESD immunity characteristics of ICs inside the products.

From the above viewpoint, this paper proposes an immunity estimation technique to ESD that based on a conducted immunity measurement of the ICs and a circuit simulation of equipments. This immunity estimation technique is able to evaluate immunity of the equipments to ESD at absolute values without trial manufactures. This technique applied to immunity estimation of ICs on printed wiring boards (PWBs), and its results are evaluated experimentally.

II. IMMUNITY ESTIMATION TECHNIQUE TO ESD

Fig.1 shows procedure of the immunity estimation technique, which consists of the conducted immunity measurement and the circuit simulation. In the conducted

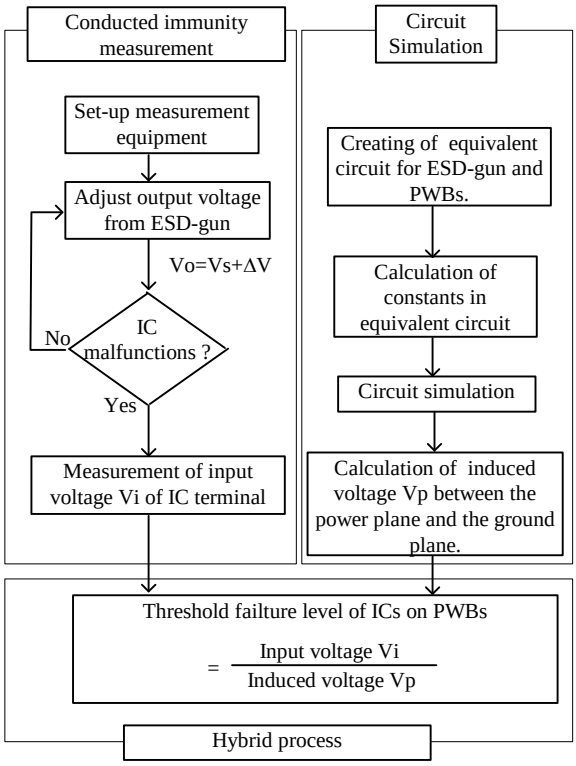

Fig. 1 Procedure of immunity estimation technique

immunity measurement, at first the ESD-gun is directly connected into the IC power terminals by coaxial cables. Next, the output voltage Vo from the ESD-gun is increased until the IC malfunctions at intervals of ΔV. When the IC malfunctions, the input voltage Vi is measured between the power terminal and the ground terminal of the IC. In the circuit simulation, the induced voltages Vp between the power plane and the ground plane of the PWBs are calculated. At first, equivalent circuits are created by modeling the structure of the ESD-gun and the PWBs. Next, the constant values of the circuits are calculated by electrostatic field analysis. Finally, the induced voltages Vp are calculated by the equivalent circuits by the circuit simulation. In the hybrid process, the threshold failure levels of ICs on PWBs were defined as ratio of the input voltage Vi and the induced voltage Vp. Therefore, it is possible to estimate immunity of the PWBs at absolute values without the trial manufactures.

III. Application of Immunity Estimation Technique

A. Structure of Printed Wiring Boards

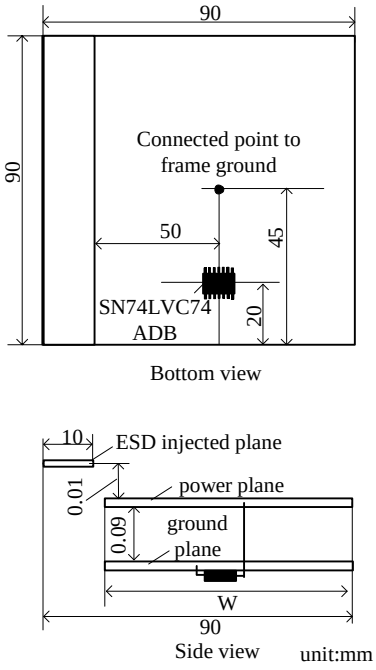

Fig. 2 Structure of printed wiring boards

The immunity estimation technique and a verification experiment were carried out with test PWBs in order to investigate the relation between the threshold failure level and the magnitude of the noise from the ESD-gun. Figure 2 shows the schematic of the 4-layer test PWBs. The first, second, third and fourth layers are the ESD injected plane, the power plane, the ground plane and the composite plane respectively. The PWBs were fabricated of an epoxy glass with a relative permittivity of ε_r=4.3. The surface sizes of the ESD injected plane were 90mm X 10 mm. The surface sizes of the power plane and the ground plane were 90mm X W mm. Here three kinds of PWBs with a width of W= 90 mm, W=80 mm and W=70 mm were used. The capacitive coupling between the ESD injected plane and the power plane was adjusted by altering W. The ICs, which were mounted on the fourth layer, were SN74LVC74ADB with flip-flops. In the initial condition, the information in the flip-flops was fixed high. When the information on the IC changed into low by injecting ESD, we defined this phenomenon as "malfunction".

B. Conducted Immunity Measurement

Figure 3 shows the method of injecting the output voltage of ESD to the IC power terminal. A part of the output current from the ESD-gun was separated into the ground by a branch circuit. The output current from the branch circuit to the IC side was injected to the IC power terminal through a capacitor. The DC current from the DC supply was injected at the IC power terminal through an inductor. The output current from the ESD-gun and the DC current could be efficiently transmitted to the IC power terminal with the inductor and capacitor. When the IC malfunctioned, the input voltage was measured between the IC ground terminal and the IC power terminal. The ESD-gun was shielded by an anionic chamber so that the emission from the ESD-gun should not affect to the voltage measurement of the IC terminals.

An experimental result is shown in Fig.4, where the output voltage of the ESD-gun is swept from 21kV to 23kV at intervals of 1kV. When the output voltage from the ESD-gun

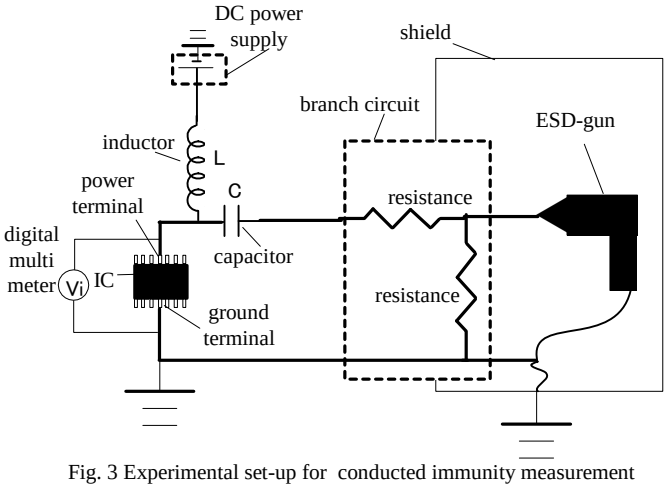

Fig. 3 Experimental set-up for conducted immunity measurement

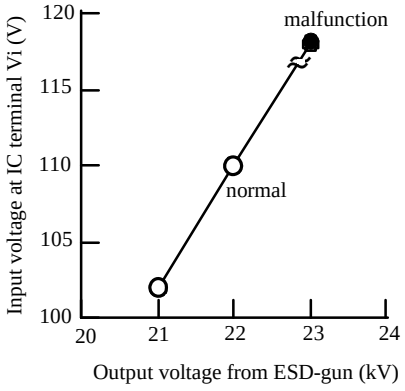

Fig. 4 Measurment result for conducted immunity measurement

became 23kV, the IC malfunctioned. At that time the input voltage was 118V between the IC power terminal and the IC ground terminal.

C. Circuit simulation of Printed Wiring Board

The circuit simulation was carried out as shown in Fig.1. Figure 5 shows analysis model for circuit simulation. The ESD-gun was placed vertically in contact with the ESD injected plane on the PWBs. These capacitances between ESD injected plane and power plane, the capacitance between power plane and ground plane, the capacitance between ESD injected plane and ground plane are defined as C_2, C_3, and C_4 respectively. The inductance of the cable is defined as L_2 between the ground plane and frame ground.

The equivalent circuits of the ESD-gun and the PWB are shown Fig.6. Table 1 shows the constants of the equivalent circuits. The constants of the ESD-gun were cited from Ref[2]. The capacitances C_2, C_3 and C_4 in the PWBs were calculated by electrostatic field analysis. These capacitances are different depending on the W. In the case of W=90, the capacitances C_2 and C_3 became the largest and the capacitance C_4 became zero, because the ESD injected plane and the power plane were completely faced. In the case of W=80, the capacitance C_4 became the largest, and the capacitances C_2 and C_3 were smaller than those of W=90. In the case of W=70, the capacitances C_2 and C_3 were lower than those of W=90 and W=80.

The capacitance C_5 between the ESD-gun and the frame ground was determined experimentally so that the circuit simulation coincides with measured current. The measured current was measured by inserting current transformer into the cable as shown in Fig.5. Figure 7 shows comparison of the currents that obtained circuit simulation and measurement. When the value of C_5 was 8pF, the simulation result agreed with the measured current.

Table 2 shows the calculation results of the induced voltage Vp by the circuit simulation. The induced voltages Vp were different depending on W.

D. Verification of Immunity Estimation Technique

The threshold failure levels of the ICs on the test PWBs were obtained when the input voltage Vi(=118V) as shown in Fig.4 were divided by the induced voltage Vp as shown in Table 2.

The threshold failure levels were verified experimentally. Figure 8 shows experimental set-up for verified measurement.

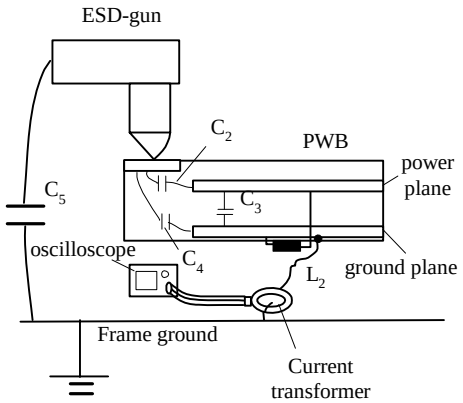

Fig. 5 Analysis model for circuit simulation

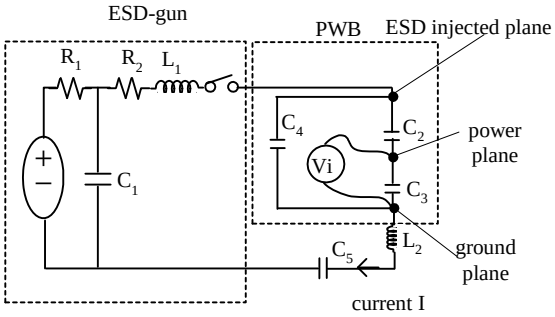

Fig. 6 Equivalent circuit for circuit simulation

Table 1 Specifications of ESD-gun and PWB

		W=90	W=80	W=70
ESD -gun	R_1	10MΩ		
	R_2	330Ω		
	L_1	200nH		
	C_1	150pF		
PWB	C_2	370pF	53pF	1.0pF
	C_3	350pF	320pF	280pF
	C_4	0pF	3.6pF	0.9pF
	C_5	8pF		
	L_2	0.26μH		

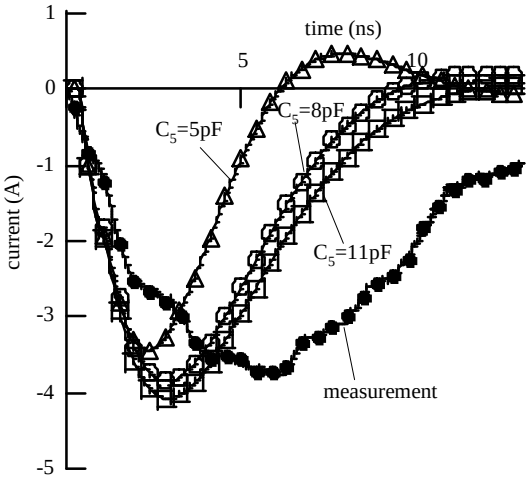

Fig. 7 Comparizon of current between measured and simulated values

Table 2 Calculation results of induced voltage by circuit simulation

	W=90	W=80	W=70
Induced voltage Vp(V)	23.2	21.4	3.8

A DC voltage was imposed on between the power plane and the ground plane through the inductor. The ESD-gun was placed vertically in contact with the ESD injected plane on the PWBs. As the output voltage from the ESD-gun was increased, the information of the memory in the ICs was measured by a digital multi meter. When the information of memory changed from high to low, the output voltage from the ESD-gun was measured as the threshold failure levels.

The comparison result of the immunity estimation technique and verified measurement is shown in Fig.9. The differences of both results in case of W=90, 80, 70 were 1.9%, 14% and 4.6% respectively.

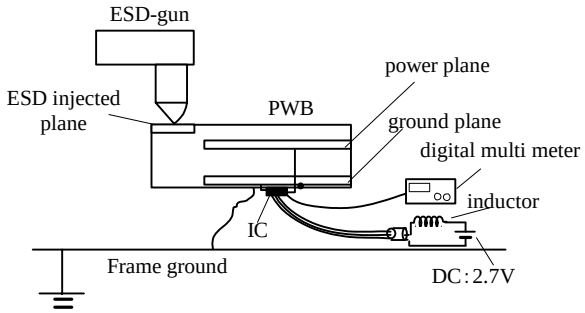

Fig. 8 Experimental set-up for verified measurement

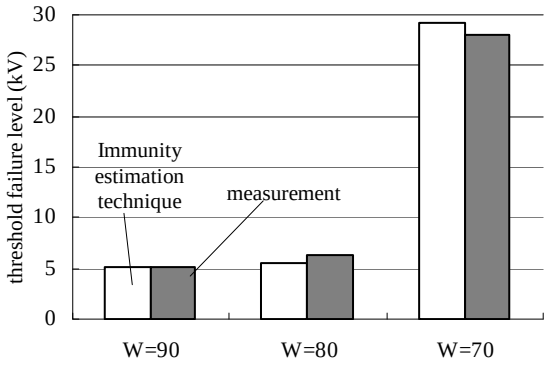

Fig. 9 Comparison of threshold failure level between immunity estimation technique and measurement

IV. CONCLUSION

In this paper, we proposed the immunity estimation technique to ESD that consists of the conducted immunity measurement and the circuit simulation. In the conducted immunity measurement, it was developed the method that the output voltage from the ESD-gun could directly injected the IC power terminal. To demonstrate the validity of the immunity estimation technique, it is investigate the relationship between the capacitive coupling and the threshold failure levels of the ICs on the PWBs due to output voltage from the ESD-gun. The results of the immunity estimation technique were evaluated experimentally, its results agreed with the accuracy within 14% of the experimental results.

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