Examination of Power-Ground Resonance for IBIS Model with Non-Ideal Power Supply

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Abstract —The effects of power-ground resonance in input/output buffer information specification (IBIS) models under non-ideal power supply are discussed. Though IBIS models are widely used as a behavioral model of input/output circuits in signal integrity assessments, problems of accuracy under non-ideal power supply have been pointed out. We discuss the cause of these difficulties and a solution by adding power-ground impedance.
Key words: power-ground resonance, signal integrity, IBIS, power-ground impedance

I. Introduction

With increasing frequency, density and power, as well as decreased size and logic level in electronic devices, signal integrity (SI) issues are becoming more and more serious. Demand for SI analysis at board and system levels is becoming greater and greater. Such analysis is mainly performed by simulating propagation of signals driven by the integrated circuits (ICs) on a printed circuit board. Therefore, an IC model is a key element.

Commercial transistor level IC models are usually large and consume a large amount of memory and simulation time. Furthermore, the transistor level IC models include the proprietary information of semiconductors. Therefore, such models cannot be easily distributed between companies. An alternative approach to the transistor level model is a macro model. One of the most common macro models is input/output buffer information specification (IBIS) [1]. IBIS models are widely used in SI analysis. However, it was reported that IBIS models cannot handle power integrity (PI) analysis well [2][3], and has difficulties even in SI analysis under non-ideal power supply.

We show that the problems in SI analysis under non-ideal power supply is closely related to power-ground resonance. We also show that a structure adding power-ground impedance to existing IBIS models, which is equivalent to the proposed structure in [3], is also effective against these problems. A commercial digital device is used as an example, and an IBIS model including the power-ground impedance is constructed from the measurements. Then the simulated results of the newly constructed model and an existing IBIS model are compared to the measured results.

The rest of this paper is organized as follows. Section II describes the effects of power-ground resonance in SI analysis and a construction method of the IBIS model with power-ground impedance. Section III shows the comparison of simulated and measured results in impedance and SI analyses. Section IV concludes the paper.

II. Effects of power-ground resonance in SI analysis

A. Effects of power-ground resonance

To investigate the effects of power-ground resonance in SI analysis, a commercial digital device, 74LVCU04AD made by Philips semiconductor[4], was used as an example. Figure 1 is a schematic of the device, which consists of six CMOS inverters and input protection elements and does not include a pre-driver. The output voltages of this device were measured with an output load of 50 Ω connected to a voltage source of 0 V and 3.3 V through a low pass filter as shown in Fig. 2. The measured results of the output voltage are shown in Fig. 3. We found that an attenuation resonance of 320 MHz occurs just after both rise and fall edges.

Next, to investigate the power-ground resonant frequency, an impedance simulation, as shown in Fig. 4, was performed, where Z_{device} represents the power-ground impedance of the device obtained using the method described in *C*. Since the simulated resonant frequency almost matched to that of the attenuation resonance (320 MHz), it is probable that the power-ground resonance is propagated to the output terminal through the on-state transistor as shown in Fig. 5.

B. Addition of power-ground impedance to IBIS model

We added power-ground impedance to an IBIS model to express the power-ground resonance. An IBIS model consists of a set of I-V tables that describes the static characteristics of the buffer, a set of V-T tables that represent the dynamic characteristics of the buffer and other information such as die capacitances and parasitic elements of the package as shown in Fig. 6. Since this information is fully derived from particular simulations or measurements [1], IBIS models do not reveal any proprietary information of I/O buffers.

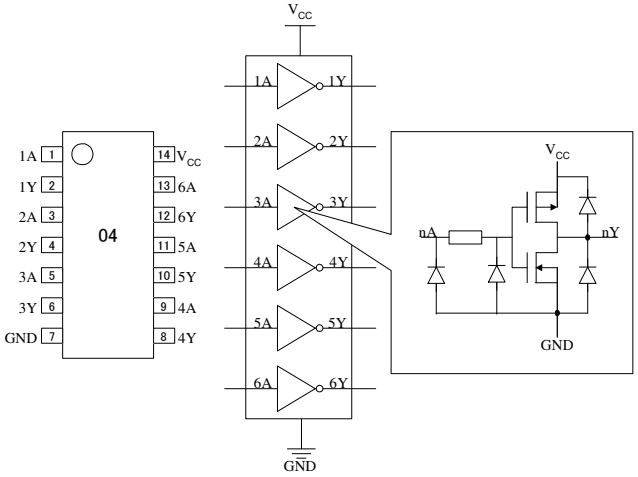

Fig. 1: Device under test (74LVCU04AD)

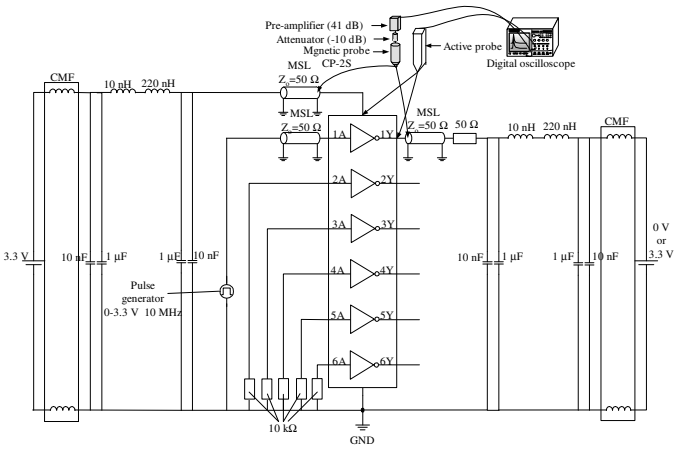

Fig. 2: Setup for measuring transient properties

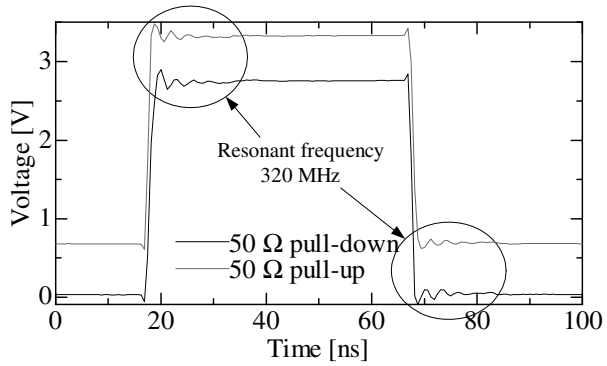

Fig. 3: Measured output voltages

In an IBIS model, the power-ground impedance is composed of a series of C_{pu} (or C_{pd}) and an on-state resistance extracted from the I-V tables of the pull-down element (or pull-up element) in Fig. 6. This impedance is, however, not accurate even in the device which has no pre-driver

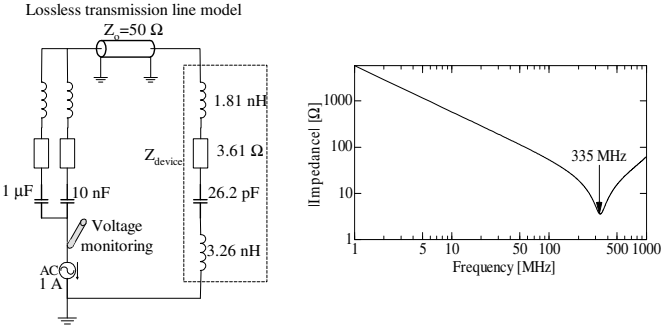

Fig. 4: Schematic of power-ground impedance simulation and simulated result

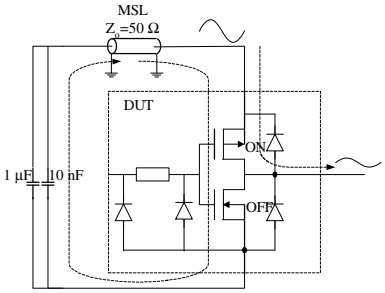

Fig. 5: Propagation mechanism of power-ground resonance

circuit, shown in Fig. 1, as presented in section III. We then added an impedance between the power and ground nodes on a chip, as shown in Fig. 6.

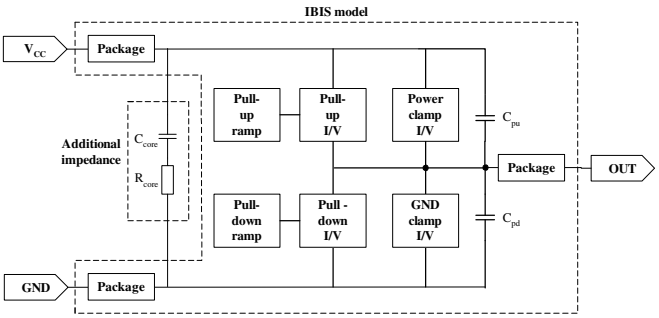

Fig. 6: IBIS model with power-ground impedance

C. Extraction of IBIS model including the power-ground impedance

A method for extracting the power-ground impedance as well as the IBIS model from measurements with the device under test (DUT) is described. The three following measurements are needed to construct an IBIS model with power-ground impedance.

1. I-V curves of pull-up, power clamp, pull-down and GND clamp elements

2. 3-port S-parameters

(Vcc-GND, OUT-GND and IN-GND)

3. Transient output voltage/current
   and power voltage/current in two output load conditions

Since the 1st and the 3rd measurements are the same as those in the well known IBIS modeling procedure, the only 2nd measurement is described. Only one inverter was used and the rest were pull-down with 10 kΩ in every measurement.

To identify each impedance element $C_{\rm core}$, $R_{\rm core}$, $C_{\rm pu}$ and $C_{\rm pd}$ in Fig. 6, 3-port S-parameters were measured with the setup shown in Fig. 7. Bias-Tees were used to give DC bias voltages to IN and Vcc terminals. With input voltages of 0 and 3.3 V, the S-parameters ($S_{11} \sim S_{33}$) were measured, then the S-parameters were converted to Z-parameters ($Z_{11} \sim Z_{33}$). The package impedances are assumed to be only inductance elements. This assumption makes sense because the parasitic capacitor and parasitic resistor of the package are much smaller than those of the chip. Also it is difficult to separate those of the package from the measured impedances. Therefore, $L_{\rm Vcc}$, $L_{\rm GND}$, $L_{\rm OUT}$ can be obtained from Z_{11}, Z_{13}, Z_{33}. The inductance elements in Z_{11}, Z_{13}, Z_{33} were 5.07, 3.26, and 4.51 nH, respectively. The inductance element in Z_{13} can be regarded as $L_{\rm GND}$, so $L_{\rm GND}$ was 3.26 nH. The inductance element in Z_{11} can be regarded as an addition of $L_{\rm Vcc}$ and $L_{\rm GND}$, so $L_{\rm Vcc}$ was 1.81 nH. The inductance element in Z_{33} can be regarded as an addition of $L_{\rm OUT}$ and $L_{\rm GND}$, so $L_{\rm OUT}$ was 1.25 nH. To identify the rest, each impedance element in Fig. 8 was calculated from Z_{11}, Z_{13}, Z_{33} by simultaneously solving the following equations, assuming that the IN terminal was completely isolated from the OUT terminal.

$$Z_{\rm pu} = \frac{Z_{11}Z_{33} - Z_{13}^2}{Z_{13}} \quad (1)$$

$$Z_{\rm pd} = \frac{Z_{11}Z_{33} - Z_{13}^2}{Z_{11} - Z_{13}} \quad (2)$$

$$Z_{\rm core} = \frac{Z_{11}Z_{33} - Z_{13}^2}{Z_{33} - Z_{13}} \quad (3)$$

$C_{\rm core}$ is identified from $Z_{\rm core}$, and $C_{\rm pu}$ and $C_{\rm pd}$ are obtained by subtracting $C_{\rm core}$ from the capacitance in Z_{11}. $R_{\rm core}$ is calculated from the resistance in Z_{11} and the on-state resistance of the transistor. The identified results of Z_{11} and $Z_{\rm core}$ are shown in Fig. 9.

III. Comparison of simulated and measured results

A. Comparison in impedances

With regard to the Z-parameters (Z_{11}, Z_{13}, Z_{33}) of the device, a comparison of simulated results of the IBIS model with the power-ground impedance and measured results is shown in Fig. 10. They are almost the same below the resonant frequency. Above the resonant frequency, the sim-

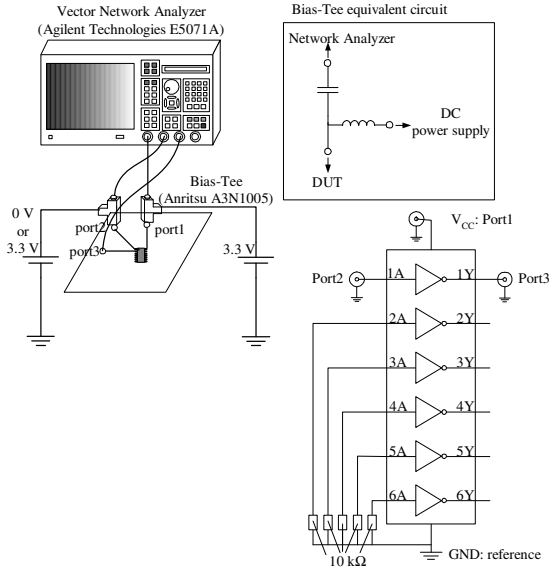

Fig. 7: Setup for measuring S-parameter

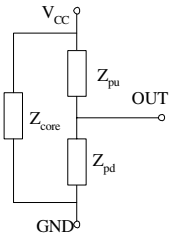

Fig. 8: Linear equivalent circuit for impedance extraction

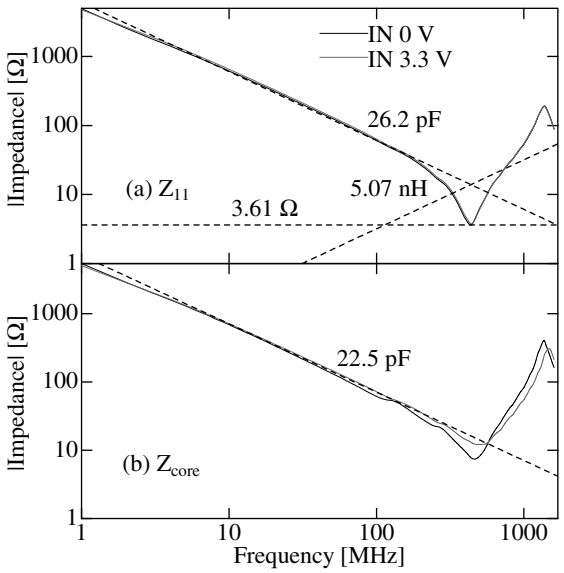

Fig. 9: Z_{11}- and $Z_{\rm core}$- identified results

ulated results are not in agreement with the measured results because of anti-resonance. The anti-resonance might be related to package capacitances.

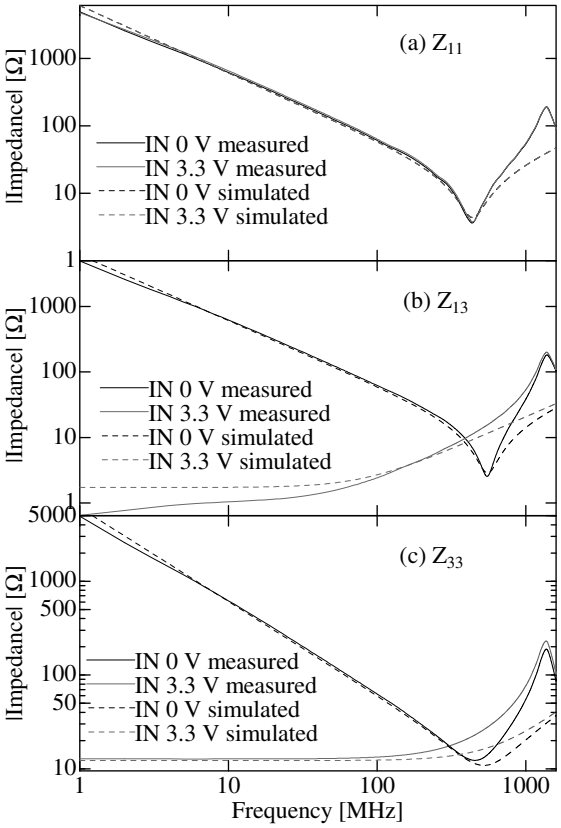

Fig. 10: Comparison of Z-parameters

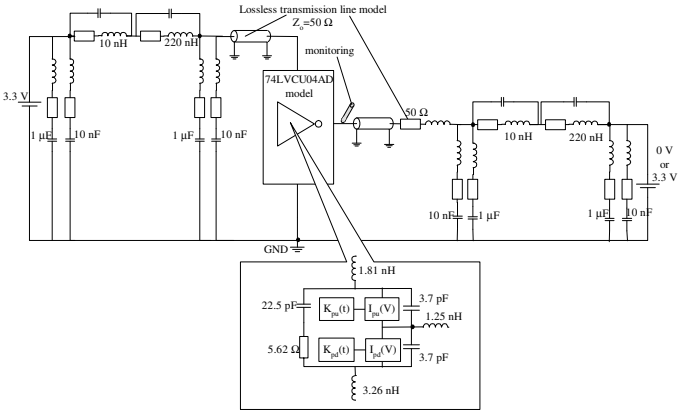

Fig. 11: Schematic of transient simulations

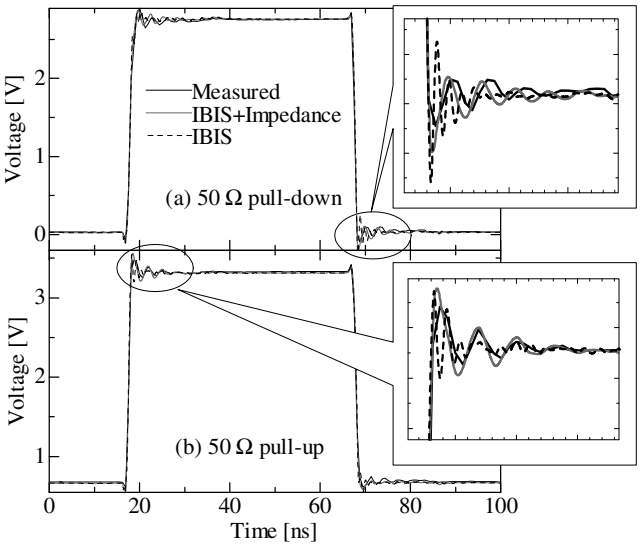

Fig. 12: Comparison of output voltages

B. Comparison of output voltages

The simulated results from the IBIS model with and without the power-ground impedance are compared to the measured results of the output voltage in section II. The schematic for the simulations is shown in Fig. 11 and the results are shown in Fig. 12. As expected, the results show that the IBIS model with the power-ground impedance is in better agreement with the measured results concerning the resonant frequency. However, the attenuation constant and properties around the overshoot and undershoot are not in agreement with the measured results. It might be necessary to reconsider R_{core}, K_{pu}, K_{pd}, etc...

IV. Conclusion

The effects of the power-ground resonance in SI analysis were described, then a structure adding power-ground impedance to an existing IBIS model was presented. Two IBIS models of a commercial digital device were constructed from measurements : the IBIS models with and without the power-ground impedance. The simulated results from these models were compared to the measured results, and it was shown that the better results can be obtained using the IBIS model with the power-ground impedance. In the future, we plan to develop a more accurate model for SI analysis.

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