A CMOS Opamp Immune to EMI with no Penalty in Baseband Operation

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Abstract— **In this paper, a novel CMOS Operational Amplifier input stage which is robust to high power electromagnetic interference (EMI) without any significant penalty in baseband performance is presented and its operation principle is discussed. An opamp which includes the new input stage is proposed and it is compared in terms of immunity to EMI with a standard opamp circuit on the basis of computer simulations and experimental results.**

I. Introduction

The steady increase of environmental electromagnetic pollution has constantly raised the level of RF interference (RFI) superimposed onto nominal signals in present-day integrated circuits (ICs) and a high immunity to EMI has consequently become a mandatory requirement for any micro- and nano-electronic product.

In such a scenario, the susceptibility to RFI of operational amplifiers (opamps), whose input differential pair demodulates RFI and translates it into a DC offset and/or baseband distortion, is a serious concern in microelectronic design [1]. To this purpose, several opamp input stages immune to Electromagnetic Interference (EMI) have been proposed in the literature over the last years [2]. The baseband electrical performance of these circuits, however, is typically worse with respect to standard opamps, especially for what concerns bandwidth and/or phase margin [3].

In this paper, a novel opamp input stage, which exploits negative feedback to achieve a robust compensation of RFI-induced distortion, is proposed. Such a circuit has been employed to design a CMOS opamp which has been fabricated by a 0.35um CMOS technology. According with both computer simulations and EMI susceptibility measurements, the designed opamp is much more immune to EMI with respect to a standard opamp and does not show any remarkable penalty in baseband performance.

The paper has the following structure: in Section II, the effects of RFI in an MOS device are revised and the RFI compensation mechanism, on which the novel opamp input stage is based, is described. In Section III, the design of the novel opamp input stage, which is intrinsically immune to EMI, is addressed. In the same Section, the design of a CMOS opamp which includes the novel input stage, is also presented.

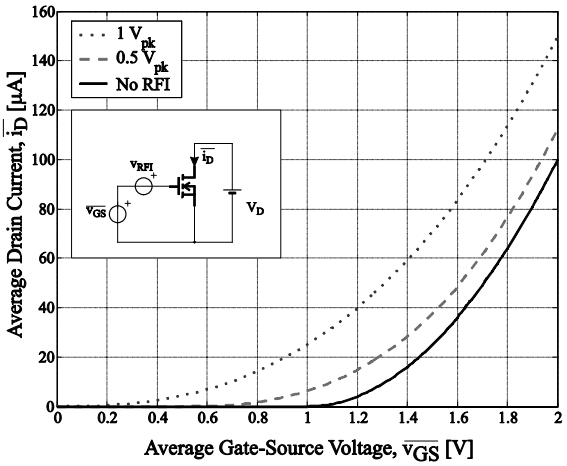

Fig. 1 Static $I_D(V_{GS})$ curve of an MOS device in the presence of RFI $I_D(V_{GS})$

In Section IV, the novel opamp circuit is compared with a standard CMOS Miller opamp both in terms of susceptibility to EMI and in terms of baseband performance, on the basis of computer simulations and experimental results. Finally, in Section V, some concluding remarks are drawn.

II. Effects of RFI in Analog Circuits

RFI-induced failures in integrated opamps have been ascribed to the nonlinear effects of RFI on the operation of the devices of their input differential pair. In this Section, the effects of RFI on the operation of active devices, which were previously analyzed in [4-5], are revised and a nonlinearity compensation principle is proposed in order to achieve immunity to RFI. Such a principle will be implemented in the novel opamp input stage proposed in this paper.

A. Effects of RFI on MOS Transistors

RFI-induced failures in opamp input stages are related to the effects of EMI on the operation of active devices, whose nominal DC characteristics are affected by RFI [5-6]. In order to highlight such effects, the MOS device in the inset of Fig.1, which is biased in the saturation region and in which continuous wave (CW) RFI is superimposed onto the gate-source voltage, is now considered.

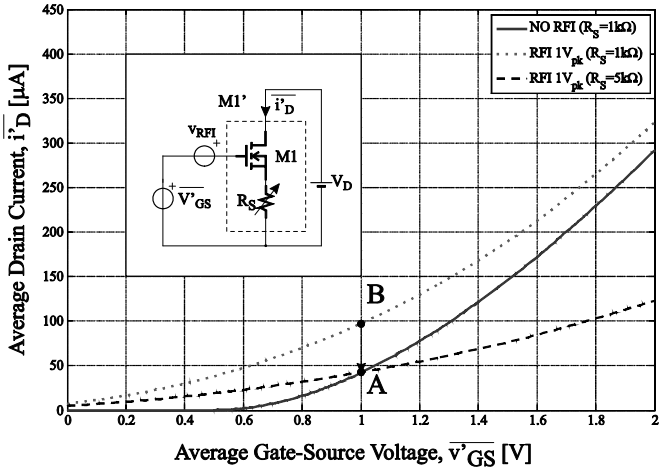

Fig. 2 RFI Compensation Principle

With reference to such a device, the time-averaged drain current, $\overline{i_D}$, can be expressed as a function of the time-averaged gate-to-source voltage $\overline{v_{GS}}$ but such a function is not given by the nominal static $I_D = f(V_{GS})$ relation of the MOS transistor and it depends on the amplitude V_{rf} of RFI superimposed onto the gate-source voltage. The equivalent $\overline{i_D} = \tilde{f}(\overline{v_{GS}}, V_{rf})$ characteristics of an MOS transistor in the presence of continuous wave (CW) RFI, (V_{rf}=500mV and V_{rf} =1V peak amplitude) are compared with its nominal characteristic in Fig.1.

It can be noticed that, for a given V_{GS}, the average drain current of an MOS transistor in the presence of RFI is higher than the average drain current of a similar device with no RF excitation and it increases with the amplitude of RFI. Such a change in the DC drain current originates RFI-induced failures in analog circuits.

B. RFI Effects Compensation

On the basis of the above considerations, the effects of RFI on an MOS transistor could be compensated, in principle, by replacing an MOS device with the equivalent device M1', that includes an MOS transistor M1 and a variable source-degenerating resistor R_S, as depicted in the inset of Fig.2. With reference to such a figure, the proposed RFI compensation technique will be illustrated in the following.

Assuming that the DC characteristic of M1 is $I_D = f(V_{GS})$, the DC characteristics $I'_D = f(V'_{GS})$ of the equivalent device M1' in Fig.2 can be expressed as

$$I'_D = f(V'_{GS} - R_S I'_D). \quad (1)$$

Such a characteristics, which depends on the value of R_S, is plotted in Fig.2 in continuous line for R_S=1kΩ.

In the presence of RFI excitation, the average current $\overline{i_D}$ characteristic of the MOS device M1, included in M1', can be expressed as $\overline{i_D} = \tilde{f}(\overline{v_{GS}}, V_{rf})$, as described with reference to Fig.1. If the value of R_S is kept constant, the overall average current of M1', $\overline{i'_D}$, is now expressed as

$$\overline{i'_D} = \tilde{f}(\overline{v_{GS}} - R_S \overline{i'_D}, V_{rf}), \quad (2)$$

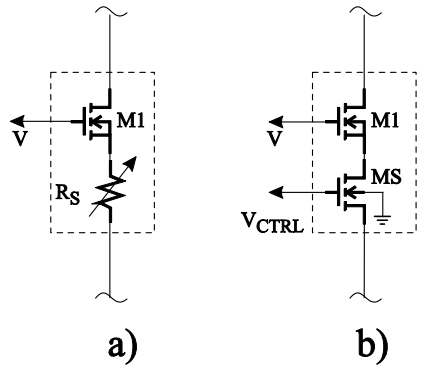

Fig. 3 Equivalent device for RFI compensation (a) and its CMOS implementation (b),

and it is affected by RFI, as shown in Fig.2 (dotted line, for RFI peak amplitude V_{rf} =1V). As a consequence, if the equivalent device M1' is biased at point A ($V'_{GS} = 1V, I'_D = 45\mu A$) with no RFI excitation, its bias point changes to B ($V'_{GS} = 1V, I'_D = 98\mu A$) in the presence of RFI.

Since $\overline{i'_D}$ depends on R_S, the effects of RFI on M1' can be compensated, in principle, if the value of the resistance R_S is modified properly in the presence of RF disturbances. With reference to Fig.2, it can be observed that, if R_S is changed from 1kΩ to 5kΩ, the DC current flowing into the equivalent device M1' in the presence of RFI (V_{rf} =1V, dashed line), for $\overline{v'_{GS}} = 1V$ is equal to the current flowing in M1' for the same value of $\overline{v'_{GS}}$ with no RFI excitation. In conclusion, the RFI-induced shift in the DC operating point from A to B has been compensated by the change in R_S and the bias point of M1', in the presence of RFI, has been brought back to A.

C. CMOS Implementation

The compensation principle, which has been outlined above, can be implemented in CMOS technology by replacing the tunable resistor R_S with an MOS transistor MS biased in deep triode region as depicted in Fig.3. The equivalent drain-to-source resistance R_{DS} of an MOS transistors biased in the resistive region can be expressed as

$$R_{DS} = \frac{1}{\frac{W}{L}\mu C_{ox}\left(V_G - V_T + \frac{V_D+V_S}{2}\right)} \quad (3)$$

where μ is the mobility of the channel carriers, C_{ox} is the gate capacitance per unit area, W/L is the aspect ratio, V_T is the threshold voltage and V_G, V_D, V_S are, respectively, the gate, drain and source voltages of the MOS device, evaluated with reference to the body terminal.

It can be observed that R_{DS} depends on the gate voltage of MS, as a consequence, the nonlinear compensation mechanism highlighted in Sect.IIB can be achieved by providing a suitable RFI-dependent voltage V_{CTRL} to the gate of the MS transistor. This control voltage can be generated by a closed-loop EMI control circuit, which senses nominal signals and RFI added to the gate-source voltage of the device.

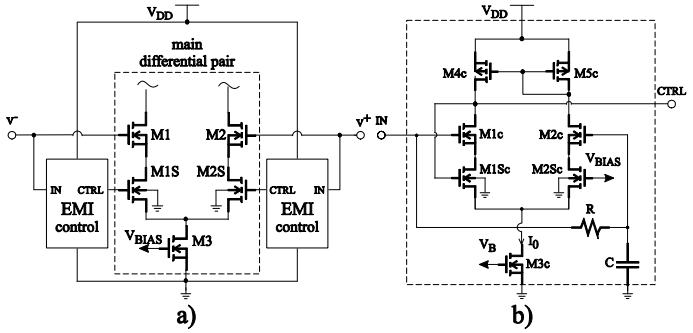

Fig. 4 Schematic of the EMI resisting differential pair (a) and of its transconductance control network (b)

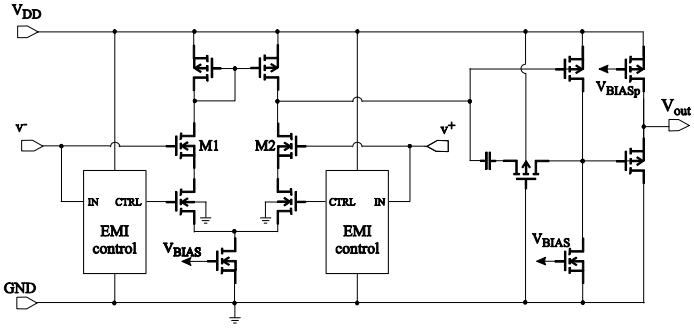

Fig. 5 Schematic of the CMOS Miller opamp circuit immune to EMI

In the following, the EMI compensation technique described above will be employed in order to design an opamp input stage insensitive to high power EMI. A CMOS implementation of the EMI-control circuit, in particular, will be proposed for such a specific application.

III. Operational Amplifier Input Stage Immune to EMI

The compensation principle, which has been described in the previous Section, has been employed in order to design an opamp input stage immune to high power EMI, whose schematic is reported in Fig.4a. Such a circuit is similar to a standard differential pair, in which the input devices have been replaced by the equivalent devices shown in Fig.3b. The control voltage of such equivalent devices is provided by the two EMI-control blocks depicted in Fig 4a, whose schematic is reported in Fig.4b and whose operation principle is discussed in the following.

A. EMI Control Building Block

In order to generate the control voltages V_{CTRL1} and V_{CTRL2}, required in the opamp input stage in Fig.4a, the EMI-control block in Fig.4b has been designed.

Such a circuit includes a replica of the differential pair in Fig. 4a (M1c, M2c and bias current source M3c) and of its source-degeneration transistors (M1Sc, M2Sc). The replica differential pair is loaded by a current mirror (M4c, M5c) which translates the differential current into a single-ended output voltage, which is the output V_{CTRL} of the transconductance control block.

The inverting input terminal v^- of the replica differential pair is directly connected to one of the input terminals of the main differential pair (see Fig.4b) while the non-inverting input v^+ is connected to the same terminal through a low pass *RC* filter that is designed to suppress RF disturbances and to pass nominal baseband signals. The gate voltage of the source-degeneration transistor MS2c is connected to a constant bias voltage V_{BIAS} while the gate terminal of MS1c is connected in feedback to the output voltage V_{CTRL}.Thanks to negative feedback, the gate voltage of MS1c is driven so that the baseband component of the drain currents of M1c and M2c are equal, independently of the presence of RFI.

RFI superimposed onto the external input affects the operation of M1c but not the operation of M2c (M2c is connected to the external input through an *RC* filter which suppresses RFI). As a consequence, the DC current flowing in the branch M2c - M2Sc is constant and not affected by RFI and negative feedback compensates RFI-induced changes in the characteristics of M1c with opposite changes in the resistance of M1Sc, so that the currents flowing in the two branches are equal.

Since the branch M1c - M1Sc is matched to the branch M1 - M1S of the main differential pair and both M1 and M1c are directly connected to the same external input voltage (including both nominal signal and RFI components), the output voltage of the EMI control circuit can be exploited to provide the gate voltage of M1S which is required to keep the current of the branch M1 - M1S constant and independent of RFI, according with the principle depicted in Sect.II. The same EMI control technique can be employed for the branch M2-M2S of the main differential pair by introducing a second identical EMI control block, as shown in Fig.4a.

IV. Design of an Operational Amplifier Immune to EMI

A CMOS Miller opamp circuit, which employs the EMI-robust differential pair described in the previous Section, has been designed and integrated on silicon by a CMOS 0.35μm technology and its operation in the presence of EMI has been compared with a CMOS Miller opamp with a standard differential input stage. The schematic of the novel opamp circuit topology is given in Fig.5. The standard circuit considered for comparison is identical to the one in Fig.5 (identical aspect ratios), except that M1S, M2S and the transconductance control blocks are not included and that the sources of the input devices M1 and M2 are directly shorted to the drain of the bias transistor M3.

A. Baseband Electrical Characteristics

The main electrical characteristics of the designed opamp circuits, obtained from DC and AC simulations, are reported in Tab.I. From such a table, it can be noticed that, unlike other solutions which have been previously proposed to achieve immunity to EMI, the baseband performance of the novel opamp circuit is not degraded with respect to the standard design.

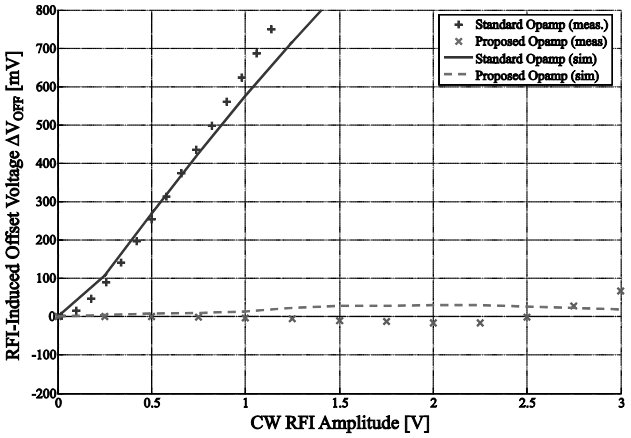

Fig. 6 Simulated and Measured RFI-induced Offset Voltage versus CW RFI amplitude (CW RFI frequency: 100MHz) in a standard CMOS Miller opamp (continuous line) and in the proposed opamp circuit (dashed line)

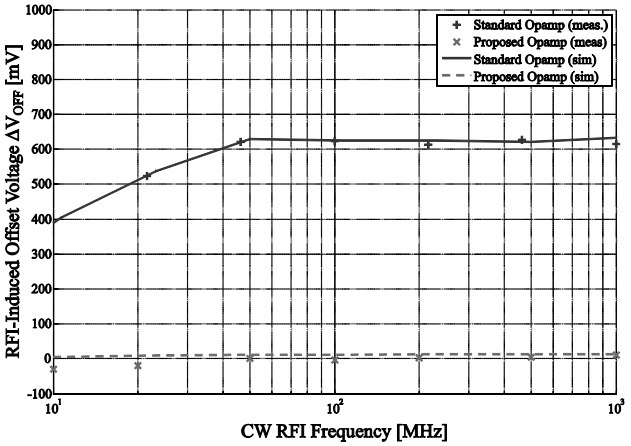

Fig. 7 Simulated and Measured RFI-induced Offset Voltage versus CW RFI frequency (CW RFI peak amplitude: 1V) in a standard CMOS Miller opamp (continuous line) and in the proposed opamp circuit (dashed line)

It should be observed, in particular, that the proposed solution does not suffer of the limitations in terms of bandwidth and phase margin which are experienced in EMI-resisting opamps where RFI filtering is performed in the main signal path [3]. It should be noticed, however, that a certain degradation in large-signal (*slew rate*) performance has been noticed.

The performance in terms of immunity to EMI of the two circuits is discussed in the following on the basis of time-domain computer simulation results.

B. Computer Simulations and Experimental Results

The susceptibility to EMI of both the standard and the novel opamp circuit has been tested by computer simulations and on-chip direct injection measurements. To this purpose, both circuits have been connected in the voltage follower configuration and an RF continuous wave (CW) interference has been added to the nominal DC input voltage.

The setup described in [6] has been employed for chip-level susceptibility measurements. The RFI-induced offset on the opamp output voltage has been considered to compare the susceptibility of the two circuits.

TABLE I
OPAMP MAIN ELECTRICAL CHARACTERISTICS

Parameter	**Standard Opamp**	**Proposed Opamp**
Power Supply	3.3V	3.3V
DC Current Consumption	144μA	168μA
DC Gain	95dB	95dB
Gain-Bandwidth Product	12MHz	12MHz
Phase Margin (volt follower)	89°	89°

In Fig.6 the simulated and measured RFI-induced offset voltage in the immune and in the standard opamp circuit is plotted versus the peak amplitude of CW RFI with a frequency of 100MHz. In Fig.7, the RFI-induced offset is plotted versus CW RFI frequency in the band 10MHz-1GHz, for an RFI peak amplitude of 1V. It can be observed from both figures that the new opamp circuit, that is based on the high immunity input stage described in this paper, shows a high immunity to EMI, even in the presence of high power disturbances (up to 3V of peak amplitude).

V. CONCLUSIONS

A new opamp input stage which is robust to high power EMI has been proposed and its operation principle has been discussed. An opamp circuit, which includes the new input stage, has been designed and compared with a standard Miller opamp. Simulated and experimental results show that the novel circuit achieves a high immunity to EMI without penalty in baseband performance.

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