EMC Modeling of an Intel Dual Die CPU

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***Abstract*— With the continuous increment in the requirement of chip performance, multiple dies integrated in a single package have become an effective and efficient way. However, under such high integration, it is found that electromagnetic interference generated turns to be a critical potential problem in further application environment. This paper presents an electromagnetic study with Intel Pentium Dual Die CPU model which is modelled as a patch antenna model with high radiation frequency relating to the industrial, scientific and medical (ISM) radio bands (2.45GHz and 5.80GHz). The model geometry is extracted from the data sheet of existing chip with some approximations. Various comparisons are studied under different situations of mounted heatsink and die distance, by means of FEM in frequency domain.**

Key words: Heatsink, Electromagnetic radiation, Dual die CPU, EMI, EMC

I. INTRODUCTION

Hitherto, Moore's Law is still effective in processor fabrication where the number of transistor doubles every two years. However, the quest of higher performance stimulates the designer to extract the ultimate implementation on a single chip. Intensive chip density, increasing operation frequency and low supply voltage have been applied maturely in the integrated circuit. Recently, multi-die packages have become widely used in the processor industry. This packaging technique combines multiple dies inside one single package. One typical product is Intel Quad Core processor. There are two cores in each die and two dies in the same package. Considering the high performance with fast operation frequency, low working voltage and complex internal structure, the electromagnetic effect turns out to be more and more important. This makes the research of EMI/EMC quite valuable.

Referring to the Intel processor datasheet [6], a transverse section of the Intel dual die processor with heatsink is illustrated in Fig. 1, packaging with a Flip-Chip Land Grid Array (FC-LGA6). The die stands upon the substrate with help of die attach material. Sealing is the integrated heat spreader (IHS) covering the dies in order to protect them. Adhered by the thermal interface material (TIM), the heatsink is fully contacting the top of IHS. In this paper, the CPU model for EMC modeling is extracted as a microstrip patch antenna structure, which is upgraded from the conventional IEEE challenging model 2000-4 [1] on the electromagnetic problem of CPU and heatsink and will be presented in a later section. The purpose of this research is to find how the interference generated around ISM radio bands (2.45GHz and 5.80GHz) is affected and to provide optimization based from the previous work [2]. Modeling and simulation are implemented using High Frequency Structure Simulator (HFSS) [10] with Finite Element Method (FEM) in the frequency domain.

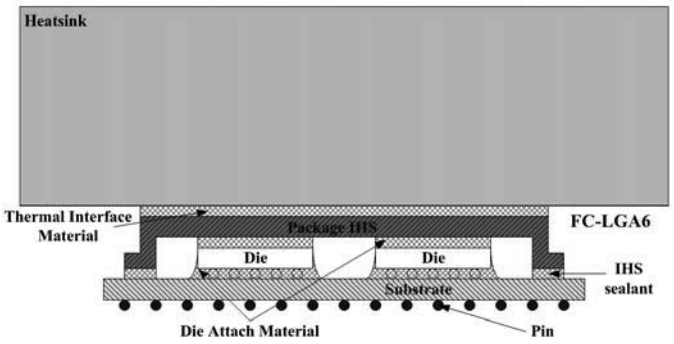


Fig. 1 Transverse section of Intel Dual Die processor

II. INTEL DUAL DIE CPU MODELING

A. Frequency domain EM modeling

A full-wave electromagnetic solution, which solves electromagnetic problem with Maxwell's equations, is of great importance to high performance VLSI designs in computational electromagnetics. With numerous fast numerical algorithms developed, Finite Element Method (FEM) is relatively efficient in finding approximate solutions of partial differential equations (PDE).

In this paper, simulation is applied on the full-wave frequency domain solution with variable sized meshes implemented. Frequency is setup to sweep in an interested range to find out the expectant resonant frequency when it is uncertain. However, deciding the correct frequency range is quite important for the simulation results. Computational errors may be introduced if the solution frequency range is mismatched.

B. Extracted Model

Recent research has been done on the EMC problem of CPU heatsink based on the conventional IEEE challenging model 2000-4 [3][4][5]. When considering CPU with multiple

dies, however, the model is no longer applicable. Therefore, a new microstrip patch antenna structure (as shown in Fig. 2) is proposed which is close to the real chip structure.

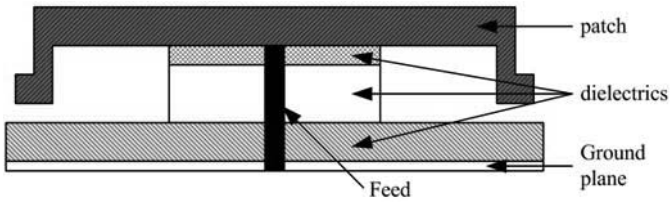


Fig. 2 Applied microstrip patch antenna structure for CPU model

As each microstrip patch antenna structure applied in the model representing a single die, the location of feed points is a critical factor that affects the accuracy and validation of simulation result. Fig. 3 gives a heat distribution on an existing Intel dual die CPU [7][8][9], where different colours represent different activity rates. The hottest point is the area of highest current flow and activity, therefore the electromagnetic interference generated is more significant. These points are consequently used as excitation points in the model for EMC simulation.

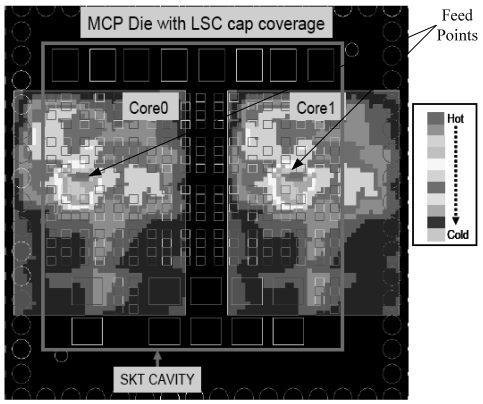
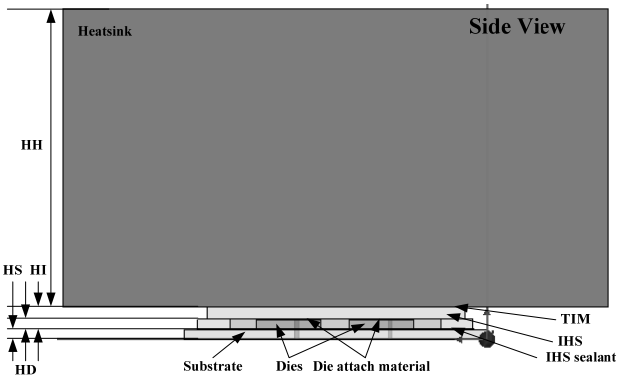
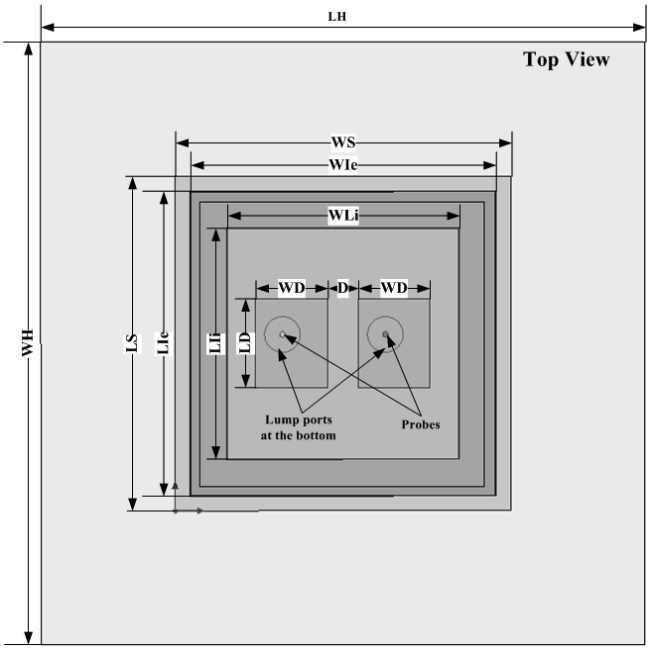


Fig. 3 Dual die hot spot locations [8]

Returning back to the top of view, the physical chip model consists of substrate, dies, IHS, heatsink and other adhesive materials. The whole structure is extracted following the released documents [6], with certain assumptions on parameters which are classified. Modification and simplification are implemented to reduce the mesh complexity which could save simulation time and resources. The bottom surface of the substrate is grounded and two lump ports are subtracted from it to give the internal excitations separately in order to simulate the two dies action inside the chip which acts as microstrip patch antenna. Two probes are standing through the substrate and dies acting as the internal connections. After implementing the extraction, the final model is illustrated in Fig. 4(a) and Fig. 4(b). The structure specification is also detailed in TABLE 1.



(a) Side view of model for Intel Dual Die processor



(b) Top view of model for Intel Dual Die processor

Fig. 4 Simulation model of Intel Dual Die processor with heatsink

TABLE 1

STRUCTURE SPECIFICATION OF INTEL DUAL DIE PROCESSOR [6]

Name	Min (mm)	Typical (mm)	Max (mm)
Height of Heatsink (HH)		37	
Height of IHS (HI)		1.65	
Height of Dies (HD)		1.15	
Height of Substrate (HS)		1.25	
Depth of TIM		0.1	
Depth of Die attach material		0.1	
Depth of IHS sealant		0.1	
Length of Heatsink (LH)		67.5	
Width of Heatsink (WH)		67.5	
Length of Substrate (LS)	37.45	37.5	37.55
Width of Substrate (WS)	37.45	37.5	37.55
Length of IHS external (LIe)	33.9	34	34.1
Width of IHS external (WIe)	33.9	34	34.1
Length of IHS internal (LIi)		26	
Width of IHS internal (WIi)		26	

C. Applied Simulation Setup

1) *Materials*: The assignments of all materials are described in TABLE 2.

TABLE 2

MATERIAL ASSIGNMENT OF SIMULATION MODEL

Name	Materials	Permittivity	Conductivity (Siemens/m)
Substrate	polyimide	3.5	0
Die	silicon	11.9	0
IHS	aluminum	1	3.8×10^{7}
Heatsink	aluminum	1	3.8×10^{7}
TIM	silicone	1.8	0
Die Attach Material	silver	1	6.1×10^{7}
IHS Sealant	epoxy	1.8	0

2) *Excitations*: In this model, in order to observe the scattering parameter in the close structure, two circular lumped ports with impedance of 50 ohm are defined separately to the two individual dies at the bottom of substrate. Connecting each lumped port, there is a copper probe standing through the substrate and die acting as microstrip patch antenna.

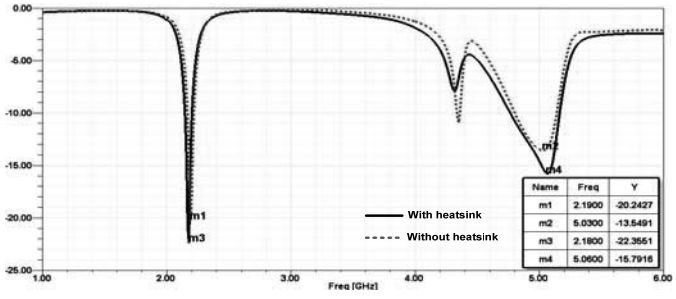
3) *Boundaries*: Finite conductivity boundary and radiation boundary are applied in the model. Finite conductivity boundary means imperfect conductor and Radiation boundary is applied in the simulation of open problems where the infinite spread radiation waves need to be calculated. As the real substrate is implemented with several layers, we simplified the structure with the bottom applied as the ground with finite conductivity boundary. The radiation boundary is used on the surface of surrounding air. A box shape model is employed instead of sphere for more suitable results.

III. Simulation And Results

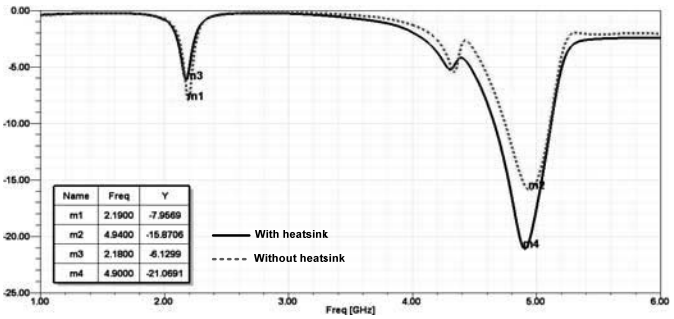
In simulation, solutions are setup with sweep frequency between 2GHz and 6GHz. Several resonant frequencies are found for the port1 and port2 respectively. Results of different situations are collected as the following.

A. Simulation results with or without Heatsink

Simulation is accomplished with the situation of with and without heatsink mounted upon the CPU model. Fig. 5(a) and Fig. 5(b) illustrate a comparison of reflection coefficients at port1 and port2 separately.



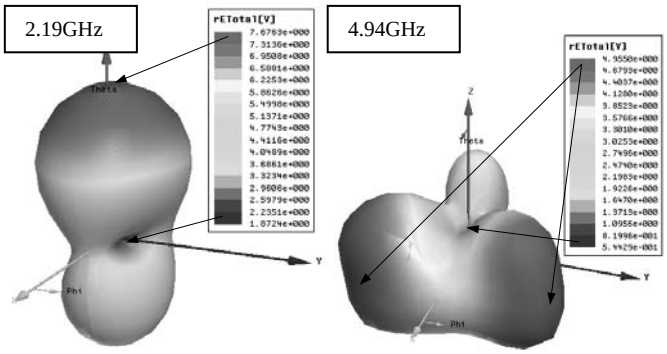
(a) Comparison of reflection coefficient S_{11} excited at port1



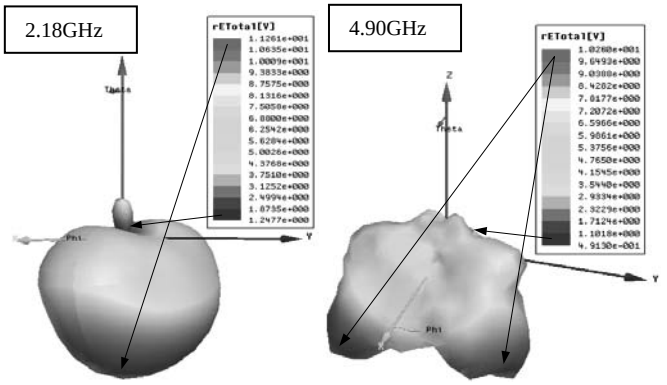
(b) Comparison of reflection coefficient S_{11} excited at port2

Fig. 5 Comparison of reflection coefficients

It is found that, although the resonant frequency is not significantly changed, the S_{11} is getting deeper and the radiation efficiency is dramatically increased with heatsink mounted. Some critical far-field distributions are compared as shown in Fig. 6. Detailed data is shown in next section.



(a) The far-field distribution (E field) of model without heatsink



(b) The far-field distribution (E field) of model with heatsink

Fig. 6 The far-field distribution (E field) of simulation models

B. Variation of Heatsink

In addition, simulations are executed under various configurations of heatsink in order to find how the heatsink changes the interference generation. All the results are given in TABLE 3 and TABLE 4. We assert CPU and heatsink can be treated as a very efficient antenna. In the meantime, no matter how the heatsink is being modified, the resonant frequency is barely changed, which means the resonant frequency of a microstrip patch antenna is dominated its structure and not easily affected by what it is mounted.

TABLE 3
COMPARISON OF KEY RESULTS UNDER DIFFERENT CONFIGURATION AT PORT1

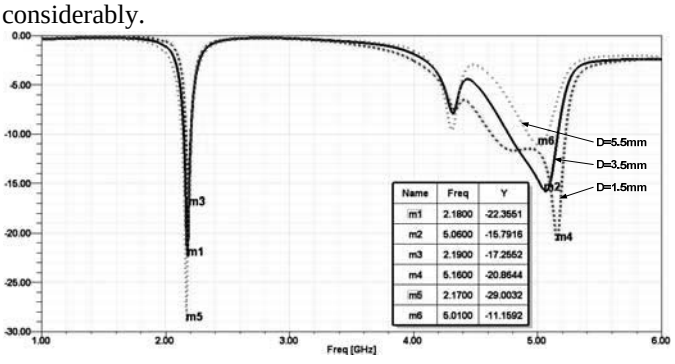
Heatsink Setup	Reflection coefficient		Radiation Efficiency
	GHz	dB	
Without heatsink	2.19	-20.24	58.01%
	5.03	-13.55	55.06%
With heatsink	2.18	-22.36	84.80%
	5.06	-15.79	85.68%
Only HH+5mm	2.18	-22.91	83.67%
	5.08	-15.67	79.96%
Only HH+10mm	2.18	-22.92	86.45%
	5.08	-15.65	80.01%
Only WH and LH +5mm	2.18	-22.73	84.92%
	5.07	-15.41	81.96%
Only WH and LH +10mm	2.18	-23.73	84.05%
	5.08	-15.26	79.15%
Round shape with same vol.	2.18	-24.04	76.42%
	5.07	-14.54	79.66%

TABLE 4
COMPARISON OF KEY RESULTS UNDER DIFFERENT CONFIGURATION AT PORT2

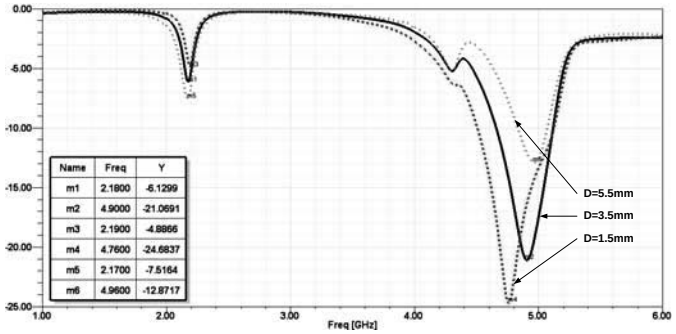
Heatsink Setup	Reflection coefficient		Radiation Efficiency
	GHz	dB	
Original without heatsink	2.19	-7.96	58.01%
	4.94	-15.87	60.66%
Original with heatsink	2.18	-6.13	84.80%
	4.90	-21.07	91.08%
Only HH+5mm	2.18	-6.12	83.67%
	4.92	-21.35	85.39%
Only HH+10mm	2.18	-6.22	86.45%
	4.92	-21.49	84.75%
Only WH and LH +5mm	2.18	-6.22	84.92%
	4.91	-21.15	90.07%
Only WH and LH +10mm	2.18	-6.19	84.05%
	4.92	-21.37	84.61%
Round shape with same vol.	2.18	-6.26	76.42%
	4.92	-22.61	85.53%

C. The distance between two dies

Beside the influence of heatsink, the die distance could also affect S_{11} as given in Fig. 7(a) and Fig. 7(b). The resonant frequencies are found changing with the distance (D) between dies. Especially the high resonant frequencies changes considerably.



(a) Comparison of reflection coefficient S_{11} excited at port1



(b) Comparison of reflection coefficient S_{11} excited at port2

Fig. 7 Comparison of reflection coefficients

IV. CONCLUSIONS AND FUTURE WORK

The model constructed in this paper presents how efficient a dual die CPU could be acting as an antenna creating electromagnetic interference. Different configurations are considered and discussed. It is found that the resonant frequency of the model is not easily affected by heatsink modification. However, it could be impacted by the distance between the two dies.

Furthermore, dual die excitation configurations, phase shift and further optimization of patch and size will continue to be studied. The validation of this model is also currently underway.

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