# Size Reduction of the Waveguide Feed Circuit for a Millimeter-Wave Dipole Antenna on a Thick Resin Layer on the Back Side of a Silicon Chip at 60GHz

<sup>#</sup>Tomoya Suzuki<sup>1</sup>, Jiro Hirokawa<sup>1</sup>, Yasutake Hirachi<sup>2</sup> and Makoto Ando<sup>1</sup>
<sup>1</sup> Dept. of Electrical and Electronic Eng., Tokyo Institute of Technology 2-12-1, O-okayama, Meguro-ku, Tokyo, 152-8552, Japan <sup>2</sup> AMMSYS. Inc. 844-1, Nikaido, Kamakura, Kanagawa 248-0002, Japan E-mail: suzuki\_tomoya@antenna.ee.titech.ac.jp

#### 1. Introduction

Recently, there are many discussions on integration of an antenna on a 60 GHz silicon CMOS chip. When the antenna is integrated on the same layer of a RF circuit, the radiation efficiency is quite low due to the small height (typically 10  $\mu$ m) of the RF circuit layer. When the antenna is integrated separately from the chip, the connecting loss is quite large (typically 2 dB). We proposed the configuration where an antenna is integrated on a thick resin layer on the opposite side of a RF circuit layer by feeding through a hole as shown in Fig.1 [1]. The thick resin layer can make the radiation efficiency larger and the connection loss can be small. We designed a dipole antenna on a 200  $\mu$ m -thick resin layer on the back side of a 5 mm square silicon chip at 60 GHz. The hole size was 2.0 mm by 1.0 mm, which was large in comparison with the size of the silicon chip. This paper proposes the size reduction of the feed circuit by decreasing the post diameter as well as the hole in the silicon chip.

#### 2. Antenna Structure

Figure 1 shows the antenna structure. The size of the silicon chip is 5 mm square. The antenna layer is placed on the opposite side of the layer for a RF circuit on a silicon chip.

The resin layer for the antenna takes a large height of 200  $\mu$ m to increase the radiation efficiency. The dielectric constant of the resin is 2.846 and the loss tangent is 0.0151 at 50 GHz by measurements. Copper is plated between the resin and the silicon to prevent from loss of the silicon. Two metal posts are placed in the hole for differential operation of the RF circuit. A dipole is used as a balanced antenna suitable for the differential operation. The posts had a tapered side wall with different diameter for the top side (*D*) and for the bottom side (*d*) to spread copper easily on the side wall. However the side wall in the previous fabrication became rough by making by a laser. The fabrication is improved to coat copper on a straight side wall with the same diameter (*D*=*d*) for the top and bottom sides in the post and to make the side wall smoother by milling as shown in Fig.3. Waveguide feed from the bottom side is adopted to demonstrate feasibility of the dipole antenna on the thick resin layer as shown in Fig. 2. An H-shaped aperture is opened in the bottom. The silicon chip is placed on a fixture with a diameter of about 20 mm equal to a circular flange of a hollow waveguide for measurement. The analysis includes the shape of the fixture. The hole size is *a* by *b*, which is determined so that the distance should be 0.1 mm between the side walls of the silicon hole and the posts. The antenna length q is adjusted to maximize the bandwidth for the reflection below -10 dB.

#### **3. Simulated Results**

Table 1 summarizes the antenna parameters for various values of *D*. The conductivity in the simulation is  $14.5 \times 10^6$  (S/m). Figure 4 shows the simulated reflection. The dotted line shows the previous model for (D,d)=(0.6,0.3) (in mm). The bandwidth was 7.1 %. The bandwidth for D=0.20 mm by the solid line, D=0.15 mm by the dashed line and D=0.10 mm by the dash-dotted line are 4.0 %, 7.7 %, 5.3 %, respectively. The double resonance is observed for D=0.20 mm and 0.15 mm, so that the bandwidth can increase. Figure 5 and 6 shows the directivity and the gain in simulation. The directivity for (D,d)=(0.6,0.3) (in mm) is 5.2 dBi at 60 GHz. Those for D=0.20 mm, D=0.15 mm and D=0.10 mm are 5.0 dBi, 6.7 dBi, 6.6 dBi, respectively. The directivity becomes larger for a thinner post because the antenna length becomes longer. The gain is 5.4 dBi for (D,d)=(0.6,0.3) (in mm). Those for D=0.20 mm, D=0.15 mm and D=0.10 mm is 4.8 dB, 6.3 dB, 6.2 dB, respectively. The loss due to material could be 0.2–0.4 dB.

#### 4. Conclusion

We have proposed the size reduction of the waveguide feed circuit for a dipole antenna on a silicon chip with 5 mm square at 60 GHz. The hole size has reduced from 2.0 x 1.0 mm for the post diameter D=0.6 mm and d=0.3 mm to 0.9 x 0.6 mm for D=d=0.2 mm, where the bandwidth is 4 % and

the gain is 4.8 dBi. We are trying to fabricate the antenna to show the measured result in the presentation.

### Acknowledgment

This work is in part supported by the research and development project for expansion of radio spectrum resources of the Ministry of Internal Affairs and Communications and JSPS Grant-in-Aid for Scientific Research (22246052).

## References

[1] K.Kimishima et al., "Feasibility Study of a Millimeter-Wave Antenna on an Thick Resin Layer on the Back Side of a Silicon CMOS Chip", IEICE Society Conf, B-1-164, 2008-09. (in Japanese)



Figure 2 Waveguide feed structure





(a) Top view (b) Cross sectional view Figure 3 Pictures for posts (D=0.2 mm)

*			
<i>D</i> [mm]	<i>a</i> [mm]	<i>b</i> [mm]	<i>q</i> [mm]
0.20	0.90	0.60	1.10
0.15	0.80	0.55	1.25
0.10	0.70	0.55	1.28

Table 1 Antenna parameters







Figure 5 Directivity



Figure 6 Gain