An Industry-Compliant Immunity Modeling Technique for Integrated Circuits

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***Abstract*— This paper introduces a new technique for immunity modeling of integrated circuits, compliant with industrial requirements. A specific modeling flow is introduced and validated through measurements performed on several devices.**

Keywords: immunity, integrated circuit, EMC model, ICIM, black-box modeling, Spice.

I. INTRODUCTION

Nowadays, the complexity and operation speed of electronic systems are getting higher and higher. Therefore, they are subject to many EMC issues, either in emission or immunity. In particular, integrated circuits (ICs) are one of the main causes of parasitic emission, while their immunity is decreasing. Consequently, EMC models of ICs are becoming compulsory for proper PCB- (printed circuit board) or system-level EMC simulations. Previous research has already led to the development of ICEM (Integrated Circuit Emission Model), addressing emission issues [1][2]. The use of such a model has already been validated to predict electromagnetic emission at PCB or system level [3][4].

Many studies have been conducted on immunity modeling of ICs, but these techniques are often difficult to implement in an industrial context. For example, in Boyer's [5] and Alaeldine's [6] approaches, model extraction generally requires information on the internal structure of the IC, which is not easy to collect. Besides, a black-box approach based on a neural technique has also been suggested by Chahine [7]; however, a huge amount of characterization is then required to generate an accurate model. In the aforementioned techniques, models can only be used in time domain to highlight IC failures (detection efficiency, jitter…).

Conversely, industrial constraints require another approach: ICs must be treated as black boxes, and only external information should be used to generate their models. Moreover, generation must be as fast as possible, and the resulting model should be usable in frequency domain. Therefore, this paper describes a new technique driven by these constraints.

The paper is organized as follows. Sect. II describes the structure and validity conditions of the model. Then, in Sect. III, the extraction flow is explained and illustrated through an example. Finally, Sect. IV summarizes the results obtained on various IC families, thus validating this technique and leading to new perspectives.

II. STRUCTURE OF THE SUGGESTED MODEL

A. Validity domain and assumptions

The suggested model is dedicated to the prediction of immunity behavior for continuous wave (CW) disturbances, in the 1 MHz - 3 GHz frequency range, and up to 36 dBm incident power in a direct power injection (DPI) test [8]. On a single IC, it can be deduced from experience that this corresponds more or less to the equivalent disturbance level induced by a system-level test such as bulk current injection (BCI) [9] or radiated immunity [10], for typical automotive applications and requirements.

The suggested model, like the ICEM model [1][2], is mainly based on a passive distribution network (PDN). For this model to be used in the frequency domain, it must be assumed that PDN impedances are constant and will not be influenced by the injected HF disturbance. This assumption of linearity is linked to the disturbance characteristics to be considered for immunity analysis. In the case of 36 dBm incident power in DPI, the voltage induced across a high-impedance input (worst case) is approximately 28 V. Seeing that non-linear effects affecting input impedances in ICs are mainly due to ESD protections, which are typically triggered by voltages from 30 to 40 V, it can be considered that such an assumption is realistic. Nevertheless, this must be systematically checked for model validation. For higher disturbance levels, or for high-voltage pulses, other techniques should be used, such as [5][6][7], including non-linear behaviors, or [11] for particular pulsed-wave considerations.

The second assumption states that a given device is always perturbed by a constant transmitted (or active) power through its inputs, and that passive devices, located around the IC in a real application, only define the transfer function for the disturbance from outside the system to the IC itself. The choice of this criterion is motivated by the requirement to settle for only external observations of ICs. Once more, this assumption must be validated by specific measurements.

Finally, a failure criterion in the IC model must be defined from the functional tolerances related to its use in the

application. This means that a given model is only valid for specific failure criteria, and that a set of models should be generated if different tolerances must be considered in an application.

B. Model Structure

The model structure corresponds to the current IEC standard proposal for the Integrated Circuit Immunity Model (ICIM) [12]. The first part of the model is based on a PDN structure which can be described with the same techniques as ICEM. This paper uses Spice polynomial black-box models obtained from direct S-parameter measurements thanks to the IdEM tool [13], sparing long and tedious modeling procedures.

The second part of the model consists of a table indicating the transmitted power triggering a failure as a function of frequency. This table makes it possible to state, in any configuration, if transmitted power goes reaches the threshold which generates a malfunction.

C. General extraction flow for the model

The objective of the extraction flow (Fig. 1) is to define some characterization steps to extract the PDN, to evaluate the transmitted power threshold, and to perform model validation.

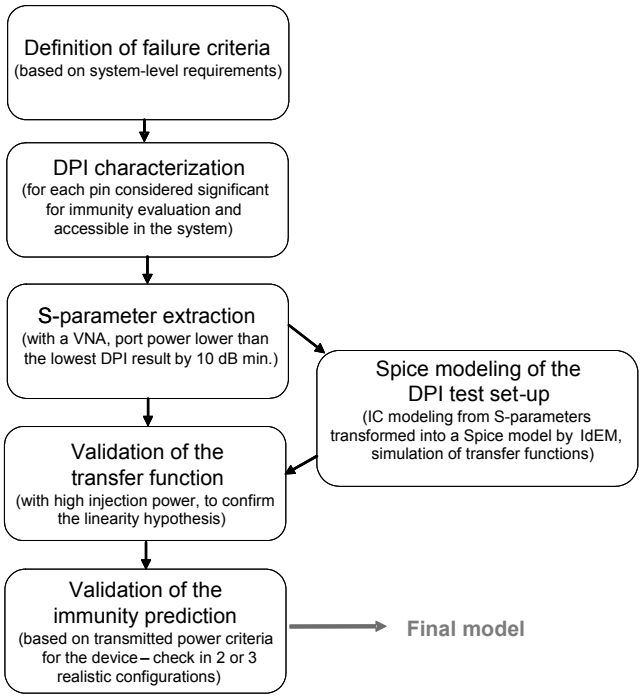

Fig. 1 Extraction and validation flow

The characterization requires a testing methodology and a test set-up which make it possible to determine the transmitted power accurately during the test. DPI and modeling techniques are indeed the most appropriate methods.

The PDN is then required to compute transmitted power. The other steps of the flow only validate the model, by checking the linearity assumption for the impedance and the validity of the active power criterion.

III. AN EXAMPLE OF MODEL EXTRACTION

A. Test case definition

The aforementioned flow will be detailed through a simple example, dealing with the case of a LIN transceiver. The failure criteria are the functional requirements defined in the LIN specification: ± 5 µs jitter and ± 2.5 V in amplitude on the LIN signal.

B. *DPI characterization*

Only the pins connected outside the system (LIN and 12V) will be considered for this test case. A specific test board is used, in order to control the injection path.

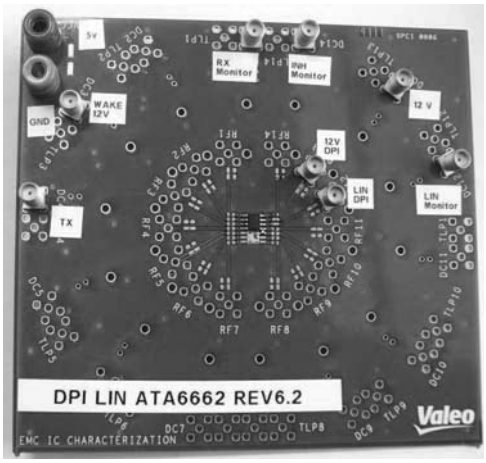

Fig. 2 Test board used for DPI characterization

As far as the 12V pin characterization is concerned, several tests are performed: the first one is a reference configuration without any filter, making it possible to obtain the actual transmitted power threshold. Two other configurations are also tested, with different decoupling capacitance values (100 pF or 10 nF), to provide additional results for the validation of the model. Results obtained on the 12V pin are given in Fig 3.

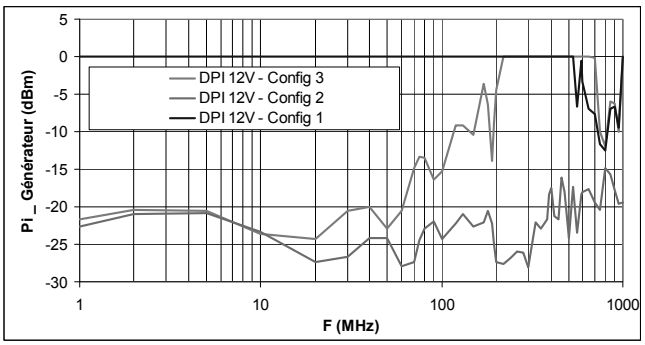

Fig. 3 DPI results: incident power triggering a failure
Config. 2: reference without any decoupling
Config. 1 and 3: with 10 nF or 100 pF decoupling

C. *Extraction of S-parameters*

After the DPI characterization, the S-parameters of the IC must be extracted, by considering each pin as a port (referenced to the ground pin of the IC). This step is

performed after the DPI tests, so that the vector network analyzer (VNA) can be configured with an incident power lower by at least 10 dB than the minimum identified disturbance level. Below the failure level, it can be considered that the linearity assumption is true but, as soon as the device is perturbed, this is not the case; for example, the impedance of a logic output will differ depending on its state, which can change due to the disturbance. The same PCB as in Fig. 2 is used, and a direct calibration is performed in the reference plane of the IC. This is achieved by using a specific calibration kit having the same traces (impedance and length) as the ones of the DPI board, and with the same implemented capacitances. Furthermore, a fine characterization of the calibration kit must be performed to ensure correct calibration and measurements.

Finally, the extracted S-parameters are transformed into a Spice model, using IdEM [13]. This corresponds to the PDN of the ICIM model.

D. *PCB modeling and extraction of the active power*

It can be noted that it is difficult to obtain, from direct measurements, the power transmitted to the IC itself; in fact, the use of a bidirectional coupler makes it possible to estimate the power transmitted to the whole PCB (including losses in traces, in coupling capacitances, in bias tee inductances …) and not only to the IC itself. In addition to that, the typical measurement uncertainty of wattmeters can reach ± 100% for highly mismatched devices.

Consequently, in order to estimate the power transmitted to the IC, a simulation based on a complete DPI set-up modeling is used. The PCB model is built up using well-known techniques: traces are modeled by transmission lines, devices by their equivalent model taking into account their parasitic elements, and the device under test by its PDN. The model displayed in Fig.4 corresponds to the DPI test on the 12V pin in the reference configuration. The amplifier, battery, LISN, coaxial cables and oscilloscope input impedance involved in the test are also replaced by their equivalent model in the simulation, as already explained in [5][6][7][14].

A simulation performed with a 0 dBm incident source provides the complex voltage and current in the pin under test. The active power can be then obtained from:

$$P_{active} = \frac{1}{2} \cdot \left(U \cdot I^{*} + U^{*} \cdot I \right) \qquad (1)$$

Seeing that the incident power triggering a failure and the actual power transmitted to the device for a 0 dBm incident power are both known, and that all models are linear, the active power threshold mentioned in Sect. II.B can be deduced.

From now on, all required data are available and will then be combined in order to generate the model.

E. *Validation of the model*

The first step of model generation consists in validating all the assumptions previously made.

The first assumption deals with linearity. In order to check it out, comparisons between measurements and simulations of the S_{21} parameter are performed for different configurations, and for an incident power close to the failure level (typically 3 dB below). This can be achieved by connecting port 1 of the VNA to the amplifier input, injecting into the 12V pin, and connecting port 2 on the LIN pin. This makes it possible to check out if the input impedance and the equivalent transfer impedance of the IC are still linear for such an injected power. An example is provided in Fig. 5. On this result, it can be noted that a 42-dB amplifier is used only up to 1 GHz, which explains the important variation observed at this frequency. Moreover, some oscillations are observed on measurements and not on simulations. They are due to the important reflected power into the amplifier which is not matched to 50 Ω anymore. It can be deduced that the assumption of linearity is valid up to 3 GHz, and that the complete simulation model is correct. This task is generally achieved for several configurations (such as S21 measurements with injection and measurement on the same pin, with the pin impedance in parallel) in order to come to a complete validation.

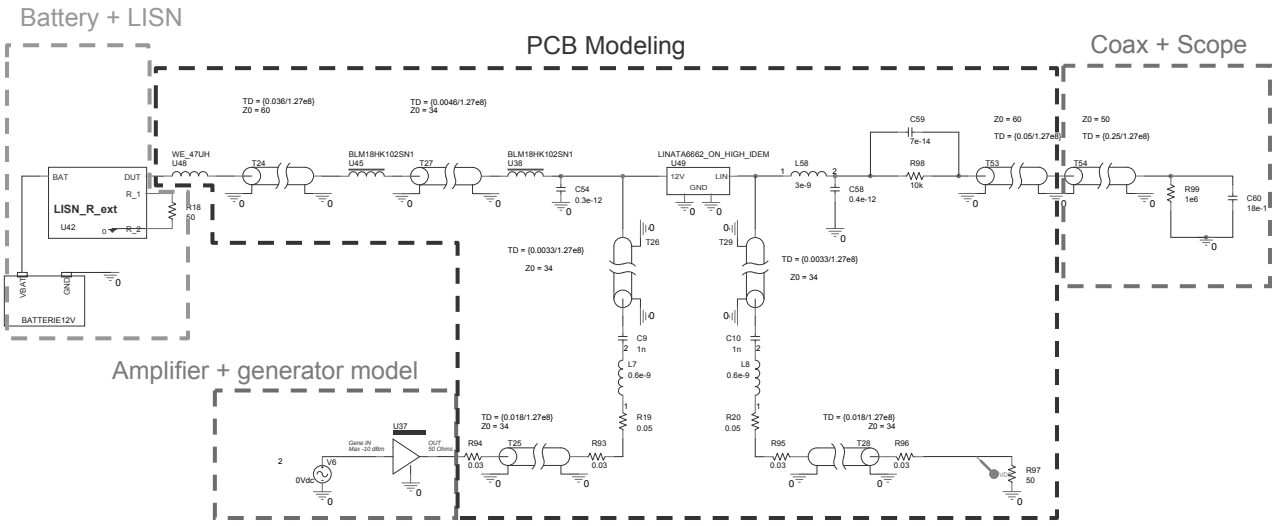

Fig. 4 Modeling of the DPI test set-up

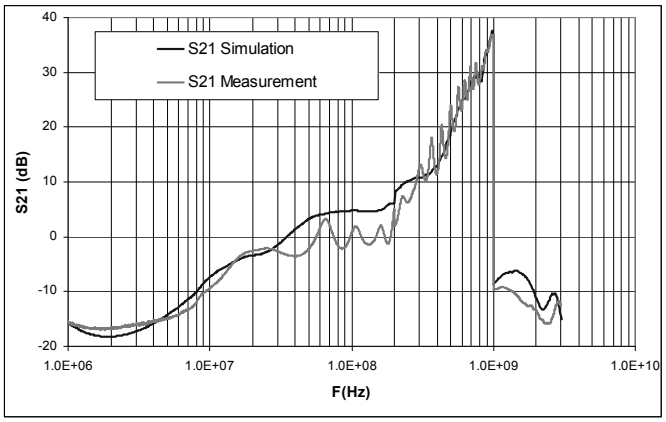

Fig. 5 Validation of the transfer function

Then, the active power criteria used to predict immunity in other configurations must be validated. Using the same model as in Fig. 4, modified according to the configuration to be estimated, the incident power required to reach the maximum power transmitted to the device which triggers a defect, in this second configuration, can be computed. In the case of the 100 pF capacitor, the results in Fig. 6 are obtained. Between 0 and -10 dBm (RF generator), some discrepancies between simulations and measurements are observed, due to the saturation effect of the amplifier which was not taken into account in this analysis. Nonetheless, these results demonstrate that the method can be validated.

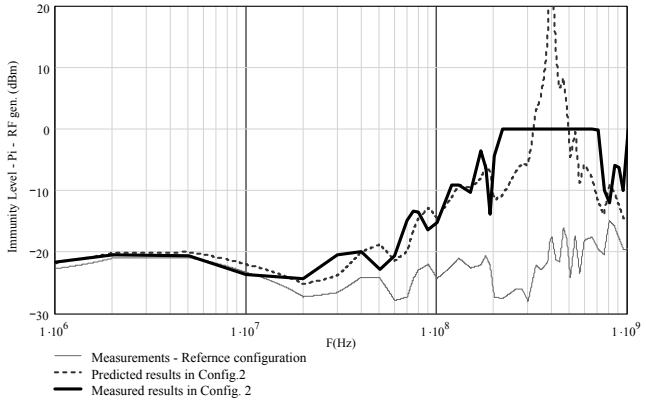

Fig. 6 Comparison between measurement and prediction

IV. Conclusion and Perspectives

In this paper, only partial results were given for a LIN transceiver, but these one are representative of the quality and accuracy obtained for the characterization of other pins (transfer function and immunity prediction). Other devices such as transistors, logic ICs (74HC08, 74HC14), other LIN transceivers, and voltage regulators, have been modeled up to 3 GHz as well, with the same quality.

A very interesting similar general trend was observed on the frequency behavior of the active power causing a malfunction on all these circuits. Average levels for some of the devices quoted above are plotted in Fig. 7. It can be noticed that this active power is generally constant in low frequency and increases linearly above a given frequency.

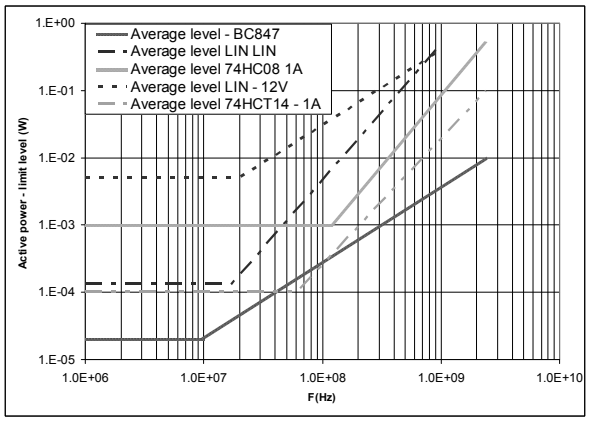

Fig. 7 Limit of the active power for several devices

These observations must be confirmed with other ICs but, nevertheless, provide interesting perspectives for the reduction of experimental characterization and the development of a semi-empirical approach to model generation, in the same manner as in the ICEM model.

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