Integrated Common-mode-noise Reduction Technique for LSI/PCB

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Abstract— A study was conducted on common-mode noise which is generated in the large-scale-integrated circuit (LSI) of an in-vehicle electronic device and flows through the printed circuit board (PCB) to the wiring harnesses. For a model circuit comprising an LSI, PCB and wiring harnesses, the model equation was solved to verify that common-mode noise in the wiring harnesses can be minimized by cancelling the unbalanced impedance of the LSI with respect to the ground plane using the impedances on the PCB. Test boards were fabricated, each containing a microprocessor adopted in actual electronic products, and experimental evaluation was conducted on these test boards to verify the effectiveness of this technique in reducing common-mode noise.

I. INTRODUCTION

Vehicles on the market today are each equipped with dozens of electronic devices to provide various functions to users. Many of these devices (including sensors and actuators) are interconnected via wiring harnesses. The total length of wiring harnesses per vehicle reaches several kilometers. Many signals are transmitted between these electronic devices, and some of these signals become noise affecting other devices. Under such circumstances, the importance of electromagnetic compatibility (EMC) of in-vehicle electronic devices has been increasing year by year. Development of an efficient noisereduction technique is being awaited to ensure EMC.

II. PROBLEMS WITH THE CONVENTIONAL TECHNIQUE

The common-mode-noise occurrence mechanism and reduction method have been studied and reported by several researchers.[1]-[4] We also conducted studies on these topics in the past using an evaluation system of an in-vehicle electronic device that comprised an electronic control unit (ECU) and wiring harnesses with no direct contact with the ground plane, to demonstrate that common-mode noise flowing in the wiring harnesses is the major cause of radiated noise and that the common-mode noise current can be minimized by adjusting the pattern and component impedances on the PCB.[5] Fig. 1 shows the model circuit used in our study. Expression 1 and 2 is a model equation for the noise-reduction condition.



Fig. 1 Current model circuit

$$\Delta V = \frac{Z_{VC} Z_{GC} \left(\frac{Z_{VL}}{Z_{VC}} - \frac{Z_{GL}}{Z_{GC}}\right)}{(Z_{VL} + Z_{GL})(Z_{VC} + Z_{GC}) + Z_{IN}(Z_{VL} + Z_{GL} + Z_{VC} + Z_{GC})} Z_{IN} \cdot I_{source} , I_{common} = \frac{\Delta V}{Z_{Harness}} (1)$$

$$\frac{Z_{VL}}{Z_{VC}} - \frac{Z_{GL}}{Z_{GC}} = 0$$
(2)

The above model equation expresses the power-wiring and ground-wiring impedances on the circuit board using a set of four impedance parameters. The current intensity is therefore constant throughout the board. The bypass capacitance on the board is concentrated at one point of the connector.

The PCB-side external impedance viewed from the LSI of the model circuit increases by the pattern impedance (Z_{VL} + Z_{GL}) and the board-impedance-adjusting term. This makes it difficult to suppress the impedance within a specified target range when designing an LSI. In addition, since a large number of components are mounted on an actual PCB, the noise transmission route is far more complex than in this model circuit. For these reasons, we have had difficulty in directly applying this model circuit to a PCB design.

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With the aim of solving the abovementioned problem, we have decided to correct the model circuit and newly develop a noise-reduction formula for the circuit which is expressed by the term for impedances of the circuit portion from the LSI (noise source) to the bypass capacitor near the LSI, and the term for PCB pattern impedances on the downstream side of the bypass capacitor.

III. COMMON-MODE NOISE IN LSI/PCB

Referring to the circuit diagram of Fig. 2, Z_{IN} represents the internal impedance of the LSI which is a noise source, Z_{IVL} and Z_{IGL} the pattern impedances in the circuit section before the bypass capacitor near the LSI, and Z_{IVC} and Z_{IGC} the respective impedances between these patterns and the ground plane. Z_{CAP} is the impedance of the abovementioned bypass capacitor and of the wiring pattern. The impedances in the circuit section from the bypass capacitor to the PCB connector are expressed by Z_{PVL} , Z_{PGL} , Z_{PVC} and Z_{PGC} .



Fig. 2 Proposed model circuit

The common-mode voltage for this circuit, when solved in terms of the difference between the midpoint potential of the connector and the ground-plane potential, is expressed as follows:

$$\Delta V = \frac{\left[Z_{IGC}Z_{PGC}[Z_{IVL}Z_{PVC}(Z_{PVL} + Z_{PGL} + Z_{CAP}) + Z_{PVL}Z_{CAP}[Z_{IVL} + Z_{IVC} + Z_{PVC}]\right]}{Z_{IVC}Z_{IGC}\left[\left[Z_{IVL}Z_{PVC}[Z_{IGL}Z_{PGC}(Z_{PVL} + Z_{PGL} + Z_{CAP}) + Z_{PGL}Z_{CAP}[Z_{IGL} + Z_{IGC} + Z_{PGC}]\right]\right]} + \frac{Z_{IVC}Z_{IGC}}{Z_{IVC}Z_{IGC}}\left[\left[Z_{IVL} + Z_{PVL} + Z_{IGL} + Z_{PGL}\right]Z_{PVC} + Z_{PGC}Z_{CAP}}{Z_{IVC}Z_{IGC}}\right]\right] + \left(Z_{IVL} + Z_{IGL}\right)\left[Z_{PVL} + Z_{PGL}\right]Z_{PVC} + Z_{PGC}\right]Z_{PVC} + Z_{PGC}Z_{CAP}}$$

$$+ \left[Z_{IVC} + Z_{IGC}\right]\left[\left(Z_{PVL} + Z_{PGL}\right)Z_{PVL} + Z_{PGC}\right]Z_{PVC} + Z_{PGC}Z_{CAP}} + Z_{ICC}Z_{IVL} + Z_{PVC}Z_{IGL} + Z_{PCC}Z_{IVL} + Z_{PCC}Z_{IVL} + Z_{PCL}Z_{IVL} + Z_{PCC}Z_{IVL} + Z_{PCL}Z_{IVL} + Z_{PCL}Z_{I$$

In the subsequent paragraphs, only the numerator of Expression 3 will be described for simplicity. The numerator of Expression 3 can be developed as follows:

$$- \begin{cases} Z_{IGC} Z_{PGC} \left[Z_{IVL} Z_{PVC} \left(Z_{PVL} + Z_{PGL} + Z_{CAP} \right) + Z_{PVL} Z_{CAP} \left(Z_{IVL} + Z_{IVC} + Z_{PVC} \right) \right] \\ - Z_{IVC} Z_{PVC} \left[Z_{IGL} Z_{PGC} \left(Z_{PVL} + Z_{PGL} + Z_{CAP} \right) + Z_{PGL} Z_{CAP} \left(Z_{IGL} + Z_{IGC} + Z_{PGC} \right) \right] \end{cases} \cdot Z_{IN} \cdot I_{\text{source}}$$

$$= -Z_{VVC}Z_{PVC}Z_{IGC}Z_{PGC}(Z_{PVL} + Z_{PGL} + Z_{CAP})$$

$$\left\{ \begin{bmatrix} \frac{Z_{VL}}{Z_{VC}} - \frac{Z_{IGL}}{Z_{IGC}} \end{bmatrix} + \frac{Z_{CAP}}{Z_{PVL} + Z_{PGL} + Z_{CAP}} \\ \begin{bmatrix} \frac{Z_{VL}Z_{PVL}}{Z_{VC}} - \frac{Z_{IGL}Z_{PGL}}{Z_{IGC}Z_{PGC}} + Z_{PVL} \end{bmatrix} - Z_{PGL} \begin{bmatrix} \frac{1}{Z_{IGC}} + \frac{1}{Z_{PGC}} \end{bmatrix} \end{bmatrix} \right\} \cdot Z_{IN} \cdot I_{source}$$

$$(5)$$

Since the patterned board of PCB is larger than that of LSI in general, the following relations hold:

$$Z_{IVC} >> Z_{PVC} \quad , Z_{IGC} >> Z_{PGC} \tag{6}$$

By using these assumptions (if the condition of Expression 6 is satisfied), Expression 5 can be simplified as follows:

$$\approx -Z_{IVC}Z_{PVC}Z_{IGC}Z_{PCC}(Z_{PVL} + Z_{PGL} + Z_{CAP}) \\ \left\{ \left[\left(\frac{Z_{IVL}}{Z_{IVC}} - \frac{Z_{IGL}}{Z_{IGC}} \right) + \frac{Z_{CAP}}{Z_{PVL} + Z_{CAP}} \left(\frac{Z_{PVL}}{Z_{PVC}} \left(1 + \frac{Z_{IVL}}{Z_{VVC}} \right) - \frac{Z_{PGL}}{Z_{PGC}} \left(1 + \frac{Z_{IGL}}{Z_{IGC}} \right) \right) \right] \right\} \cdot Z_{IN} \cdot I_{source}$$
(7)

The following term (Expression 8) of Expression 7 has been obtained by replacing the parameters of Expression 1 with the impedances of the LSI, and represents the unbalanced impedance of the LSI pattern on the upstream side of the bypass capacitor.

$$\frac{Z_{IVL}}{Z_{IVC}} - \frac{Z_{IGL}}{Z_{IGC}}$$
(8)

Expression 9 below comprises the impedance of bypass capacitor and the pattern impedances on the downstream side of the bypass capacitor, and represents the bypass effect of the bypass capacitor.

$$\frac{Z_{CAP}}{Z_{PVL} + Z_{PGL} + Z_{CAP}}$$
(9)

Expression 10 below represents the unbalanced impedance of the PCB.

$$\frac{Z_{PVL}}{Z_{PVC}} \left(1 + \frac{Z_{IVL}}{Z_{IVC}} \right) - \frac{Z_{PGL}}{Z_{PGC}} \left(1 + \frac{Z_{IGL}}{Z_{IGC}} \right)$$
(10)

It is clear from the above expressions that entirely balanced impedance between LSI and PCB is essential to reduce the common-mode noise of the PCB and LSI circuitry as a whole. However, it must be noted here that due to the effect of the bypass capacitor mounted midway in the circuit of the PCB, the impedance-balancing effect is smaller on the PCB board that on the LSI board. In order to balance the impedances in the entire circuitry by cancelling the unbalanced impedance of the LSI by the impedances on the PCB, therefore, it is necessary to adopt larger constants in comparison to the amount of unbalanced impedance of the LSI.

In the above expressions, if the pattern impedance to the connector and the impedance to the ground plane can be represented by inductance and stray capacitance, respectively, and if the impedance of the bypass capacitor is higher than that for the self-resonant frequency of the capacitor and can be represented by the parasitic series inductance " L_{ESL} ", i.e., if each of the conditional equations 11 below is satisfied:

$$\begin{split} & Z_{IVC} = \frac{1}{j\omega C_{IV}}, \quad Z_{PVC} = \frac{1}{j\omega C_{PV}}, \quad Z_{IGC} = \frac{1}{j\omega C_{IG}}, \quad Z_{PGC} = \frac{1}{j\omega C_{PG}} \tag{11} \\ & Z_{IVL} = j\omega L_{IV}, \quad Z_{PVL} = j\omega L_{PV}, \quad Z_{IGL} = j\omega L_{IG}, \quad Z_{PGL} = j\omega L_{PG}, \quad Z_{CAP} = j\omega L_{ESL} \end{split}$$

then Expression 7 can be rewritten as follows:

$$= \left\{ \left(L_{IV}C_{IV} - L_{IG}C_{IG} \right) + \frac{L_{ESL}}{L_{PV} + L_{PG} + L_{ESL}} \left[L_{PV}C_{PV}(1 - \omega^{2}L_{IG}C_{IG}) - L_{PG}C_{PG}(1 - \omega^{2}L_{IV}C_{IV}) \right] \right\}$$

$$\cdot \frac{j(L_{PV} + L_{PG} + L_{ESL})}{\omega C_{IV}C_{PV}C_{IG}C_{PG}} \cdot Z_{IN} \cdot I_{source}$$

$$(12)$$

Here, if the following relational expressions hold:

$$\omega << \frac{1}{\sqrt{L_{IV}C_{IV}}} \quad , \quad \omega << \frac{1}{\sqrt{L_{IG}C_{IG}}} \tag{13}$$

then Expression 12 can be simplified as follows:

$$\approx \left\{ \left(L_{IV}C_{IV} - L_{IG}C_{IG} \right) + \frac{L_{ESL}}{L_{PV} + L_{PG} + L_{ESL}} \left(L_{PV}C_{PV} - L_{PG}C_{PG} \right) \right\}$$

$$\cdot \frac{j(L_{PV} + L_{PG} + L_{ESL})}{\omega C_{IV}C_{PV}C_{IG}C_{PG}} \cdot Z_{IN} \cdot I_{source}$$

$$(14)$$

in which the parenthesized terms for minimizing the common-mode noise do not include a "w" term. Therefore, common-mode noise can be reduced over a wide frequency range (in the range in which all of the relational expressions 11, 13 and 15 are satisfied).

$$\left(L_{IV}C_{IV} - L_{IG}C_{IG}\right) + \frac{L_{ESL}}{L_{PV} + L_{PG} + L_{ESL}} \left(L_{PV}C_{PV} - L_{PG}C_{PG}\right) = 0$$
(15)

IV. EXPERIMENTAL EVALUATION

To verify the theoretical expressions mentioned above, we conducted the experiment described in the following. The experiment used an LSI (single-chip microprocessor H8S-2134 manufactured by Renesas Technology Corp.) adopted in actual in-vehicle electronic devices. For the experiment, we fabricated LSI and PCB boards separately. The LSI board included an LSI and the pattern up to the capacitor near the LSI. The PCB constituted the external circuit for the LSI. The LSI board measured 50 mm \times 50 mm, and the PCB measured 50 mm \times 100 mm (FR-4, double-sided board 1.6 mm in thickness). Fig. 3 shows the external view of these boards.



Fig. 3 Evaluation PCBs. The left side is LSI board. The right side is PCB board.

On the LSI board, the power wiring and ground wiring were patterned to the same length and width to prevent a pattern-attributed impedance mismatch. A capacitor (ceramic capacitor 1.6mm \times 0.8mm in size, with a capacitance of 0.1 μ F) was located near the power terminal to ensure that the capacitor would work stably, independent of impedance variation on the PCB.

Four PCBs were fabricated, each having a power-wiring pattern and ground pattern with or without solid pattern. The solid power/ground pattern was 80 mm × 42 mm in size.

For the experiment, additional chip inductors (1.6mm×0.8mm in size, with a inductance of 1nH~330nH) were mounted at the connector of each PCB to adjust the

impedances on the PCB using the board impedance and chipinductor impedance.

Three-dimensional electromagnetic analysis was conducted on the PCB using an Ansoft Q3D extractor to extract pattern impedances. Table 1 shows the result of PCB impedance calculations.

EXTRACTED IMPEDANCE OF PCB					
Pattern Width VCC side / GND side	C _{₽V} [pF]	C _{PG} [pF]	L _{PV} [nH]	L _{PG} [nH]	
Narrow / Narrow	0.916	0.854	38.2	37.8	
Wide / Narrow	2.14	0.641	18.6	55.7	
Narrow / Wide	0.527	2.24	56.1	18.4	
Wide / Wide	1.78	1.69	27.1	27.1	

TABLE I

Fig. 4 shows the appearance of the experimental system. The abovementioned package board is connected to a 1,500 mm long wiring harness, and driven with power supplied via the line impedance stabilization network (LISN) which is attached to the other end of the harness to regulate the voltage between 9 V and 5 V. A current probe (Model 94111-1 manufactured by ETS-Lindgren) is positioned at a point 50 mm away from the PCB to measure the common-mode noise at this point using a spectrum analyzer (Model E4407B manufactured by Agilent Technologies).



Fig. 4 A measurement setup of common-mode current evaluation.

The measuring frequency is set at 32, 64, 96, 128, 160, 192, 224, 256 and 288 MHz, which are even harmonics of the microprocessor clock (16 MHz).

The experiment was conducted first with board No. 1 connected for an LSI board. The common-mode noise current was decreased virtually uniformly with increase in L_{PV}, it was not possible to identify the point at which the commonmode noise would be minimized. This is presumably because the unbalanced impedance of the LSI could not be cancelled by the impedances on the PCB. Based on this result, the experiment was conducted next with board No. 2, which has a larger product of constants (inductance × capacitance) on the power-supply side than on board No. 1. Fig. 5 shows the result.



Fig. 5 Measured peaks results of common-mode current at even harmonics frequency of 16 MHz.

The result shown in Fig. 5 reveals that board No. 2 provides the smallest common-mode current value at around additional component's constants of additional $L_{PV} = 33$ nH and additional $L_{PG} = 1$ nH. At all measuring frequencies except 32 MHz, the common-mode noise was minimized at around this point. The result at 32 MHz differed from those at other frequencies presumably for the following reason: since the frequency of 32 MHz is close to the resonant frequency of the bypass capacitor, the "Z_{cap}" characteristics do not satisfy Expression 11, unlike at other frequencies.

Next, the inductance value of the chip inductor mounted on board No. 2 was added to Table 1, and the impedances on board 2 were calculated using Expression 16 below. Table 2 shows the result.

$$\frac{L_{ESL}}{L_{PV} + L_{PG} + L_{ESL}} (L_{PV}C_{PV} - L_{PG}C_{PG})$$
(16)

 TABLE II

 Relation between noise average value and expression 16

Add. L _{PV}	Add. L _{PG}	Average of Noise 32MHz to 288MHz	(16)
1nH	330nH	4.70 dBuA	-1.03e-18
1nH	100nH	3.12 dBuA	-0.69e-18
1nH	33nH	1.54 dBuA	-0.32e-18
1nH	10nH	0.86 dBuA	-0.06e-18
1nH	3.3nH	0.66 dBuA	0.05e-18
1nH	1nH	-0.16 dBuA	0.11e-18
3.3nH	1nH	-0.50 dBuA	0.28e-18
10nH	1nH	-1.61 dBuA	0.61e-18
33nH	1nH	-4.11 dBuA	1.39e-18
100nH	1nH	-3.01 dBuA	2.51e-18
330nH	1nH	3.07 dBuA	3.52e-18

It is clear from this table that the common-mode noise is minimized when the result of calculation with Expression 16 is 1.39e-18. If Expression 16 is satisfied under the conditions at which the common-mode noise is minimized, the amount of unbalanced impedance of the microprocessor package subjected to the present experiment, calculated using Expression 16 below, will be somewhere between -0.61e-18 and -2.51e-18.

$$-2.51e - 18 < L_{IV}C_{IV} - L_{IG}C_{IG} < -0.61e - 18$$
 (17)

It has conventionally been difficult to determine the unbalanced impedance of an LSI board because of difficulty in identifying the current flow route and internal LSI impedance from the outside. It is significant in this regard that the technique described above can be used to determine the effective unbalanced impedance of an LSI board.

As indicated by Expression 7, large unbalanced impedance occurring in the LSI board is difficult to cancel on the PCB since it is difficult for the components and patterns on the PCB to provide sufficiently large constants. To achieve integrated design of LSI and PCB, therefore, it is essential to estimate the unbalanced impedance of the LSI in advance and build a common-mode-noise reduction design into the LSI. In the example employed for the present experiment, the impedance of the LSI board can be balanced if the powerwiring inductance or capacitance of the LSI is increased.

V. CONCLUSION

We studied common-mode noise which is generated in the LSI of an in-vehicle electronic device and flows through the PCB to the wiring harnesses. The model equation for a model circuit was solved to verify that common-mode noise in the wiring harnesses can be minimized by cancelling the unbalanced impedance between the LSI and the ground plane using the impedances on the PCB. Based on this, we have experimentally demonstrated that the unbalanced impedance of an LSI can be determined through inverse calculations if a PCB with known impedance is used. It has also been demonstrated that feedback of this result to the design process of LSI would make it possible to achieve integrated reduction of common-mode noise in the LSI/PCB package.

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