LECCS-core Model Including Inter-Block Coupling for an LSI with Multiple Power-Supply Pins

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***Abstract*— An EMC macro model for LSIs, called the LECCS-core model, is under development for simulating high frequency noise in power supply currents. An LSI usually consists of core blocks plus I/O blocks. In this report, we show that a microcontroller's I/O block has AC coupling to the core block at high frequencies that affects the impedance characteristics of the core circuit. We enhanced the conventional LECCS-core model by adding AC coupling to I/O blocks. In the new model, transfer impedance between two core supply terminals is simulated under different external conditions on the I/O block. The simulation result shows a good agreement with measurement results.**

Key words: EMC macro model, LECCS-core model, inter-block coupling, S-parameter

I. INTRODUCTION

EMI problems are a growing problem, since high frequency current-carrying circuits are becoming commoner due to higher clock frequency and the increasing density of transistors integrated into LSIs. It is therefore desirable to simulate dynamic current during the early stages of circuit design. We have developed and are improving an EMC macro model of an LSI that will enable this to be done more efficiently [1]. We also have been developing an EMC macro model called the LECCS (Linear Equivalent Circuit and Current Sources) model [2]. In the LECCS model, the LSI is represented by several sets of linear equivalent circuits and current sources. Since the LECCS model is constructed of linear elements only, it is possible to analyze high frequency current faster than using non-linear models such as the SPICE model.

Most LSIs have two types of blocks: CORE blocks and I/O blocks, which are classified according to whether external connections other than power and ground connections are present or not, as shown in Fig. 1. We therefore model these two blocks separately.

When formulating the model, we first measured DC resistance between two power pins. If high DC resistance was measured between blocks, they were modeled separately. On the other hand, if a low resistance was measured, they were modeled together as one block. However, if an LSI has numerous core blocks and I/O blocks, it is difficult to model it correctly using this method, since some blocks experience AC coupling, even if they do not have direct DC connections. The purpose of this study is to include high-frequency AC coupling in the LECCS model.

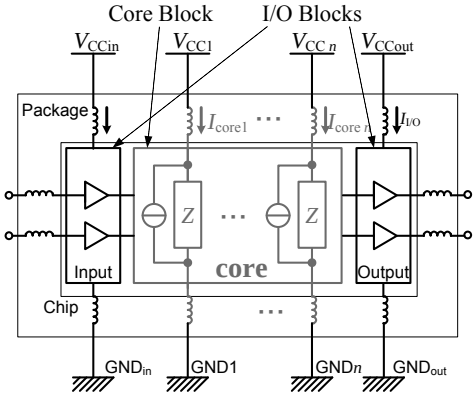

Fig. 1 Model for power distribution network of an LSI

II. CONVENTIONAL LECCS-CORE MODEL OF AN LSI

In this study, our target LSI for modeling was the H8S/2623, a microcontroller made by Renesas Technology, packaged in a 100-pin quad flat package (QFP). TABLE I shows the names and numbers of the power/ground pins of this LSI. This controller has three circuit blocks with 8 pairs of power/ground pins and a power pin for reference voltage (VREF). Here we modeled this controller as a LECCS-core model with 8 ports, since there is no resistance between VREF and AVCC, which are power pins for the analog circuit.

TABLE I

NAMES AND NUMBERS OF POWER/GROUND PINS

Circuit Block	Supply voltage	Power pin name (number)	Ground pin name (number)	Port
Core	3.3 V	VCC (6)	VSS (8)	Core1
		PLLVCC (59)	PLLVSS (57)	Core2
		VCC (63)	VSS (65)	Core3
I/O	5 V	PVCC1 (17)	VSS (15)	I/O1
		PVCC2 (39)	VSS (37)	I/O2
		PVCC3 (52)	VSS (54)	I/O3
		PVCC4 (97)	VSS (95)	I/O4
Analog	5 V	VREF (77)	VSS (94)	Analog
		AVCC (76)		

In our previous study, this controller was modeled as a combination of six independent one-port models and a two-port model, as shown in Fig. 2, since the DC resistance between Core1 and Core3 is small in comparison with the resistances between the other power pins [2]. Fig. 3 shows the details of the conventional two-port Z_{CORE13} model.

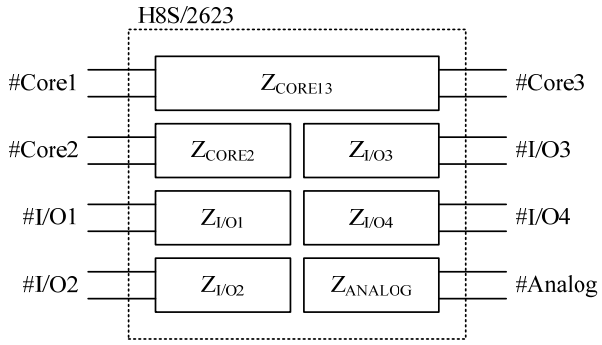

Fig. 2 Conventional model of H8S/2623

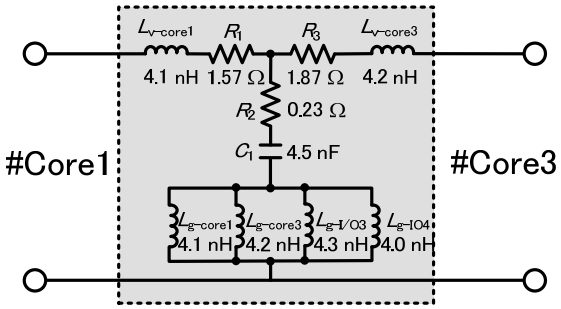

Fig. 3 Conventional model of Z_{CORE13}

III. INTER-BLOCK COUPLING

A. *Evaluation of inter-block coupling by S-parameter*

In conventional modeling methods, an LSI is divided into several blocks based on DC resistances between power supply pins. Next, each block is modeled one by one. If there is low DC resistance between the power supply pins, they are thought to belong to the same block. However, when using DC resistance, it is not possible to take into account AC coupling between blocks in the model.

To confirm how large couplings exist between blocks, we measured S-parameters using the evaluation PCB shown in Fig. 4.

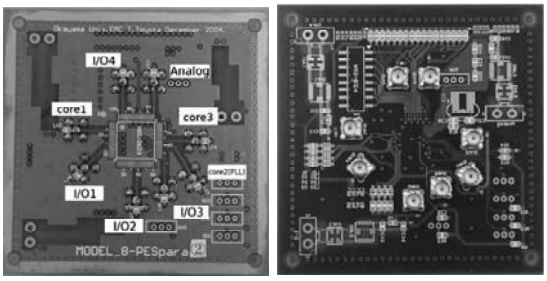

Fig. 4 Evaluation PCB for measurement of S-parameter

Fig. 5 and Fig. 6 show the measurement results of S-parameters. Here we assume that AC coupling exists between ports when the S-parameter exceeds -26 dB (5%): the I/O1 port has AC coupling with the Core1 and Core3 ports in the frequency range above 150 MHz. Therefore, AC coupling with the I/O1 port needs to be added to the model of Core1 and Core3, as shown in Fig. 7.

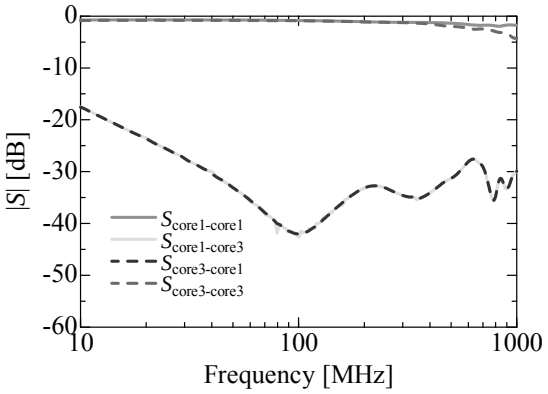

Fig. 5 S-parameters between Core1 port and Core3 port

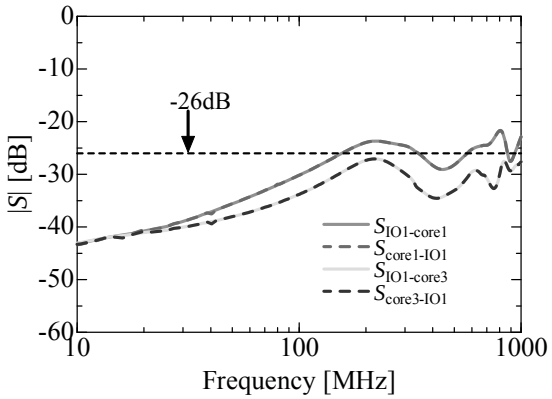

Fig. 6 S-parameters between I/O1 port and Core1, Core3 port

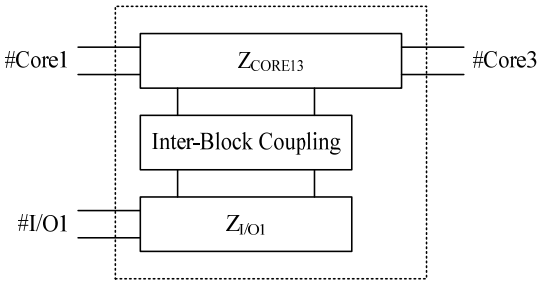

Fig. 7 3-port model with inter-block coupling

B. *Construction of 3-port LECCS-core model*

To build the 3-port LECCS-core model, we calculated the Z-parameters from the S-parameters. Fig. 8 shows the magnitude of the Z-parameters calculated. Port 1, 2 and 3 represent the Core1 port, Core3 port and I/O1 port, respectively, in Fig. 8. Since Z_{12}, Z_{13} and Z_{23} are almost the same as Z_{21}, Z_{31} and Z_{32}, respectively, they are not shown in Fig. 8.

We then extracted the equivalent circuit from the Z-parameters by means of symbolic analysis [3], [4]. The details of the symbolic analysis are explained in the Appendix.

Construction of an equivalent circuit configuration is the most important part of the symbolic analysis. We assumed it to be as shown in Fig. 9: we placed a capacitance (C_{IBC1}) and a resistance (R_{IBC1}) in series between the power side of Z_{CORE} and the ground side of $Z_{I/O1}$, and a capacitance (C_{IBC2}) and a resistance (R_{IBC2}) in reverse series. We assumed a capacitive coupling to exist between the power line and the ground line due to parasitic capacitances in the LSI. We also set two mutual inductances (M_{POW} and M_{GND}), to model inductive couplings at the lead frame.

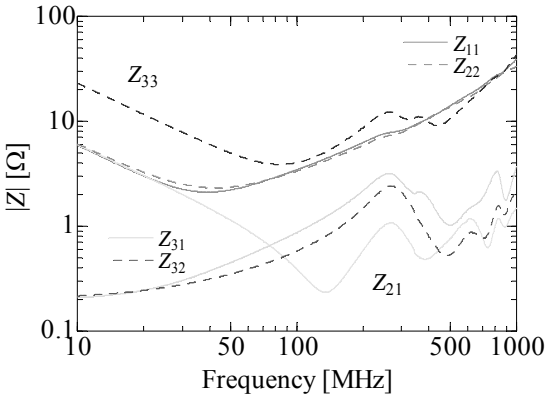

Fig. 8 Magnitude of Z-parameters

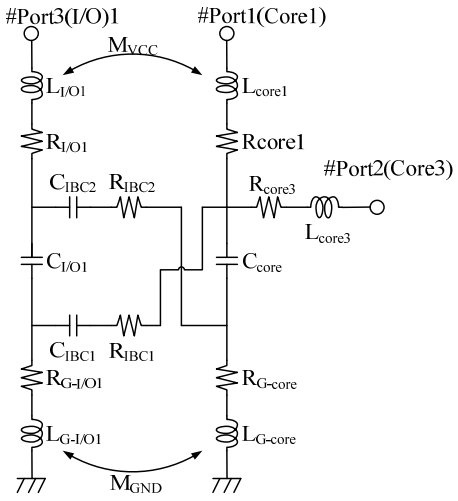

Fig. 9 Configuration of equivalent circuit

TABLE II shows circuit parameters of the equivalent circuit obtained by symbolic analysis. We used the data in the frequency range from 10 MHz to 500 MHz. Fig. 10 shows the comparison between the simulated Z characteristics of the equivalent circuit and the measured Z characteristics. In Fig. 10, dotted lines and solid lines represent simulated results and measurement results, respectively. We can see a good agreement between the simulated and measured results up to 300 MHz.

TABLE II

CIRCUIT PARAMETERS OF THE EQUIVALENT CIRCUIT

Parameter	Value	Parameter	Value
R_{core1}	2.48 Ω	$L_{I/O1}$	3.05 nH
R_{core3}	2.47 Ω	$L_{G\text{-}core}$	0.209 nH
$R_{I/O1}$	3.09 Ω	$L_{G\text{-}IO}$	1.97 nH
$R_{G\text{-}core}$	0.0958 Ω	C_{core}	1.99 nF
$R_{G\text{-}I/O1}$	0.895 Ω	$C_{I/O1}$	0.698 nF
R_{IBC1}	0.0347 Ω	C_{IBC1}	0.506 nF
R_{IBC2}	0.001 Ω	C_{IBC2}	0.001 nF
L_{core1}	4.06 nH	M_{VCC}	0.145 nH
L_{core3}	3.91 nH	M_{GND}	0.585 nH

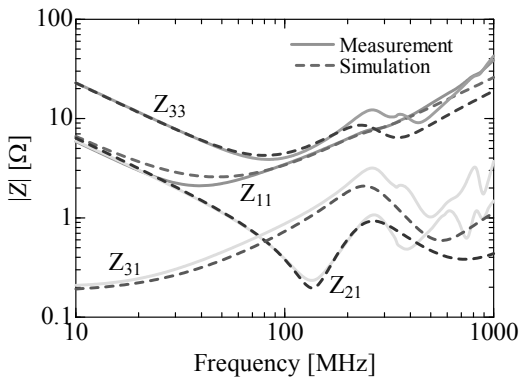

Fig. 10 Comparison of Z characteristics

IV. CONFIRMATION OF MODEL ACCURACY

To confirm the accuracy of the 3-port model, we simulated transfer characteristics between Core1 port and Core3 port, with the I/O1 port terminated in two ways. One is by connecting a bypass capacitor and the other is open. Fig. 11 shows the simulation model when using the capacitor. The parameters of the capacitor (C_{bypass}, ESR and ESL) are 0.01 μF, 0.01 Ω and 1 nH. We connected an external current source to the Core1 port and monitored the voltage at Core3 port. When the external current source is set to 1 A in the 10 MHz – 1 GHz frequency range, the voltage at Core3 indicates the transfer impedance Z_{21} from Core1 to Core3.

Fig. 12 shows a comparison of simulated results and measurement results. The solid line and dotted line in Fig. 12 represent simulated results and measured results, respectively, and the red line and blue line represent those with a capacitor and without a capacitor, respectively. We were able to confirm a good agreement up to 300 MHz.

When using a capacitor, the frequency of the 1st resonance is higher than without the capacitor, demonstrating that the inductance has been reduced by connecting a capacitance to the I/O1 port. When the I/O1 port is open-terminated, the inductance ($L_{G\text{-}I/O1}$) is only connected to the core model through the mutual inductance (M_{GND}). However, with a capacitor, $L_{I/O1}$ and $L_{G\text{-}I/O1}$ are connected in parallel through the M_{GND}, since the capacitance is closely equivalent to short termination in the high frequency range; and connecting a capacitor is equivalent to connecting the I/O1 port to the ground. Since the 3-port model includes inter-block coupling,

we can simulate the difference in transfer impedance between the Core1 port and the Core3 port, including the effect of I/O1 port termination.

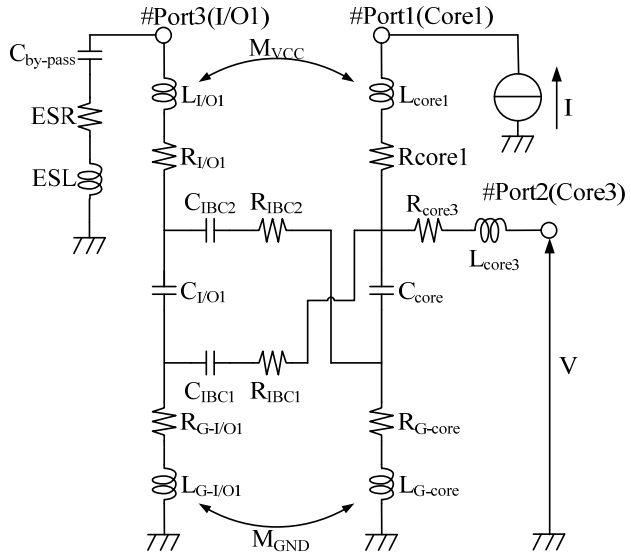

Fig. 11 Simulation model for transfer characteristic between Core1 and Core3

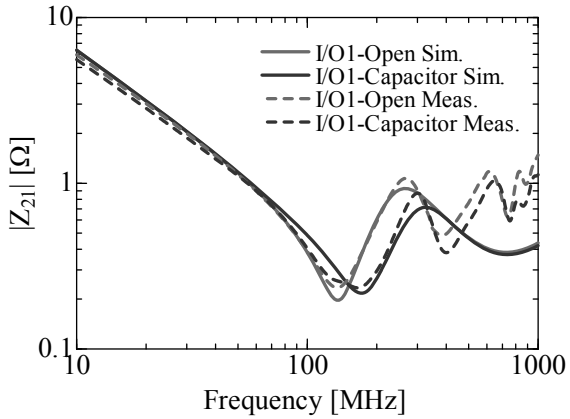

Fig. 12 Comparison of simulated results and measurement results

V. CONCLUSION

In this paper, we confirmed inter-block coupling in an 8-bit microcontroller by using S-parameters. As a result, we verified AC coupling between the core block and the I/O block, even though there is a large DC resistance between them.

We built a 3-port LECCS-core model including inter-block coupling by means of symbolic analysis. We simulated the transfer characteristics between the core ports, including I/O port termination, using the 3-port model and compared the results with actual measurements. We were able to confirm a good agreement between these results up to 300 MHz.

In future studies, we will extend the multiport LECCS model to a higher frequency range.

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APPENDIX

EXTRACTION METHOD USING SYMBOLIC ANALYSIS

We extracted the equivalent circuit parameters using the following procedure.

1. Determining the structure of the equivalent circuit.
2. Extracting the equations of the Z parameters in the complex frequency domain. Here, the circuit parameters are variables.
3. Fitting the circuit parameters.

In Step 2, the Z matrix can be represented as functions of the Laplace operator "s" and the circuit parameters, as below.

$$Z(s) = f(s; C_{core}, C_{I/O1}, \cdots, R_{G-core}, R_{G-I/O1}) \quad (1)$$
$$= f(s; \mu) \quad (2)$$
$$\mu = (Ccore, \cdots, R_{G-I/O1})^T, \ \mu \in \mathbb{R}^{n_\mu} \quad (3)$$

Here, $n_\mu \in \mathbb{N}$ and n_μ is the dimension of the circuit parameters. $Z(s)$ can thus be represented by using elements of 3-port Z parameters in the following way.

$$Z_{11}(s) = (A_{11} + \cdots + B_{11} \cdot s^5) / (C_{11} \cdot s + \cdots + D_{11} \cdot s^4) \quad (4)$$
$$A_{11} = (C_{IBC1} + C_{I/O1})$$
$$B_{11} = (C_{IBC1}C_{IBC2}C_{I/O1}C_{core}L_{core1}L_{G-core}R_{IBC2} + \cdots)$$
$$C_{11} = (C_{IBC1}C_{core} + \cdots + C_{IBC2}C_{I/O1})$$
$$D_{11} = (C_{IBC1}C_{IBC2}C_{I/O1}C_{core}L_{G-core}R_{IBC2} + \cdots)$$
$$\cdots$$
$$Z_{33}(s) = (A_{33} + \cdots + B_{33} \cdot s^5) / (C_{33} \cdot s + \cdots + D_{33} \cdot s^4) \quad (5)$$

To extract the above equations, we used SAPWIN[1], which is Windows PC software.

We can calculate the magnitude and phase of Z parameters by substituting $j\omega_i$ for s at the frequency ω_i.

$$Z(\omega_i) = f(j\omega_i, \mu) \quad (6)$$
$$Z_{11}(\omega_i) = \{A_{11}+B_{11}(j\omega_i)^5\}/\{C_{11}(j\omega_i)+D_{11}(j\omega_i)^4\} \quad (7)$$
$$\cdots$$
$$Z_{33}(\omega_i) = \{A_{33}+B_{33}(j\omega_i)^5\}/\{C_{33}(j\omega_i)+D_{33}(j\omega_i)^4\} \quad (8)$$

When $\zeta(\omega_i)$ represents the measured Z parameter, the evaluation function, F_{val}, is defined as below.

$$F_{val} = \Sigma W(\omega_i) \cdot [\log\{Z_{MAG}(\omega_i)\} - \log\{\zeta_{MAG}(\omega_i)\}]^2 + \Sigma W(\omega_i) \cdot \{Z_{PHA}(\omega_i) - \zeta_{PHA}(\omega_i)\}^2 \quad (9)$$

Here, $W(\omega_i)$ is a weight function and a function of frequency. In this paper, $W(\omega_i)$ is set to 1 in the frequency range, in which the S parameter exceeds -26 dB and it is set to 0.5 in other frequency ranges. The circuit parameters, $\mu = (C_{core}, \cdots, R_{G-I/O1})^T$, are calculated to minimize F_{val} interactively in the 3rd step. We used the Matlab Optimization Toolbox to minimize F_{val}.

[1] SAPWIN can be downloaded from http://cirlab.det.unifi.it/Sapwin.